JEDEC STANDARD

DDR5 SDRAM

JESD79-5D_v1.41

(Revision of JESD79-5C.01_v1.31, July 2024)

November 2025

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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DDR5 SDRAM

(From JEDEC Board Ballot JCB-25-78, formulated under the cognizance of the JC-42.3 Subcommittee on Dynamic RAMs (DDRx), item number 1848.99R).

1 Scope

This standard defines the DDR5 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 8 Gb through 32 Gb for x4, x8, and x16 DDR5 SDRAM devices. This standard was created based on the DDR4 standards (JESD79-4) and some aspects of the DDR, DDR2, DDR3, and LPDDR4 standards (JESD79, JESD79-2, JESD79-3, and JESD209-4).

1.1 JM7 Verbal Forms and Terms

JEDEC manual JM7 provides examples and directives for the use of verbal forms (e.g., ‘shall’ compared with ‘should’ and ‘may’ compared with ‘can’).

This standard adheres to the verbal forms defined in JM7A - July 2024 revision.

2 DDR5 SDRAM Package, Pinout Description, and Addressing

2.1 DDR5 SDRAM Row for X4, X8

The DDR5 SDRAM x4/x8 component shall have 13 electrical rows of balls. Electrical is defined as rows that contain signal ball or power/ground balls. There may be additional rows of inactive balls for mechanical support.

2.2 DDR5 SDRAM Ball Pitch

The DDR5 SDRAM component shall use a ball pitch of 0.8mm by 0.8mm.
The number of fully depopulated columns is 3.

2.3 DDR5 SDRAM Columns for X4, X8

The DDR5 SDRAM x4/x8 component shall have 6 electrical columns of balls in 2 sets of 3 columns. There shall be columns between the electrical columns where there are no balls populated. The number of these is 3. Electrical is defined as columns that contain signal ball or power/ground balls. There may be additional columns of inactive balls for mechanical support.

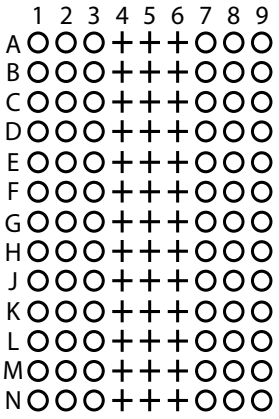
2.4 DDR5 SDRAM x4/8 Ballout Using MO-210

Table 1 — DDR5 SDRAM x4/8 Ballout Using MO-210

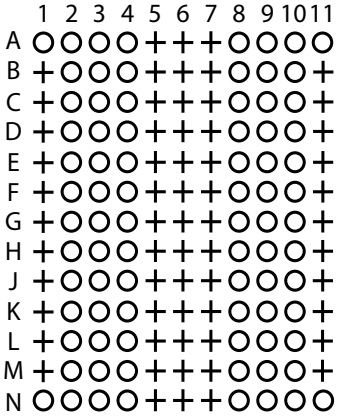
AN	1	2	3	4	5	6	7	8	9	10	11	
AL		1	2	3	4	5	6	7	8	9		
A	DNU	LBDQ	VSS	VPP				ZQ[7]	VSS	LBDQS	DNU	A
B		VDD	VDDQ	DQ2				DQ3	VDDQ	VDD		B
C		VSS	DQ0	DQS_t				DM_n[4], TDQS_t[2]	DQ1	VSS		C
D		VDDQ	VSS	DQS_c				TDQS_c[3]	VSS	VDDQ		D
E		VDD	DQ4[1]	DQ6[1]				DQ7[1]	DQ5[1]	VDD		E
F		VSS	VDDQ	VSS				VSS	VDDQ	VSS		F
G		CA_ODT	MIR	VDD				CK_t	VDDQ	TEN[5] (CS1_n[5])		G
H		ALERT_n	VSS	CS_n				CK_c	VSS	VDD		H
J		VDDQ	CA4	CA0				CA1	CA5	VDDQ		J
K		VDD	CA6	CA2				CA3	CA7	VDD		K
L		VDDQ	VSS	CA8				CA9	VSS	VDDQ		L
M		CAI, ZQ1[8]	CA10	CA12				CA13	CA11	RESET_n		M
N	DNU	VDD	VSS	VDD				VPP	VSS	VDD	DNU	N

NOTE 1 DQ4-DQ7 are higher order DQ pins and are not connected for the x4 configuration.
NOTE 2 TDQS_t is not valid for the x4 configuration
NOTE 3 TDQS_c is not available for the x4 configuration
NOTE 4 DM_n not valid for the x4 configuration
NOTE 5 For single die package (SDP) or 3DS, this pin is TEN; CS1_n is not connected, and is used as Test Mode Enable. For dual die package (DDP), this pin is CS1_n; and TEN is disconnected, and is used as CS1_n.
NOTE 6 The electrical parameters for DDP package are TBD and will be covered from future ballots.
NOTE 7 For dual die package (DDP), ZQ is connected to bottom die (Rank 0).
NOTE 8 For single die package (SDP) or 3DS, CAI is used to indicate Command Address Inversion (ZQ1 is not applicable). However, for dual die package (DDP), CAI die pads are grounded inside the package, and ZQ1 pin is connected to the top die ZQ pad (Rank 1).

MO-210-AL (x4/x8)



MO-210-AN (x4/x8) with support balls



O Populated ball
+ Ball not populated

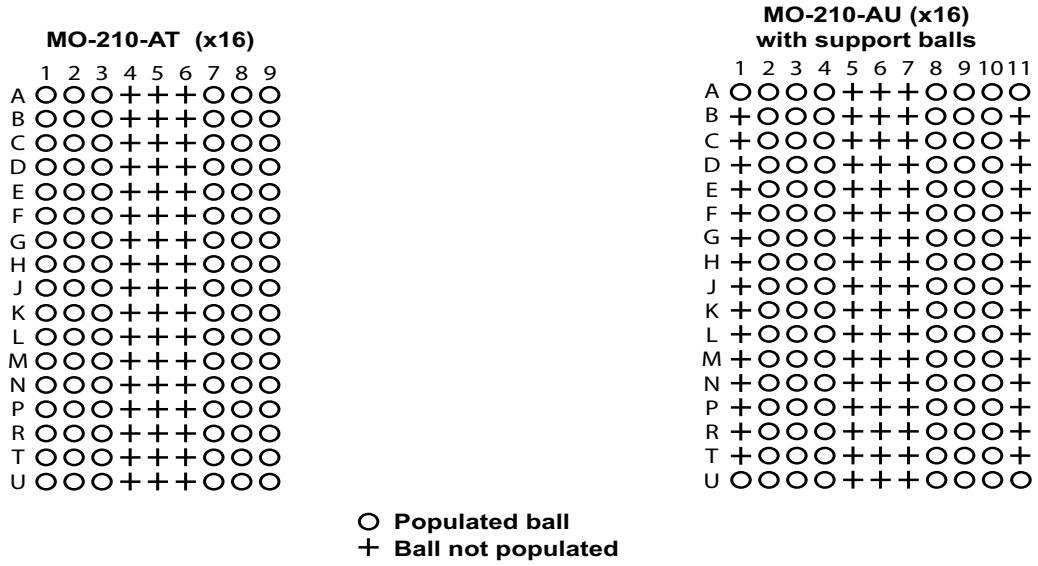
NOTE(s):
1. Additional columns and rows of inactive balls in MO-210 Terminal Pattern AN (x4/x8) with support balls are for mechanical support only, and should not be tied to either electrically high or low.
2. Some of the additional support balls can be selectively populated under the supplier's discretion. Refer to supplier's datasheet.

Figure 1 — DDR5 Ball Assignments for the x4/8 Component

2.5 DDR5 SDRAM x16 Ballout using MO-210

Table 2 — DDR5 SDRAM x16 Ballout using MO-210

AU	1	2	3	4	5	6	7	8	9	10	11	
AT		1	2	3	4	5	6	7	8	9		
A	DNU	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	DNU	A
B		VDD	VDDQ	DQU2				DQU3	VDDQ	VDD		B
C		VSS	DQU0	DQSU_t				DMU_n	DQU1	VSS		C
D		VDDQ	VSS	DQSU_c				RFU	VSS	VDDQ		D
E		VDD	DQU4	DQU6				DQU7	DQU5	VDD		E
F		VDD	VDDQ	DQL2				DQL3	VDDQ	VDD		F
G		VSS	DQL0	DQSL_t				DML_n	DQL1	VSS		G
H		VDDQ	VSS	DQSL_c				RFU	VSS	VDDQ		H
J		VDD	DQL4	DQL6				DQL7	DQL5	VDD		J
K		VSS	VDDQ	VSS				VSS	VDDQ	VSS		K
L		CA_ODT	MIR	VDD				CK_t	VDDQ	TEN		L
M		ALERT_n	VSS	CS_n				CK_c	VSS	VDD		M
N		VDDQ	CA4	CA0				CA1	CA5	VDDQ		N
P		VDD	CA6	CA2				CA3	CA7	VDD		P
R		VDDQ	VSS	CA8				CA9	VSS	VDDQ		R
T		CAI	CA10	CA12				CA13	CA11	RESET_n		T
U	DNU	VDD	VSS	VDD				VPP	VSS	VDD	DNU	U



NOTE(s):
1. Additional columns and rows of inactive balls in MO-210 Terminal Pattern AU (x16) with support balls are for mechanical support only, and should not be tied to either electrically high or low.
2. Some of the additional support balls can be selectively populated under the supplier's discretion. Refer to supplier's datasheet.

Figure 2 — DDR5 Ball Assignments for the x16 Component

2.6 Pinout Description

Table 3 — Pinout Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CS_n, (CS1_)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down modes.
DM_n, DMU_n, DML_n	Input	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1. DM is not supported for x4 device.
CA [13:0]	Input	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are Multi-Cycle, the pins may not be interchanged between devices on the same bus.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DDQ}.
DQ	Input / Output	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via MR5:OP[4]=1, the DRAM shall enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via MR5:OP[4]=0, DM_n/TDQS_t shall provide the data mask function depending on MR5:OP[5]; TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via MR5:OP[4]=0.
ALERT_n	Input/Output	Alert: If a CRC error is detected, ALERT_n goes LOW for a time interval and goes back HIGH. During Connectivity Test mode, this pin works as an input. Optional use of this signal is dependent on the system. If the ALERT_n is not used, the ALERT_n pin must be pulled to VDDQ on the board.
TEN	Input	Connectivity Test Mode Enable: Required on x4, x8 & x16 devices. HIGH in this pin shall enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of V_{DDQ}. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
MIR	Input	Mirror: Used to inform SDRAM device that it is being configured for Mirrored mode vs. Standard mode. With the MIR pin connected (strapped) to VDDQ, the SDRAM internally swaps even numbered CA with the next higher odd number CA. Normally the MIR pin must be tied to VSS if no CA mirror is required. Mirror pair examples: CA2 with CA3 (not CA1) CA4 with CA5 (not CA3). Note that the CA[13] function is only relevant for certain densities (including stacking) of DRAM component. In the case that CA[13] is not used, its ball location, considering whether MIR is used or not, should be connected (Strapped) to VDDQ. No active signaling requirements defined.
CAI	Input	Command & Address Inversion: With the CAI pin connected (strapped) to VDDQ, DRAM internally inverts the logic level present on all the CA signals. Normally the CAI pin must be connected to VSS if no CA inversion is required. No active signaling requirements defined.

Table 3 — Pinout Description (cont'd)

Symbol	Type	Function
CA_ODT	Input	ODT for Command and Address. Apply Group A settings if the pin is connected (strapped) to VSS and apply Group B settings if the pin is connected (strapped) to V_{DDQ}. No active signalling requirements defined.
LBDQ	Output	Loopback Data Output: The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].
LBDQS	Output	Loopback Data Strobe: This is a single ended strobe with the Rising edge-aligned with Loopback data edge, falling edge aligned with data center. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].
RFU	Input/Output	Reserved for future use
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.1 V
VDD	Supply	Power Supply: 1.1 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 1.8 V
ZQ, (ZQ1)	Reference	Reference Pin for ZQ calibration. This ball is tied to an external 240 ohm resistor(RZQ), which is tied to V_{SS}.

2.7 DDR5 SDRAM Addressing

Table 4 — 8 Gb Addressing Table

Configuration		2 Gb x4	1 Gb x8	512 Mb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0	BA0	BA0
	# BG / # Banks per BG / # Banks	8 / 2 / 16	8 / 2 / 16	4 / 2 / 8
Row Address		R0~R15	R0~R15	R0~R15
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~3 / 16H	CID0~3 / 16H	CID0~3 / 16H

Table 5 — 16 Gb Addressing Table

Configuration		4 Gb x4	2 Gb x8	1 Gb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
Row Address		R0~R15	R0~R15	R0~R15
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~3 / 16H	CID0~3 / 16H	CID0~3 / 16H

Table 6 — 24 Gb Addressing Table

Configuration		6 Gb x4	3 Gb x8	1.5 Gb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
Row Address		R0~R16	R0~ R16	R0~R16
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~3 / 16H	CID0~3 / 16H	CID0~3 / 16H

NOTE 1 For non-binary memory densities, a quarter of the row address space is invalid. When the MSB address bit is “HIGH”, the MSB-1 address bit shall be “LOW”.

Table 7 — 32 Gb Addressing Table

Configuration		8 Gb x4	4 Gb x8	2 Gb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
Row Address		R0~R16	R0~R16	R0~R16
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~3 / 16H	CID0~3 / 16H	CID0~3 / 16H

2.7 DDR5 SDRAM Addressing (cont'd)

Table 8 — 64 Gb Addressing Table

Configuration		16 Gb x4	8 Gb x8	4 Gb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
Row Address		R0~R17	R0~R17	R0~R17
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~2 / 8H	CID0~2 / 8H	CID0~2 / 8H

3 Functional Description

3.1 Simplified State Diagram

This Simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

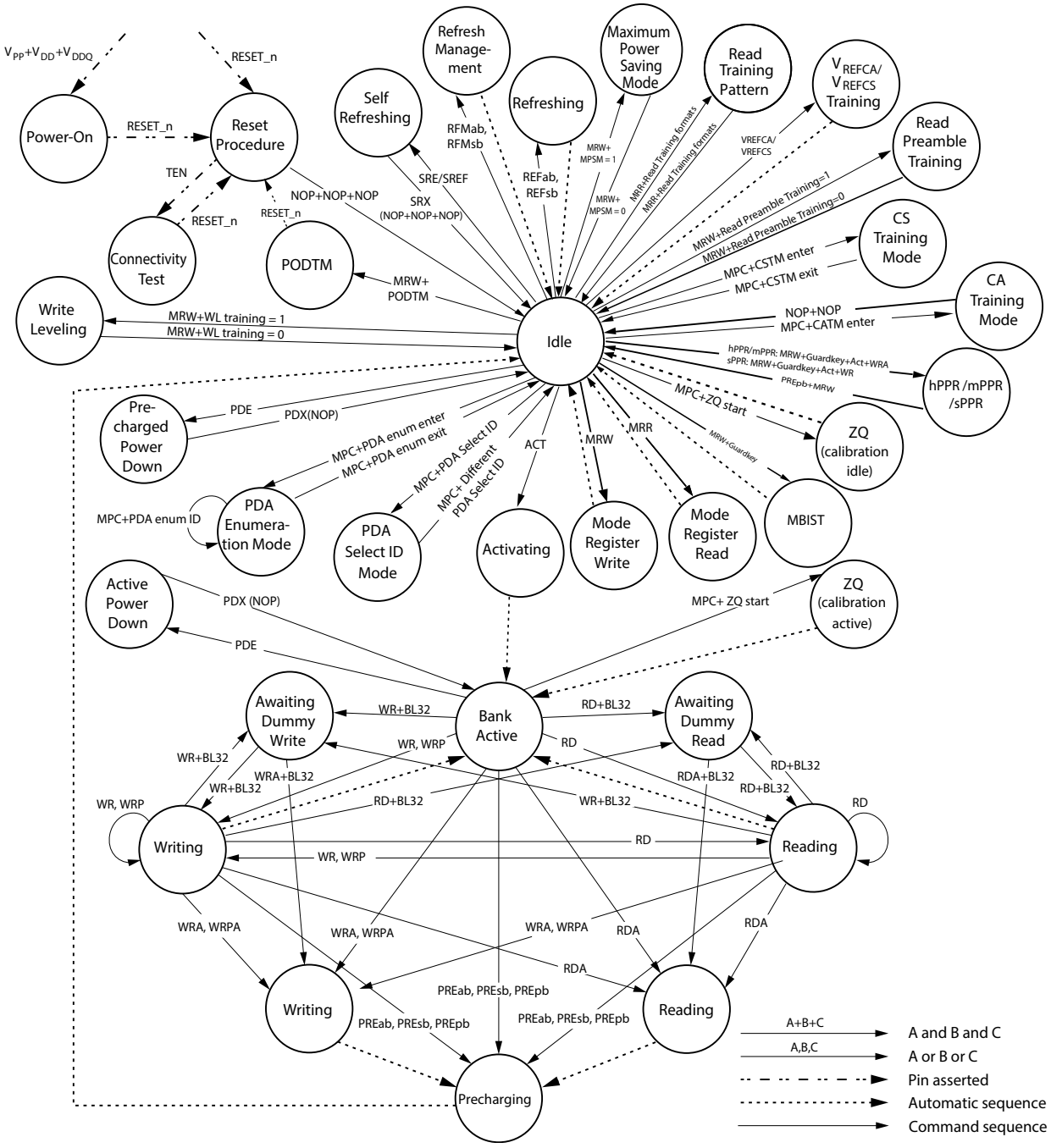


Figure 3 — Simplified State Diagram

3.2 Basic Functionality

The DDR5 SDRAM is a high-speed dynamic random-access memory. To ease transition from DDR4 to DDR5, the introductory density (8 Gb) shall be internally configured as 16-bank, 8 bank group with 2 banks for each bank group for x4/x8 and 8-bank, 4 bank group with 2 banks for each bankgroup for x16 DRAM. When the industry transitions to higher densities (=>16 Gb), it doubles the bank resources and internally be configured as 32-bank, 8 bank group with 4 banks for each bank group for x4/x8 and 16-bank, 4-bank group with 4 banks for each bankgroup for x16 DRAM.

The DDR5 SDRAM uses a 16n prefetch architecture to achieve high-speed operation. The 16n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR5 SDRAM consists of a single 16n-bit wide, eight clock data transfer at the internal DRAM core and sixteen corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR5 SDRAM are burst oriented, start at a selected location, and continue for a burst length of sixteen or a ‘chopped’ burst of eight in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered with the ACTIVATE Command are used to select the bank and row to be activated (i.e. in a 16Gb part, BG0-BG2 in a x4/8 and BG0-BG1 in x16 select the bankgroup; BA0-BA1 select the bank; R0-R17 select the row; refer to “DDR5 SDRAM Addressing” for specific requirements). The address bits registered with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (CA10=L), and select BC8 on-the-fly (OTF), fixed BL16, fixed BL32 (optional), or BL32 OTF (optional) mode if enabled in the mode register.

Prior to normal operation, the DDR5 SDRAM must be powered up and initialized in a predefined manner.

The following clauses provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

3.3 RESET and Initialization Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values for the following MR settings need to be defined.

Table 9 — MR Default Settings

Item	Mode Register	Default Setting	Description
Burst Length	MR0 OP[1:0]	00_B	BL16
Read Latency	MR0 OP[6:2]	00010_B	RL(CL) = 26 @3200
Write Latency	n/a	WL=RL-2 (CWL=CL-2)	Fixed based on RL (CL)
Write Recovery (tWR)	MR6 OP[3:0]	0000_B	WR = 48nCK @3200 or 30ns
Read to Precharge Delay (tRTP)	MR6 OP[7:4]	0000_B	tRTP=12nCK @3200 or 7.5ns
VrefDQ Value	MR10	$0010\ 1101_B$	VREF(DQ) Range: 75% of V_{DDQ}
VrefCA Value	MR11	$0010\ 1101_B$	VREF(CA) Range: 75% of V_{DDQ}
VrefCS Value	MR12	0010 1101B	VREF(CS) Range: 75% of VDDQ
ECS Error Threshold Count (ETC)	MR15	011B	256
Post Package Repair	MR23 OP[1:0]	00B	hPPR and sPPR Disabled
CK ODT	MR32 OP[2:0]	CK ODT is based on strap value	Group A= RTT_OFF=000B Group B= 40 Ohms=111B
CS ODT	MR32 OP[5:3]	CS ODT is based on strap value	Group A= RTT_OFF=000B Group B= 40 Ohms=111B
CA ODT	MR33 OP[2:0]	CA ODT is based on strap value	Group A= RTT_OFF=000B Group B= 80 Ohms=100B
DQS_RTT_PARK	MR33 OP[5:3]	000B	RTT OFF
RTT_PARK	MR34 OP[2:0]	000B	RTT OFF
RTT_WR	MR34 OP[5:3]	001B	240 Ohm
RTT_NOM_WR	MR35 OP[2:0]	011B	80 Ohm
RTT_NOM_RD	MR35 OP[5:3]	011B	80 Ohm
RTT Loopback	MR36 OP[2:0]	000B	RTT OFF
RFM RAAIMT	MR58 OP[4:1]	vendor specific	vendor specific
RFM RAAMMT	MR58 OP[7:5]	vendor specific	vendor specific
RFM RAA Counter	MR59 OP[7:6]	vendor specific	vendor specific

3.3.1 Power-up Initialization Sequence

The following sequence shall be used to power up the DDR5 device. Unless specified otherwise, these steps are mandatory.

1. While applying power (after Ta), RESET_n is recommended to be LOW (≤0.2 x VDDQ) and all other inputs may be undefined. The device outputs remain disabled while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 10 VPP shall ramp at the same time or earlier than VDD.

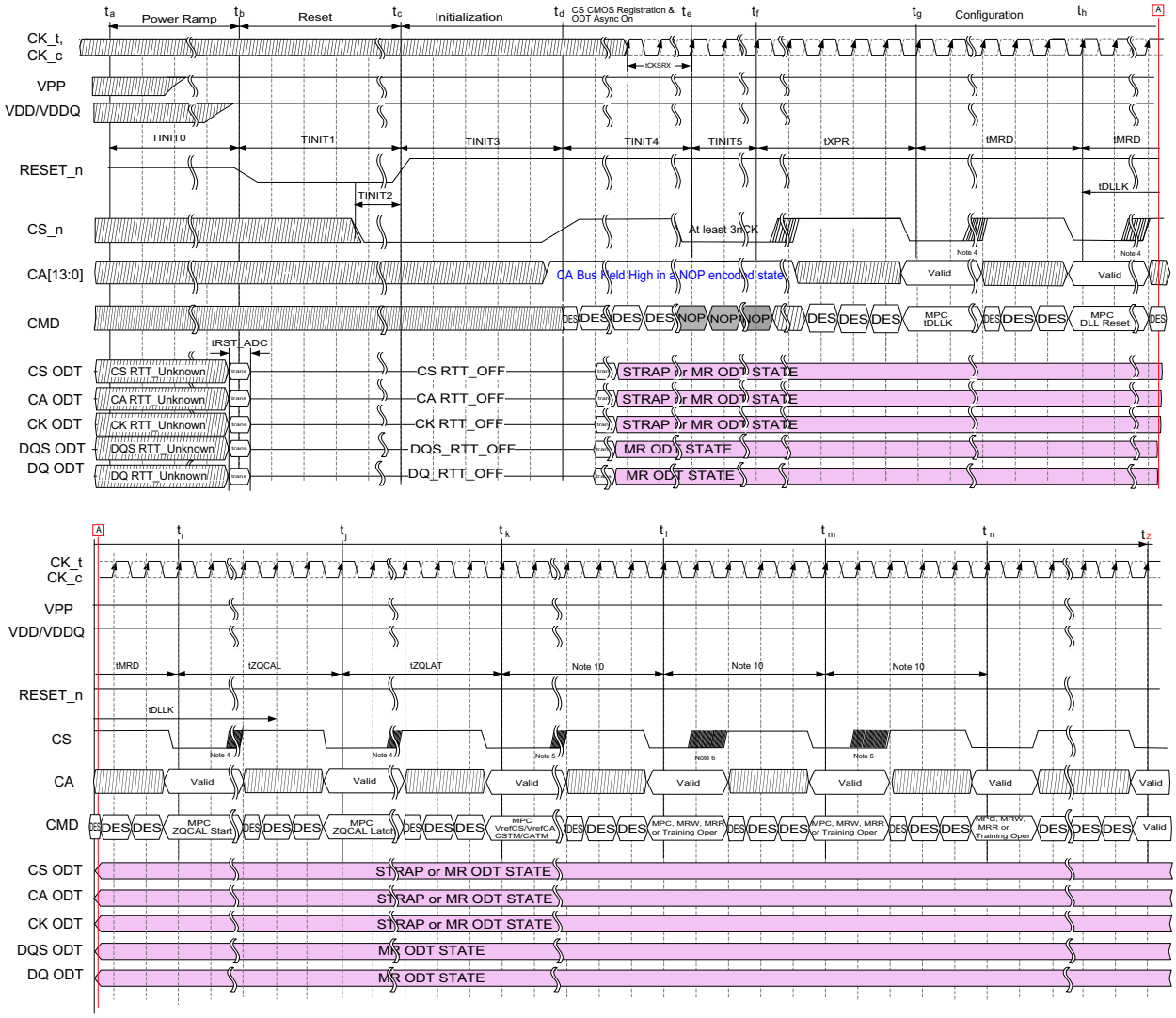
Table 10 — Voltage Ramp Conditions

After	Application Conditions
Ta is reached	VPP shall be greater than VDD
NOTE 1 Ta is the point when any power supply first reaches 300 mV NOTE 2 Voltage ramp conditions in the table above apply between (Ta) and Power-off (controlled or uncontrolled). NOTE 3 Tb is the point at which all supply and reference voltages are within their defined ranges. NOTE 4 Power ramp duration (Tb-Ta) shall not exceed tINIT0.	

2. Following the completion of the voltage ramp (Tb), RESET_n shall be maintained LOW. DQ, DQS_t, DQS_c, voltage levels shall be between VSS and VDDQ to avoid latch-up. CS_n, CK_t, CK_c and CA input levels shall be between VSS and VDDQ to avoid latch-up.

3. Beginning at Tb, RESET_n shall be maintained LOW for a minimum of tINIT1 (Tb to Tc), after which RESET_n may be de-asserted to HIGH (Tc). At least tINIT2 before RESET_n de-assertion, CS_n is required to be set LOW. All other input signals are “Don’t Care”. The DRAM shall support the ability for RESET_n to be held indefinitely.

3.3.1 Power-up Initialization Sequence (cont'd)



NOTES:
1. From time point (Ta) until (Tb), RTT_OFF may not be guaranteed due to the limitation for the DRAM to control the RTT status during the Power Ramp period.
2. From time point (Td) until (Te), the command/address (CA) bus shall be held high in a NOP encoded state.
3. From time point (Te) until (Tf), NOP commands shall be applied on the command/address (CA) bus.
4. From time point (Tf) until (Tk), DES commands must be applied between legal commands (MRR, MRW, MPC, VREFCS & VREFCA). MRR and MRW command, while legal, may not execute properly until CS and CA training routines are completed.
5. Prior to ZQcal completion at (Tk), MPC commands shall be Multi-Cycle as described in the MPC command Timings section.
6. From time point (Tk) until (Tl) all MPC, VREFCS and VREFCA commands prior to CS and CA training successfully completing, shall be Multi-Cycle (MR2:OP[4]=0) as described in the MPC, VREFCS, and VREFCA timing sections.
7. At time point (Tl), with successful completion of CS and CA training, an MRW command setting MR2:OP[4] =1 is recommended and allows for MPC,VREFCS, VREFCA commands to be single-cycle, improving training duration.
8. From time point (Tk) until (Tz), DES commands shall be applied between legal commands (MRR, MRW, MPC, VREFCS & VREFCA).
9. Starting at Tl, MRW Commands shall be issued to all Mode Registers that require defined settings.
10. Default ODT tolerances are wider prior to ZQ calibration.
11, All MPC/MRW/MRR to MPC/MRW/MRR commands shall meet the timing restrictions required.
12. Between (Tk to Tz), the SRX/NOP Clock-Sync feature can be enabled through an MRW command by programming MR13:OP[5]=1. When it is enabled, after CSTM/CATM prior to DCA training, host shall issue an SRE/SRX pair to ensure that the Clock-Sync is in effect during DCA training. It is also applied for CS Geardown Initialization sequence (for example, after Power-Up Initialization, CSTM, MPC (CS Geardown enable), Sync Pulse, CATM, MRW (SRX/NOP Clock-Sync enable), then host shall issue an SRE/SRX pair). Host (including RCD and Clock Driver) is responsible to ensure the same phases of the system clock all the time during DCA training.

Figure 4 — RESET_n and Initialization Sequence at Power-on Ramping

4. After RESET_n is de-asserted (Tc), wait at least tINIT3 before driving CS_n high.

3.3.1 Power-up Initialization Sequence (cont'd)

5. After setting CS_n high (Td), wait a minimum of tINIT4 to allow the DRAM CMOS based receiver to register the exit and allow the CS_n, CK, CA, DQ and DQS ODT to go to the defined strap or MRS state (Te). Clock (CK_t, CK_c) is required to be started and stabilized for tCKSRX before exit of tINIT4 (Te). Upon the completion of Te, all ODT states (CA, CS_n, CK, DQ and DQS ODT) should be valid and the DRAM's CS_n receiver should no longer be in its CMOS based mode. ODT termination states will be uncalibrated until completion of ZQcal at (Tj)

6. Upon (Te), NOP commands shall be issued for a minimum of tINIT5 to conclude exit of initialization process and start tXPR timer at (Tf). The system shall wait at least tXPR before issuing any legal configuration commands (Tg). During early configuration steps (Tg to Tk), only MRR, MRW, MPC, VREFCS and VREFCA commands are legal. MRR and MRW command, while legal, may not execute properly until CS and CA training routines are completed.

7. Between (Tg to Tj), the following initial configuration modes shall be completed prior to other training modes:
   - MPC for setting MR13 (tCCD_L*/tDLLK) shall be issued before the MPC command to reset the DLL.
   - MPC to execute DLL RESET shall be issued before ZQCal Start
   - MPC to execute ZQCal Start followed by ZQCal Latch shall be issued before any other training modes such as VrefCS, VrefCA, CS and CA Training.

8. Between (Tk to Tz), any number of legal configuration commands are allowed. Many training based commands are optional and may be done at the system architect's discretion and may vary depending on the systems, though proper setting of certain registers, such as those related to Write Leveling Training, is required. The host shall follow Multi-Cycle MPC timing requirements in cases where the alignment between CS_n, CA, and CK is unknown, (ie., prior to successfully completing VREFCS, VREFCA, CS, and CA training commands or host provided successful training solutions). MRW and MRR commands can be used once the alignment between CS_n, CA and CK are known. Single-cycle CS_n assertion are allowed after setting MR2:OP[4]=1.

9. Between (Tk to Tz), the SRX/NOP Clock-Sync feature can be enabled through an MRW command by programming MR13:OP[5]=1. When it is enabled, after CSTM/CATM prior to DCA training, host shall issue an SRE/SRX pair to ensure that the Clock-Sync is in effect during DCA training. It is also applied for CS Geardown Init sequence (for example, after PowerUp Initialization, CSTM, MPC (CS Geardown enable), Sync Pulse, CATM, MRW (SRX/NOP Clock-Sync enable), then host shall issue an SRE/SRX pair). Host (including RCD and Clock Driver) is responsible to ensure the same phases of the system clock all the time during DCA training to make the DCA training effective with the consistent phases of system and DRAM internal clocks.

10. After (Tz), and the completion of any training or calibration timing parameters (i.e. tZQLAT is satisfied), the DDR5 device is ready for normal operation and is able to accept any valid command. Any additional mode registers that have not previously been set up for normal operation should be written at this time. If host use writeback suppression mode, it should be set after the initial write process to prevent aliasing to 2-bit errors.

11. After all mode registers have been programmed for normal operation, optional MBIST mode can be entered by writing MR23:OP[4] to HIGH, followed by subsequent MR24 PPR guard keys, then DRAM will drive ALERT_n to LOW for a maximum of tSELFTEST time. DRAM will drive ALERT_n to HIGH to indicate that this operation is completed. After ALERT_n is driven high, the DRAM is immediately ready to receive valid commands. The MBIST/mPPR transparency status shall subsequently be checked in MR22:OP[2:0] in order to determine whether mPPR should be performed. Please refer to Ch. 4.30 MBIST/mPPR for more detailed operation procedures.

Table 11 — Initialization Timing Parameters

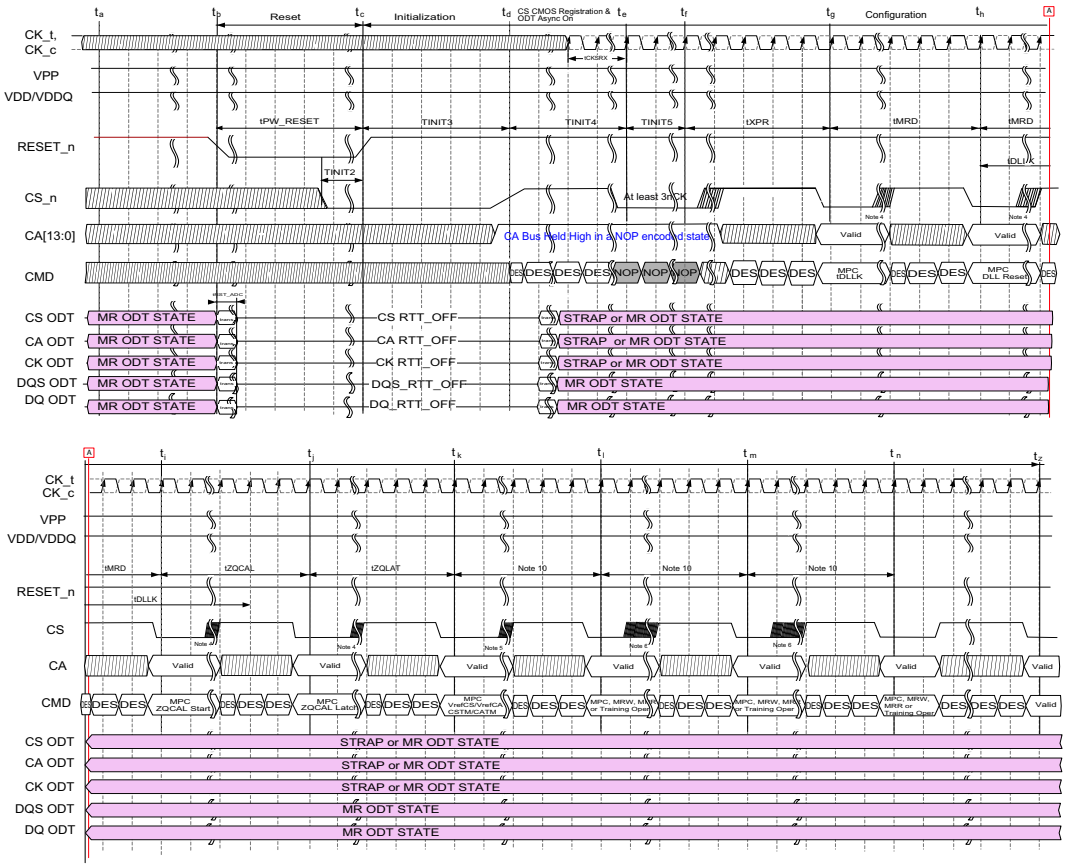
Parameter	Symbol	Value		Units	Note(s)
		MIN	MAX		
Maximum voltage-ramp time	tINIT0	-	20	ms	
Minimum RESET_n LOW time after completion of voltage ramp	tINIT1	200		µs	
Minimum CS_n LOW time before RESET_n HIGH	tINIT2	10	-	ns	
Minimum CS_n LOW time after RESET_n HIGH	tINIT3	4	-	ms	
Minimum time for DRAM to register EXIT on CS_n with CMOS.	tINIT4	2	-	µs	
Minimum cycles required after CS_n HIGH	tINIT5	3	-	*n*CK	1
Minimum time from Exit Reset to first valid Configuration Command	tXPR	tXS	-	ns	
Minimum stable clock time	tCKSRX	SEE Self Refresh Timing Table			

NOTE 1 Min number of NOP commands issued after CS_n High (tINIT4).

3.3.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization as shown in Figure 5.

1. Assert RESET_n below 0.2 x VDDQ anytime when reset is needed. RESET_n needs to be maintained for a minimum of tPW_RESET. CS_n shall be pulled LOW at least tINIT2 before de-asserting RESET_n.
2. Repeat steps 4 to 11 in Section 3.3.1



NOTES:

1. From time point (Td) until (Te), the command/address (CA) bus shall be held high in a NOP encoded state.
2. From time point (Te) until (Tf), NOP commands shall be applied on the command/address (CA) bus.
3. From time point (Tf) until (Tk), DES commands shall be applied between legal commands (MRR, MRW, MPC, VREFCS & VREFCA). MRR and MRW command while legal, may not execute properly until CS and CA training routines are completed.
4. Prior to ZQcal completion at (Tk), MPC commands shall be Multi-Cycle as described in the MPC command Timings section.
5. From time point (Tk) until (Tl) all MPC, VREFCS and VREFCA commands prior to CS and CA training successfully completing, shall be Multi-Cycle (MR2:OP[4]=0) as described in the MPC, VREFCS, and VREFCA timing sections.
6. At time point (Tl), with successful completion of CS and CA training, an MRW command setting MR2:OP[4] =1 is recommended and allows for MPC, VREFCS, VREFCA commands to be single-cycle, improving training duration.
7. From time point (Tk) until (Tz), DES commands shall be applied between legal commands (MRR, MRW, MPC, VREFCS & VREFCA).
8. Starting at Tl, MRW Commands shall be issued to all Mode Registers that require defined settings.
9. Default ODT tolerances are wider prior to ZQ calibration.
10. All MPC/MRW/MRR to MPC/MRW/MRR commands shall meet the timing restrictions required.
11. MRR is legal after DLL_reset.
12. Between (Tk to Tz), the SRX/NOP Clock-Sync feature can be enabled through an MRW command by programming MR13:OP[5]=1. When it is enabled, after CSTM/CATM prior to DCA training, host shall issue an SRE/SRX pair to ensure that the Clock-Sync is in effect during DCA training. It is also applied for CS Geardown Initialization sequence (for example, after Power-Up Initialization, CSTM, MPC (CS Geardown enable), Sync Pulse, CATM, MRW (SRX/NOP Clock-Sync enable), then host shall issue an SRE/SRX pair). Host (including RCD and Clock Driver) is responsible to ensure the same phases of the system clock all the time during DCA training.

Figure 5 — Reset Procedure at Stable Power

3.3.2 Reset Initialization with Stable Power (cont'd)

Table 12 — Reset Timing Parameters

Parameter	Symbol	Value		Units	Note(s)
		Min	Max		
Minimum RESET_n low time for Reset Initialization with stable power	tPW_RESET	1	-	µS	
Maximum time after RESET_n assertion to ODT off	tRST_ADC	-	50	nS	

3.3.3 Input Voltage Power-up and Power-Down Sequence

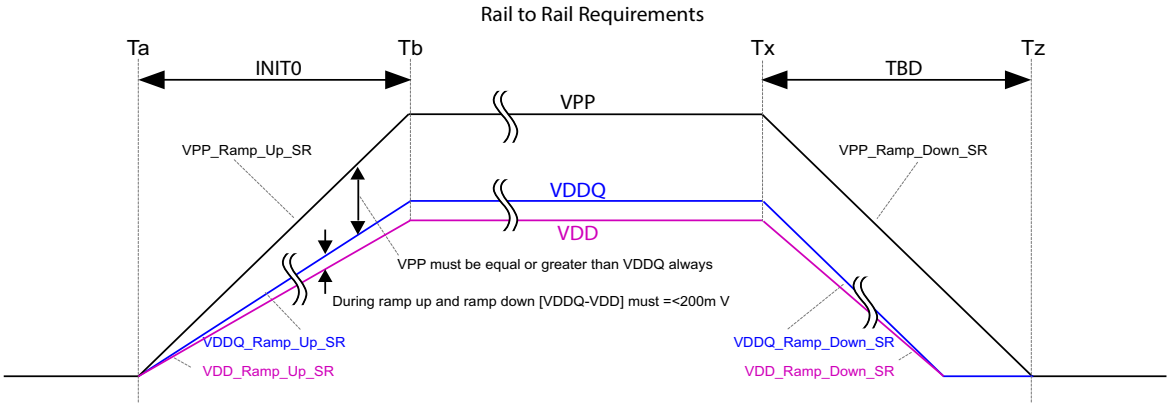


Figure 6 — Requirement for Voltage Ramp Control

Table 13 — Input Voltage Slew Rates and Power Ramp Down Time

Description	Symbol	Min	Max	Units	Notes
VPP Rail	VPP_Ramp_Up_SR	0.2	5	V/ms	1,2,3,4,5
	VPP_Ramp_Down_SR	0.1	4.5	V/ms	
VDD Rail	VDD_Ramp_Up_SR	0.1	4.5	V/ms	
	VDD_Ramp_Down_SR	0.1	4.5	V/ms	
VDDQ Rail	VDDQ_Ramp_Up_SR	0.1	4.5	V/ms	
	VDDQ_Ramp_Down_SR	0.1	4.5	V/ms	
Power Ramp Down Time	tPRD	-	19.08	ms	

NOTE 1 Both VDD and VPP supply measurements made between 10% and 90% nominal voltage
NOTE 2 1Mhz bandwidth limited measurement
NOTE 3 VPP shall be equal to or greater than VDD/VDDQ at all times.
NOTE 4 During ramp up and ramp down [VDDQ-VDD] must be equal or less than 200 mV.
NOTE 5 After tINIT0, all supplies shall be within their specified tolerance, as defined in the DC Operating Tables.

3.4 Mode Register Definition

3.4.1 Mode Register Read (MRR)

The Mode Register Read (MRR) command is used to read configuration and status data from the DDR5-SDRAM registers. The MRR command is initiated with CS_n and CA[13:0] in the proper state as defined by the Command Truth Table. The mode register address operands (MA[7:0]) allow the user to select one of 256 registers. The mode register contents are available on the second 8 UI's of the burst and are repeated across all DQ's after the CL following the MRR command. To avoid a potentially worst-case pattern, every odd DQ bit (represented with !) shall have its contents inverted. Data in the burst (BL0-7) shall be either "0" or "1", with "1" indicating that the content of the later UI's (BL8-15) are inverted.

MRR commands require all banks to be idle on the DRAM. For 3DS, MRR commands require all banks to be idle on all logical ranks, The 3DS base die (CID[3:0]=0x0) is the targeted logical rank for most Mode Register Reads, however the CID setting of MR14:OP[3:0] designates the targeted logical rank for MRR commands to MR14-MR20, MR22 and MR54-MR57, and still requires all banks to be idle not only on the targeted logical rank but also on all other logical ranks.

DQS is toggled for the duration of the MRR burst. The MRR has a command burst length 16 regardless of the MR0 setting, the training mode or the mode register address. MRR termination control and ODT timings are the same as for the Read command. The MRR operation must not be interrupted. Non-Target ODT encoding is available for MRR, just like a normal Read. MRR NT ODT termination control and ODT timings are the same as for the Read NT command.

In the case that CRC is enabled, MRR's output will come with BL18 (BL16 plus 2 CRC-bit), but the host has the option to consider the 17th and 18th bits "don't care" for MRR handling. Regardless on if the host uses the 17th and 18th bits, while CRC is enabled, the strobe needs to toggle for BL18.

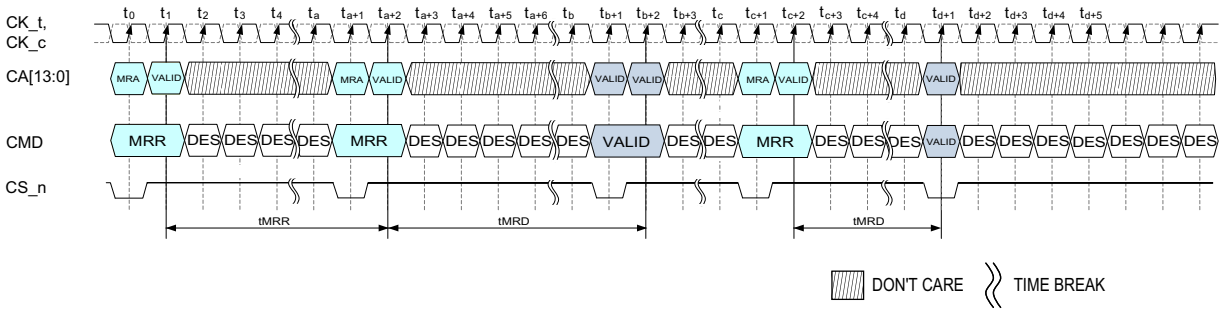


Figure 7 — Mode Register Read Timing

Table 14 — DQ Output Mapping for x4 Device

BL	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
NOTE 1 The read pre-amble and post-amble of MRR are same as normal read.									

3.4.1 Mode Register Read (MRR) (cont'd)

Table 15 — DQ Output Mapping for x8 Device

BL	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

NOTE 1 The read pre-amble and post-amble of MRR are same as normal read.

Table 16 — DQ Output Mapping for x16 Device (OSC Count - MR46 and MR47 only)

BL	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ8	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ9	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ10	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ11	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ12	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ13	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ14	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ15	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

NOTE 1 The read pre-amble and post-amble of MRR are same as normal read.
NOTE 2 Output map excludes per bit DFE, DCA and VrefDQ mode registers (MR103 through MR255)

3.4.1 Mode Register Read (MRR) (cont'd)

Table 17 — DQ Output Mapping for x16 Device (DFE Registers Excluded)

BL	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ8	Don't Care								
DQ9									
DQ10									
DQ11									
DQ12									
DQ13									
DQ14									
DQ15									

NOTE 1 The read pre-amble and post-amble of MRR are same as normal read.
NOTE 2 Output of mode register data is only duplicated and inverted across the first 8 bits of a x16 device.
NOTE 3 Output map excludes per bit DFE, DCA and VrefDQ mode registers (MR103 through MR255)

Table 18 — DQ Output Mapping for x16 Device (DFE Lower Byte - DQ[0:7], DML)

BL	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ8	Don't Care								
DQ9									
DQ10									
DQ11									
DQ12									
DQ13									
DQ14									
DQ15									

NOTE 1 The read pre-amble and post-amble of MRR are same as normal read.
NOTE 2 Output of mode register data is only duplicated and inverted across the first 8 bits of a x16 device when reading from a DFE register associated with a lower byte DQ or DML.
NOTE 3 Output map is ONLY for per bit DFE, DCA and VrefDQ mode registers (MR103 through MR255)

3.4.1 Mode Register Read (MRR) (cont'd)

Table 19 — DQ Output Mappingfor x16 Device (DFE Upper Byte - DQ[15:8], DMU)

BL	0-7	8	9	10	11	12	13	14	15
DQ0	Don't Care								
DQ1									
DQ2									
DQ3									
DQ4									
DQ5									
DQ6									
DQ7									
DQ8	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ9	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ10	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ11	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ12	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ13	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ14	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ15	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

NOTE 1 The read pre-amble and post-amble of MRR are same as normal read.
NOTE 2 Output of mode register data is only duplicated and inverted across the last 8 bits of a x16 device when reading from a DFE register associated with an upper byte DQ or DMU.
NOTE 3 Output map is ONLY for per bit DFE, DCA and VrefDQ mode registers (MR103 through MR255)

3.4.2 Mode Register WRITE (MRW)

The Mode Register Write (MRW) command is used to write configuration data to the mode registers. The MRW command is initiated with CS_n and CA[13:0] in the proper state as defined by the Command Truth Table. The mode register address and the data written to the mode registers is contained in CA[13:0] according to the Command Truth Table. The MRW command period is defined by tMRW. Mode Register Writes to read-only registers have no impact on the functionality of the device.

MRW commands require all banks to be idle on the DRAM. For 3DS, MRW commands are broadcast across all logical ranks,requiring all banks to be idle on all logical ranks. For 3DS, MBIST Enable (MR23:OP[4]=1) is only enabled on the target logical rank designated by CID[3:0] and programmed by MRW via MR14:OP[3:0], but still requires all banks to be idle on all logical ranks.

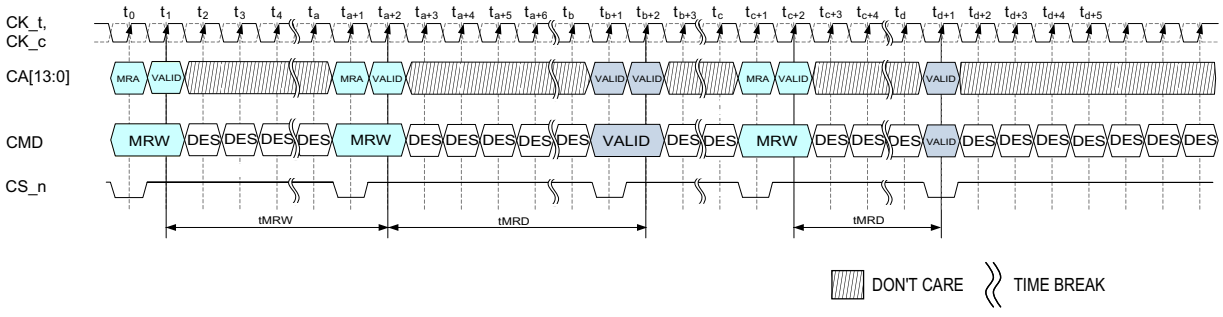


Figure 8 — Mode Register Write Timing

3.4.3 DFE Mode Register Write Update Timing

This Mode Register update timing parameter applies for MR112 (MA[7:0]=70H) thru MR248 (MA[7:0]=F8H) - Mode Registers for DFE including DFE Gain Bias, DFE Tap-1, DFE Tap-2, DFE Tap-3, DFE Tap-4 mode registers

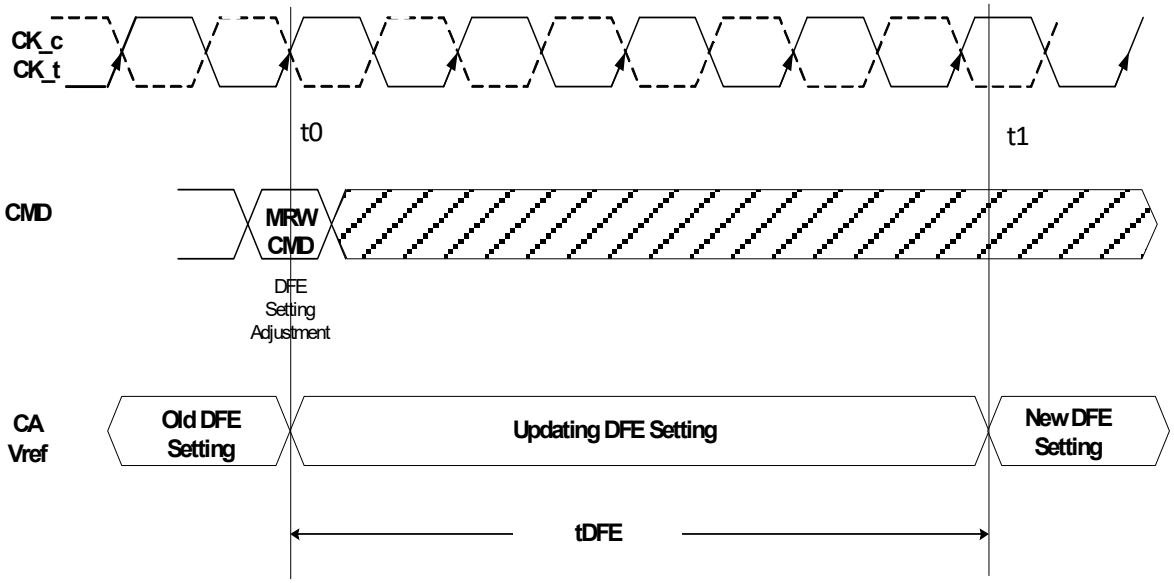


Figure 9 — DFE Update Setting

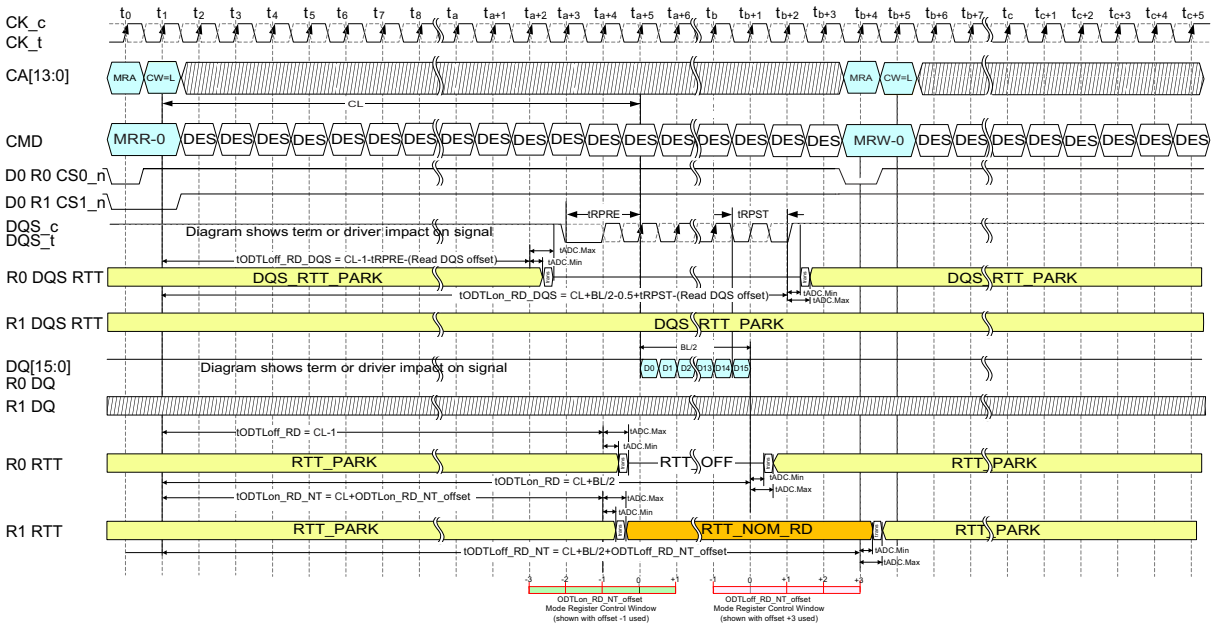
3.4.4 Mode Register Truth Tables and Timing Constraints

Table 20 — Mode Register Read/Write AC Timing

Parameter	Symbol	Min/Max	Value	Unit	Note
Mode Register Read command period	tMRR	Min	max(14ns, 16nCK)	nCK	1
Mode Register Read Pattern to Mode Register Read Pattern Command spacing	tMRR_p	Min	8	nCK	
Mode Register Write command period	tMRW	Min	max(5ns, 8nCK)	nCK	1
Mode Register Set command delay	tMRD	Min	max(14ns, 16nCK)	nCK	
DFE Mode Register Write Update Delay Time	tDFE	Min	80	ns	2

NOTE 1 MRR and MRW commands require all banks idle.
NOTE 2 This parameter applies only to MRW's to DFE registers and is defined as the settling time before a new DFE setting is active.

3.4.4 Mode Register Truth Tables and Timing Constraints (cont'd)



NOTES:

1. Example details ODTLoff_RD_Offset configured for -1, ODTLon_RD_Offset configured for 0, ODTLon_RD_NT_offset configured for -1, ODTLoff_RD_NT_offset configured for +3. Read DQS Offset programmed at 0.
2. Timing constraints for 1-cycle MPC/VrefCS/VrefCA commands are affected by ODTLoff_RD_NT_Offset the same as MRW in the diagram.
3. The tODTLoff_RD_NT minimum timing constraint begins when the MRR command is registered in the second cycle of the command, and ends on the first cycle of the MRW command. The MRW command will not be registered until the second cycle of the command, however the minimum timing spec shall be maintained as illustrated.

Figure 10 — Example MRR to MRW Timing Diagram for Same Physical Rank

3.4.4 Mode Register Truth Tables and Timing Constraints (cont'd)

Table 21 — Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)

Current State SDRAM	Command	Intermediate State SDRAM	Next State SDRAM
All Banks Idle	MRR	Mode Register Reading (All Banks Idle)	All Banks Idle
	MRW	Mode Register Writing (All Banks Idle)	All Banks Idle
NOTE 1 For 3DS, both MRR and MRW commands require all banks to be idle on all logical ranks			

Table 22 — MRR/MRW Timing Constraints: DQ ODT is Disable

From Command	To Command	Minimum Delay between "From Command" and "To Command"	Unit	Note
MRR	MRR	tMRR/tMRR_p	-	2,4
	MRW	CL+BL/2+max[1,ODTLoff_RD_NT_Offset]	tCK	2,3
	MPC	CL+BL/2+max[1,ODTLoff_RD_NT_Offset]	tCK	2,3
	VrefCA/VrefCS	CL+BL/2+max[1,ODTLoff_RD_NT_Offset]	tCK	2,3
	Any other valid command	tMRD	-	1,2
MRW	MRW	tMRW	-	
	Any other valid command	tMRD	-	
WRA	MRR	CWL + BL/2 + tWR + tRP	-	
	MRW	CWL + BL/2 + tWR + tRP	-	
RDA	MRR	tRTP + tRP		
	MRW	tRTP + tRP		
PRE	MRR	tRP	-	
	MRW	tRP	-	
REF	MRR	tRFC	-	
	MRW	tRFC	-	
NOTE 1 All data should be completed before entry into self refresh or power down. NOTE 2 MRR can refer to both Target ODT MRR and Non-Target ODT MRR NOTE 3 Minimum delay is 1 clock after the burst or until the ODT offset requirements for DQS/DQ are met. NOTE 4 During Read Training, MRR to MRR command spacing can be tMRR_p.				

3.4.4 Mode Register Truth Tables and Timing Constraints (cont'd)

Table 23 — MRR/MRW Timing Constraints: DQ ODT is Enable

From Command	To Command	Minimum Delay between "From Command" and "To Command"	Unit	Note
MRR	MRR	Same as ODT Disable Case	-	
	MRW		-	
	MPC		-	
	VrefCA/VrefCS		-	
	Any other valid command		-	
			-	
MRW	MRW	Same as ODT Disable Case	-	
	Any other valid command		-	
			-	
RDA	MRR	Same as ODT Disable Case	-	
	MRW		-	
WRA	MRR	Same as ODT Disable Case	-	
	MRW		-	
PRE	MRR	Same as ODT Disable Case	-	
	MRW		-	
REF	MRR	Same as ODT Disable Case	-	
	MRW		-	

3.5 Mode Registers

With DDR5, the utilization and programming method shall change from the traditional addressing scheme found in DDR3 and DDR4, and shall move to the method used by LPDDR, where the Mode Register Addresses (MRA) and Payload placed in Op Codes (OP) are all packeted in the command bus encoding method. Please refer to the Command Truth Table 30 for Mode Register Read (MRR) and Mode Register Write (MRW) command protocol.

For DDR5, the SDRAM shall support up to 8 MRA's, each with a byte-wide payload. Allowing for up to 256 byte-wide registers.

3.5.1 Mode Register Assignment and Definition in DDR5 SDRAM

Table 24 shows the mode registers for DDR5 SDRAM. Each bit in a register byte (MR#) is denoted as "R" if it can be read but not written, "W" if it can be written but reads shall always produce a ZERO for those specific bits, and "R/W" if it can be read and written. Additionally, a DRAM read-only bit combined with a Host write-only bit is denoted as a "SR/W" bit. This bit allows the DRAM to return a defined status during a read of that bit (SR = Status Read), independent of what the Host may have written to the bit.

A defined register byte (MR#), is any MR# that has at least one of the bits defined.

When the entire MR# is marked RFU, then it is considered undefined and all the bits from the DRAM shall be don't care for reads or writes. These undefined mode registers (completely empty bytes, not individual bits of an MR) may not be supported in the DRAM. When a defined register byte (MR#) contains an "RFU" bit, the host must write a ZERO for those specific bits and the DRAM does not guarantee any operation of those specific RFU bits. When the host issues an MRR to a defined register (MR#) that contains RFU bits in it, those specific bits shall always produce a ZERO.

For cases in which a mode register is specific to a particular device configuration (x16, x8, x4) and/or density (32Gb, 16Gb, 8Gb), the following rules shall be applied:

- When the DRAM is configured as a x4/x8, an entire MR# used only for a x16 shall be considered RFU. These bits are don't care for reads and writes, and they may be unsupported.
- When a bit field within a register is used by a different configuration or density than a given DRAM, the host may write/read programmed values to these fields, but DRAM operation will not be affected.

A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register
.

Table 24 — Mode Register Assignment in DDR5 SDRAM

MR#	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
0	RFU	CAS Latency (RL)					Burst Length	
1	PDA Select ID				PDA Enumerate ID			
2	Internal Write Timing	Reserved	Device 15 MPSM	CS Assertion Duration (MPC)	Max Power Saving Mode (MPSM)	2N Mode	Write Leveling Training	Read Preamble Training
3	Write Leveling Internal Cycle Alignment - Upper Byte				Write Leveling Internal Cycle Alignment - Lower Byte			
4	TUF	RFU	Wide Range (Optional)	Refresh tRFC Mode	Refresh Interval Rate Indicator	Minimum Refresh Rate		
5	Pull-Down Output Driver Impedance		DM Enable	TDQS Enable	PODTM Support	Pull-up Output Driver Impedance		Data Output Disable
6	tRTP				Write Recovery Time			

Table 24 — Mode Register Assignment in DDR5 SDRAM (cont'd)

MR#	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
7	RFU						(Optional) Write Leveling Internal +0.5tCK Alignment Offset - Upper Byte	(Optional) Write Leveling Internal +0.5tCK Alignment Offset - Lower Byte
8	Write Postamble Settings	Read Postam-ble Set-tings	RFU	Write Preamble Settings		Read Preamble Settings		
9	TM	RFU					x4 Writes	ECS Write-back
10	VrefDQ Calibration Value							
11	VrefCA Calibration Value							
12	VrefCS Calibration Value							
13	RFU				tCCD_L / tDLLK			
14	ECS Mode	Reset ECS Counter	Row Mode/Cod e Word Mode	RFU	CID3	CID2	CID1	CID0
15	x4 Writes	ECS Writeback	RFU		Automatic ECS in Self Refresh	ECS Error Threshold Count (ETC)		
16	Transparency - Row Address with Max Errors 1 - See MR for encoding details							
17	Transparency - Row Address with Max Errors 2 - See MR for encoding details							
18	Transparency - Row Address with Max Errors 3 - See MR for encoding details							
19	PASR	RFU	Transparency - Max Row Error Count - See MR for encoding details					
20	Transparency - Error Count (EC) - See MR for encoding details							
21	RFU					Rx DQS CTLE Control (Optional)		
22	Rx CS_n CTLE Contorl (Optional)		Rx CA CTLE Control (Optional)		Rx CTLE Support	MBIST/mPPR Transparency (Optional)		
23	RFU		RFU	MBIST (Optional)	mPPR (Optional)	sPPR		hPPR
24	PPR Guard Key							
25	RFU				Continu-ous Burst Mode	LFSR1 Pattern Option	LFSR0 Pattern Option	Read Training Pat-tern Format
26	Read Training Pattern Data0 / LFSR0 Seed							
27	Read Training Pattern Data1 / LFSR1 Seed							
28	Read Training Pattern Invert DQL7:0 (DQ7:0)							
29	Read Training Pattern Invert DQU7:0 (DQ15:8)							
30	LFSR Assignment DQL7/ DQU7	LFSR Assign-ment DQL6/ DQU6	LFSR Assign-ment DQL5/ DQU5	LFSR Assign-ment DQL4/ DQU4	LFSR Assign-ment DQL3/ DQU3	LFSR Assign-ment DQL2/ DQU2	LFSR Assignment DQL1/ DQU1	LFSR Assignment DQL0/ DQU0
31	Read Training Pattern Address							
32	RFU	CA_ODT Strap Value	CS ODT			CK ODT		
33	RFU		DQS_RTT_PARK			CA ODT		
34	RFU		RTT_WR			RTT_PARK		

Table 24 — Mode Register Assignment in DDR5 SDRAM (cont'd)

MR#	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
35	RFU		RTT_NOM_RD			RTT_NOM_WR		
36	RFU					RTT_Loopback		
37	RFU		ODTLoff_WR_offset			ODTLon_WR_offset		
38	RFU		ODTLoff_WR_NT_offset			ODTLon_WR_NT_offset		
39	RFU		ODTLoff_RD_NT_offset			ODTLon_RD_NT_offset		
40	RFU					Read DQS offset timing		
41	RFU							
42	DCA Training Assist Mode II (Optional)				DCA Training Assist Mode I		DCA Types Supported	
43	Sign Bit for OP[6:4]	DCA for IBCLK in 4-phase clocks			Sign Bit for OP[2:0]	DCA for single/two-phase clock(s) or QCLK in 4-phase clocks		
44	RFU				Sign Bit for QBCLK in 4-phase clocks	DCA for QBCLK in 4-phase clocks		
45	DQS Interval Timer Run Time							
46	DQS Oscillator Count - LSB							
47	DQS Oscillator Count - MSB							
48	Write Pattern Mode							
49	RFU							
50	RFU	RFU	Write CRC auto-disable status	Write CRC auto-disable enable	Write CRC error status	Write CRC enable upper nibble	Write CRC enable lower nibble	Read CRC enable
51	RFU	Write CRC Auto-Disable Threshold - See MR for encoding details						
52	RFU	Write CRC Auto-Disable Window - See MR for encoding details						
53	Loopback Output Mode	Loopback Select Phase		Loopback Output Select				
54	hPPR Resource BG1 Bank 3	hPPR Resource BG1 Bank 2	hPPR Resource BG1 Bank 1	hPPR Resource BG1 Bank 0	hPPR Resource BG0 Bank 3	hPPR Resource BG0 Bank 2	hPPR Resource BG0 Bank 1	hPPR Resource BG0 Bank 0
55	hPPR Resource BG3 Bank 3	hPPR Resource BG3 Bank 2	hPPR Resource BG3 Bank 1	hPPR Resource BG3 Bank 0	hPPR Resource BG2 Bank 3	hPPR Resource BG2 Bank 2	hPPR Resource BG2 Bank 1	hPPR Resource BG2 Bank 0
56	hPPR Resource BG5 Bank 3	hPPR Resource BG5 Bank 2	hPPR Resource BG5 Bank 1	hPPR Resource BG5 Bank 0	hPPR Resource BG4 Bank 3	hPPR Resource BG4 Bank 2	hPPR Resource BG4 Bank 1	hPPR Resource BG4 Bank 0
57	hPPR Resource BG7 Bank 3	hPPR Resource BG7 Bank 2	hPPR Resource BG7 Bank 1	hPPR Resource BG7 Bank 0	hPPR Resource BG6 Bank 3	hPPR Resource BG6 Bank 2	hPPR Resource BG6 Bank 1	hPPR Resource BG6 Bank 0
58	RAAMMT[2:0]			RAAIMT[3:0]				RFM Required
59	RFM RAA Counter		ARFM		BRC Support Level	Bounded Refresh Configuration		DRFM Enable
60	PASR Segment Mask							
61	RSVD			Package Output Driver Test Mode				
62	Vendor Specified							
63	DRAM Scratch Pad							
64	Reserved							
65	Serial Number 1							
66	Serial Number 2							
67	Serial Number 3							
68	Serial Number 4							
69	Serial Number 5							

Table 24 — Mode Register Assignment in DDR5 SDRAM (cont'd)

MR#	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
70	ALERT_n Verification	ALERT_n Verification Support (Optional)	Alert Back-Off Flag	RFU	Activation Counter Initialization Complete	Activation Counter Initialization	Per Row Activation Counting and Alert Back-Off Enable/Dis-able	Per Row Activation Counting and Alert Back-Off Support (Optional)
71	RFU	PRAC Testing Initialization	PRAC Testing Enable/Dis-able	PRAC Testing Support (Optional)	Adaptive Per Row Activation Counting		Min RFMab Commands during Recovery Period (ABO_RFM) and min ACT commands during Alert Back-Off Delay (ABO_Delay)	
72	RFU						Counter Address Report Flag	Counter Error Flag
73	8 bits of the row address							
74	8 bits of the row address							
75	RFU	3 bits of the bank group			2 bits of the bank address		2 bits of the row address	
76~102	RFU							
103	DQSL_t IBCLK Sign	RFU	DQSL_t DCA for IBCLK		DQSL_t QCLK Sign	RFU	DQSL_t DCA for QCLK	
104	RFU				DQSL_t QBCLK Sign	RFU	DQSL_t DCA for QBCLK	
105	DQSL_c IBCLK Sign	RFU	DQSL_c DCA for IBCLK		DQSL_c QCLK Sign	RFU	DQSL_c DCA for QCLK	
106	RFU				DQSL_c QBCLK Sign	RFU	DQSL_c DCA for QBCLK	
107	DQSU_t IBCLK Sign	RFU	DQSU_t DCA for IBCLK		DQSU_t QCLK Sign	RFU	DQSU_t DCA for QCLK	
108	RFU				DQSU_t QBCLK Sign	RFU	DQSU_t DCA for QBCLK	
109	DQSU_c IBCLK Sign	RFU	DQSU_c DCA for IBCLK		DQSU_c QCLK Sign	RFU	DQSU_c DCA for QCLK	
110	RFU				DQSU_c QBCLK Sign	RFU	DQSU_c DCA for QBCLK	
111	RFU			Global DFE Tap-4 Enable	Global DFE Tap-3 Enable	Global DFE Tap-2 Enable	Global DFE Tap-1 Enable	Global DFE gain Enable
112	RFU				DML DFE Gain Bias - See MR for encoding details			
113	DML DFE Tap-1 Bias - See MR for encoding details							
114	DML DFE Tap-2 Bias - See MR for encoding details							
115	DML DFE Tap-3 Bias - See MR for encoding details							
116	DML DFE Tap-4 Bias - See MR for encoding details							
117	RFU							
118	DML VREFDQ sign	DML VREFDQ Offset			RFU			
119	RFU							
120	RFU				DMU DFE Gain Bias - See MR for encoding details			
121	DMU DFE Tap-1 Bias - See MR for encoding details							
122	DMU DFE Tap-2 Bias - See MR for encoding details							
123	DMU DFE Tap-3 Bias - See MR for encoding details							
124	DMU DFE Tap-4 Bias - See MR for encoding details							
125	RFU							

Table 24 — Mode Register Assignment in DDR5 SDRAM (cont'd)

MR#	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
126	DMU VREFDQ sign	DMU VREFDQ Offset			RFU			
127	RFU							
128	RFU				DQL0 DFE Gain Bias - See MR for encoding details			
129	DQL0 DFE Tap-1 Bias - See MR for encoding details							
130	DQL0 DFE Tap-2 Bias - See MR for encoding details							
131	DQL0 DFE Tap-3 Bias - See MR for encoding details							
132	DQL0 DFE Tap-4 Bias - See MR for encoding details							
133	DQL0 IBCLK Sign	RFU	DQL0 DCA for IBCLK		DQL0 QCLK Sign	RFU	DQL0 DCA for QCLK	
134	DQL0 VREFDQ Sign	DQL0 VREFDQ Offset			DQL0 QBCLK Sign	RFU	DQL0 DCA for QBCLK	
135	RFU							
136	RFU				DQL1 DFE Gain Bias - See MR for encoding details			
137	DQL1 DFE Tap-1 Bias - See MR for encoding details							
138	DQL1 DFE Tap-2 Bias - See MR for encoding details							
139	DQL1 DFE Tap-3 Bias - See MR for encoding details							
140	DQL1 DFE Tap-4 Bias - See MR for encoding details							
141	DQL1 IBCLK Sign	RFU	DQL1 DCA for IBCLK		DQL1 QCLK Sign	RFU	DQL1 DCA for QCLK	
142	DQL1 VREFDQ Sign	DQL1 VREFDQ Offset			DQL1 QBCLK Sign	RFU	DQL1 DCA for QBCLK	
143	RFU							
144	RFU				DQL2 DFE Gain Bias - See MR for encoding details			
145	DQL2 DFE Tap-1 Bias - See MR for encoding details							
146	DQL2 DFE Tap-2 Bias - See MR for encoding details							
147	DQL2 DFE Tap-3 Bias - See MR for encoding details							
148	DQL2 DFE Tap-4 Bias - See MR for encoding details							
149	DQL2 IBCLK Sign	RFU	DQL2 DCA for IBCLK		DQL2 QCLK Sign	RFU	DQL2 DCA for QCLK	
150	DQL2 VREFDQ Sign	DQL2 VREFDQ Offset			DQL2 QBCLK Sign	RFU	DQL2 DCA for QBCLK	
155	RFU							
152	RFU				DQL3 DFE Gain Bias - See MR for encoding details			
153	DQL3 DFE Tap-1 Bias - See MR for encoding details							
154	DQL3 DFE Tap-2 Bias - See MR for encoding details							
155	DQL3 DFE Tap-3 Bias - See MR for encoding details							
156	DQL3 DFE Tap-4 Bias - See MR for encoding details							
157	DQL3 IBCLK Sign	RFU	DQL3 DCA for IBCLK		DQL3 QCLK Sign	RFU	DQL3 DCA for QCLK	
158	DQL3 VREFDQ Sign	DQL3 VREFDQ Offset			DQL3 QBCLK Sign	RFU	DQL3 DCA for QBCLK	
159	RFU							
160	RFU				DQL4 DFE Gain Bias - See MR for encoding details			
161	DQL4 DFE Tap-1 Bias - See MR for encoding details							
162	DQL4 DFE Tap-2 Bias - See MR for encoding details							
163	DQL4 DFE Tap-3 Bias - See MR for encoding details							
164	DQL4 DFE Tap-4 Bias - See MR for encoding details							
165	DQL4 IBCLK Sign	RFU	DQL4 DCA for IBCLK		DQL4 QCLK Sign	RFU	DQL4 DCA for QCLK	

Table 24 — Mode Register Assignment in DDR5 SDRAM (cont'd)

MR#	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
166	DQL4 VREFDQ Sign	DQL4 VREFDQ Offset			DQL4 QBCLK Sign	RFU	DQL4 DCA for QBCLK	
167	RFU							
168	RFU				DQL5 DFE Gain Bias - See MR for encoding details			
169	DQL5 DFE Tap-1 Bias - See MR for encoding details							
170	DQL5 DFE Tap-2 Bias - See MR for encoding details							
171	DQL5 DFE Tap-3 Bias - See MR for encoding details							
172	DQL5 DFE Tap-4 Bias - See MR for encoding details							
173	DQL5 IBCLK Sign	RFU	DQL5 DCA for IBCLK		DQL5 QCLK Sign	RFU	DQL5 DCA for QCLK	
174	DQL5 VREFDQ Sign	DQL5 VREFDQ Offset			DQL5 QBCLK Sign	RFU	DQL5 DCA for QBCLK	
175	RFU							
176	RFU				DQL6 DFE Gain Bias - See MR for encoding details			
177	DQL6 DFE Tap-1 Bias - See MR for encoding details							
178	DQL6 DFE Tap-2 Bias - See MR for encoding details							
179	DQL6 DFE Tap-3 Bias - See MR for encoding details							
180	DQL6 DFE Tap-4 Bias - See MR for encoding details							
181	DQL6 IBCLK Sign	RFU	DQL6 DCA for IBCLK		DQL6 QCLK Sign	RFU	DQL6 DCA for QCLK	
182	DQL6 VREFDQ Sign	DQL6 VREFDQ Offset			DQL6 QBCLK Sign	RFU	DQL6 DCA for QBCLK	
183	RFU							
184	RFU				DQL7 DFE Gain Bias - See MR for encoding details			
185	DQL7 DFE Tap-1 Bias - See MR for encoding details							
186	DQL7 DFE Tap-2 Bias - See MR for encoding details							
187	DQL7 DFE Tap-3 Bias - See MR for encoding details							
188	DQL7 DFE Tap-4 Bias - See MR for encoding details							
189	DQL7 IBCLK Sign	RFU	DQL6 DCA for IBCLK		DQL7 QCLK Sign	RFU	DQL7 DCA for QCLK	
190	DQL7 VREFDQ Sign	DQL7 VREFDQ Offset			DQL7 QBCLK Sign	RFU	DQL7 DCA for QBCLK	
191	RFU							
192	RFU				DQU0 DFE Gain Bias - See MR for encoding details			
193	DQU0 DFE Tap-1 Bias - See MR for encoding details							
194	DQU0 DFE Tap-2 Bias - See MR for encoding details							
195	DQU0 DFE Tap-3 Bias - See MR for encoding details							
196	DQU0 DFE Tap-4 Bias - See MR for encoding details							
197	DQU0 IBCLK Sign	RFU	DQU0 DCA for IBCLK		DQU0 QCLK Sign	RFU	DQU0 DCA for QCLK	
198	DQU0 VREFDQ Sign	DQU0 VREFDQ Offset			DQU0 QBCLK Sign	RFU	DQU0 DCA for QBCLK	
199	RFU							
200	RFU				DQU1 DFE Gain Bias - See MR for encoding details			
201	DQU1 DFE Tap-1 Bias - See MR for encoding details							
202	DQU1 DFE Tap-2 Bias - See MR for encoding details							
203	DQU1 DFE Tap-3 Bias - See MR for encoding details							
204	DQU1 DFE Tap-4 Bias - See MR for encoding details							
205	DQU1 IBCLK Sign	RFU	DQU1 DCA for IBCLK		DQU1 QCLK Sign	RFU	DQU1 DCA for QCLK	

Table 24 — Mode Register Assignment in DDR5 SDRAM (cont'd)

MR#	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
206	DQU1 VREFDQ Sign	DQU1 VREFDQ Offset			DQU1 QBCLK Sign	RFU	DQU1 DCA for QBCLK	
207	RFU							
208	RFU				DQU2 DFE Gain Bias - See MR for encoding details			
209	DQU2 DFE Tap-1 Bias - See MR for encoding details							
210	DQU2 DFE Tap-2 Bias - See MR for encoding details							
211	DQU2 DFE Tap-3 Bias - See MR for encoding details							
212	DQU2 DFE Tap-4 Bias - See MR for encoding details							
213	DQU2 IBCLK Sign	RFU	DQU2 DCA for IBCLK		DQU2 QCLK Sign	RFU	DQU2 DCA for QCLK	
214	DQU2 VREFDQ Sign	DQU2 VREFDQ Offset			DQU2 QBCLK Sign	RFU	DQU2 DCA for QBCLK	
215	RFU							
216	RFU				DQU3 DFE Gain Bias - See MR for encoding details			
217	DQU3 DFE Tap-1 Bias - See MR for encoding details							
218	DQU3 DFE Tap-2 Bias - See MR for encoding details							
219	DQU3 DFE Tap-3 Bias - See MR for encoding details							
220	DQU3 DFE Tap-4 Bias - See MR for encoding details							
221	DQU3 IBCLK Sign	RFU	DQU3 DCA for IBCLK		DQU3 QCLK Sign	RFU	DQU3 DCA for QCLK	
222	DQU3 VREFDQ Sign	DQU3 VREFDQ Offset			DQU3 QBCLK Sign	RFU	DQU3 DCA for QBCLK	
223	RFU							
224	RFU				DQU4 DFE Gain Bias - See MR for encoding details			
225	DQU4 DFE Tap-1 Bias - See MR for encoding details							
226	DQU4 DFE Tap-2 Bias - See MR for encoding details							
227	DQU4 DFE Tap-3 Bias - See MR for encoding details							
228	DQU4 DFE Tap-4 Bias - See MR for encoding details							
229	DQU4 IBCLK Sign	RFU	DQU4 DCA for IBCLK		DQU4 QCLK Sign	RFU	DQU4 DCA for QCLK	
230	DQU4 VREFDQ Sign	DQU4 VREFDQ Offset			DQU4 QBCLK Sign	RFU	DQU4 DCA for QBCLK	
231	RFU							
232	RFU				DQU5 DFE Gain Bias - See MR for encoding details			
233	DQU5 DFE Tap-1 Bias - See MR for encoding details							
234	DQU5 DFE Tap-2 Bias - See MR for encoding details							
235	DQU5 DFE Tap-3 Bias - See MR for encoding details							
236	DQU5 DFE Tap-4 Bias - See MR for encoding details							
237	DQU5 IBCLK Sign	RFU	DQU5 DCA for IBCLK		DQU5 QCLK Sign	RFU	DQU5 DCA for QCLK	
238	DQU5 VREFDQ Sign	DQU5 VREFDQ Offset			DQU5 QBCLK Sign	RFU	DQU5 DCA for QBCLK	
239	RFU							
240	RFU				DQU6 DFE Gain Bias - See MR for encoding details			
241	DQU6 DFE Tap-1 Bias - See MR for encoding details							
242	DQU6 DFE Tap-2 Bias - See MR for encoding details							
243	DQU6 DFE Tap-3 Bias - See MR for encoding details							
244	DQU6 DFE Tap-4 Bias - See MR for encoding details							
245	DQU6 IBCLK Sign	RFU	DQU6 DCA for IBCLK		DQU6 QCLK Sign	RFU	DQU6 DCA for QCLK	

Table 24 — Mode Register Assignment in DDR5 SDRAM (cont'd)

MR#	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
246	DQU6 VREFDQ Sign	DQU6 VREFDQ Offset			DQU6 QBCLK Sign	RFU	DQU6 DCA for QBCLK	
247	RFU							
248	RFU				DQU7 DFE Gain Bias - See MR for encoding details			
249	DQU7 DFE Tap-1 Bias - See MR for encoding details							
250	DQU7 DFE Tap-2 Bias - See MR for encoding details							
251	DQU7 DFE Tap-3 Bias - See MR for encoding details							
252	DQU7 DFE Tap-4 Bias - See MR for encoding details							
253	DQU7 IBCLK Sign	RFU	DQU7 DCA for IBCLK		DQU7 QCLK Sign	RFU	DQU7 DCA for QCLK	
254	DQU7 VREFDQ Sign	DQU7 VREFDQ Offset			DQU7 QBCLK Sign	RFU	DQU7 DCA for QBCLK	
255	RFU							

3.5.2 MR0 (MA[7:0]=00H) Burst Length and CAS Latency

MR0 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
CAS Latency (CL)						Burst Length	

Function	Register Type	Operand	Data	Notes
Burst Length	R/W	OP[1:0]	00B: BL16 01B: BC8 OTF 10B: BL32 (Optional) 11B: BL32 OTF (Optional)	
CAS Latency (CL)	R/W	OP[7:2]	000000B: 22 000001B: 24 000010B: 26 000011B: 28 ... 010011B: 60 010100B: 62 010101B: 64 010110B: 66 010111B: 68 011000B: 70 011001B: 72 ... 011101B: 80 011110B: 82 011111B: 84 100000B: 86 100001B: 88 100010B: 90 100011B: 92 100100B: 94 All other encodings reserved.	1, 2

NOTE 1 Range covers both Monolithic DDR5 and 3DS-DDR5 devices up to 9200
NOTE 2 CWL=CL-2, also known as WL=RL-2.

3.5.3 MR1 (MA [7:0] = 01_H) - PDA Mode Details

MR1 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PDA Select ID				PDA Enumerate ID			

Function	Register Type	Operand	Data	Notes
PDA Enumerate ID	R	OP[3:0]	This is a **Read Only** MR field, which is only programmed through an MPC command with the PDA Enumerate ID opcode. $xxxx_B$ Encoding is set with MPC command with the PDA Enumerate ID opcode. This can only be set when PDA Enumerate Programming Mode is enabled and the associated DRAM's DQ0 is asserted LOW. The PDA Enumerate ID opcode includes 4 bits for this encoding. Default setting is 1111_B	
PDA Select ID	R	OP[7:4]	This is a **Read Only** MR field, which is only programmed through an MPC command with the PDA Select ID opcode. $xxxx_B$ Encoding is set with MPC command with the PDA Select ID opcode. The PDA Select ID opcode includes 4 bits for this encoding. 1111_B = all DRAMs execute MRW, MPC, and VrefCA commands For all other encodings, DRAMs execute MRW, MPC, and VrefCA commands only if PDA Select ID[3:0] = PDA Enumerate ID[3:0], with some exceptions for specific MPC commands that execute regardless of PDA Select ID. Default setting is 1111_B	

3.5.4 MR2 (MA [7:0] = 02_H) - Functional Modes

MR2 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Internal Write Timing	Reserved	Device 15 MPSM	CS Assertion Duration (MPC)	Max Power Saving Mode (MPSM)	2N Mode	Write Leveling Training	Read Preamble Training

Function	Register Type	Operand	Data	Notes
Read Preamble Training	R/W	OP[0]	0B: Normal Mode (Default) 1B: Read Preamble Training	
Write Leveling	R/W	OP[1]	0B: Normal Mode (Default) 1B: Write Leveling	1, 2, 3
2N Mode	R	OP[2]	0B: 2N Mode (Default) 1B: 1N Mode	4
Max Power Saving Mode	R/W	OP[3]	0B: Disable (Default) 1B: Enable	
CS Assertion Duration (MPC)	R/W	OP[4]	0B: Only Multiple cycles of CS assertion supported for MPC, VrefCA and VrefCS commands (Default) 1B: Only a single cycle of CS assertion supported for MPC, VrefCA and VrefCS commands	
Device 15 Maximum Power Savings Mode	R/W	OP[5]	0B: Disable (Default) 1B: Enable	
Reserved	Reserved	OP[6]	Reserved	
Internal Write Timing	R/W	OP[7]	0B: Disable 1B: Enable	5

NOTE 1 To enter WL Training Mode the MR field must be programmed to 1. WL Training Mode is used when Internal Write Timing = 0 (External WL Training) and when Internal Write Timing = 1 (Internal WL Training).
NOTE 2 To exit WL Training Mode the MR field must be programmed to 0.
NOTE 3 MRR's are not supported during Write Leveling.
NOTE 4 This mode register is programmed via an explicit MPC command only.
NOTE 5 This is set during WL Training, after the host DQS has been aligned to the ideal External WL timings. The Internal Write Timing is enabled and the WL Internal Timing Alignment is set to ensure the internal Write Enable aligns within tDQS2CK of the external WL Trained location. When Internal Write Timing is Disabled, the WL Internal Cycle Alignment setting does not change the behavior of the write timings

3.5.5 MR3 (MA[7:0]=03_H) - DQS Training

MR3 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Write Leveling Internal Cycle Alignment - Upper Byte				Write Leveling Internal Cycle Alignment - Lower Byte			

Function	Register Type	Operand	Data	Notes
Write Leveling Internal Cycle Alignment - Lower Byte	R/W	OP[3:0]	0000_B: 0 tCK (Default) 0001_B: -1 tCK 0010_B: -2 tCK 0011_B: -3 tCK 0100_B: -4 tCK 0101_B: -5 tCK 0110_B: -6 tCK (Optional OPcode: 0111_B through 1111_B) 0111_B: -7 tCK 1000_B: -8 tCK ... 1110_B: -14 tCK 1111_B: -15 tCK	1, 2, 3, 5
Write Leveling Internal Cycle Alignment - Upper Byte	R/W	OP[7:4]	0000_B: 0 tCK (Default) 0001_B: -1 tCK 0010_B: -2 tCK 0011_B: -3 tCK 0100_B: -4 tCK 0101_B: -5 tCK 0110_B: -6 tCK (Optional OPcode: 0111_B through 1111_B) 0111_B: -7 tCK 1000_B: -8 tCK ... 1110_B: -14 tCK 1111_B: -15 tCK	1, 2, 4, 5

NOTE 1 This is set during WL Training, after the host DQS has been aligned to the ideal External WL timings. The Internal Write Timing is enabled and the WL Internal Timing Alignment is set to ensure the internal Write Enable aligns within t_{DQS2CK} of the external WL Trained location. When Internal Write Timing is Disabled, the WL Internal Cycle Alignment setting does not change the behavior of the write timings.

NOTE 2 The DRAM implementation may optionally have the same behavior when the Internal Write Timing is enabled vs disabled. This would mean that the CK and DQS timing paths remain matched internally. The WL Internal Cycle Alignment setting must still support pulling the Internal WL Pulse earlier so that the same WL Training Flow will produce the correct result.

NOTE 3 Lower Byte WL Internal Cycle Alignment is intended for x4, x8, and x16 configurations.

NOTE 4 Upper Byte WL Internal Cycle Alignment is intended for x16 configuration only. Although training of the Lower and Upper Bytes is independent, contact the DRAM vendor regarding recommendations for setting the WICA values to the same offset.

NOTE 5 Optional OPcode may be needed for certain speed bins.

3.5.6 MR4 (MA[7:0]=04_H) - Refresh Settings

MR4 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TUF	RFU	Wide Range (Optional)	Refresh tRFC Mode	Refresh Interval Rate Indicator	Minimum Refresh Rate		

Refresh Settings MR4 Register Information Table

Function	Register Type	Operand	Data	Notes
Minimum Refresh Rate	R	OP[2:0]	If Wide Range is not supported (OP[5]=0): 000_B: RFU 001_B: tREFI x1 (1x Refresh Rate), <80 °C nominal 010_B: tREFI x1 (1x Refresh Rate), 80-85 °C nominal 011_B: tREFI /2 (2x Refresh Rate), 85-90 °C nominal 100_B: tREFI /2 (2x Refresh Rate), 90-95 °C nominal 101_B: tREFI /2 (2x Refresh Rate), >95 °C nominal 110_B: RFU 111_B: RFU If Wide Range is supported (OP[5]=1): 000_B: tREFI x1 (1x Refresh Rate), <75 °C nominal 001_B: tREFI x1 (1x Refresh Rate), 75-80 °C nominal 010_B: tREFI x1 (1x Refresh Rate), 80-85 °C nominal 011_B: tREFI /2 (2x Refresh Rate), 85-90 °C nominal 100_B: tREFI /2 (2x Refresh Rate), 90-95 °C nominal 101_B: tREFI /2 (2x Refresh Rate), 95-100 °C nominal 110_B: tREFI /2 (2x Refresh Rate), >100 °C nominal 111_B: RFU	1, 2, 3, 4, 5, 6, 7, 8
Refresh Interval Rate Indicator	SR/W	OP[3]	DRAM Status Read (SR): 0_B: Not implemented (Default) 1_B: Implemented Host Write (W): 0_B: Disabled (Default) 1_B: Enabled	
Refresh tRFC Mode	R/W	OP[4]	0_B: Normal Refresh Mode (tRFC1) 1_B: Fine Granularity Refresh Mode (tRFC2)	
Wide Range (Optional)	R	OP[5]	0_B: Wide range is not supported 1_B: Wide range is supported (Optional)	
RFU	RFU	OP[6]	RFU	
TUF (Temperature Update Flag)	R	OP[7]	0_B: No change in OP[2:0] since last MR4 read (default) 1_B: Change in OP[2:0] since last MR4 read	

Refresh Settings MR4 Register Information Table (cont'd)

NOTE 1	The minimum required refresh rate for each OP[2:0] setting applies to tREFI1 and tREFI2. Each OP[2:0] setting specifies a nominal temperature range. The ranges defined by OP[2:0] are determined by temperature thresholds used by the system for proper operation.
NOTE 2	When OP[5]=0, the four temperature thresholds are nominally at 80 °C, 85 °C, 90 °C, and 95 °C. The <80 °C threshold has no minimum value specified and the >95°C threshold has no maximum temperature value specified. When OP[5]=1, the six temperature thresholds are nominally at 75 °C, 80 °C, 85 °C, 90 °C, 95 °C, and 100 °C. The <75 °C threshold has no minimum value specified and the >100 °C threshold has no maximum temperature value specified
NOTE 3	DRAM vendors must report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range when the system refresh interval follows there guidelines: ● Threshold ≤ 85 °C: tREFI x1 (1x Refresh Rate) or faster may be used ● Threshold > 85 °C: tREFI /2 (2x Refresh Rate) or faster is required ● Data integrity at thresholds >95°C is not assured regardless of refresh rate
NOTE 4	The 2x Refresh Rate must be provided by the system before the DRAM Tj has gone up by more than 2 °C (Temperature Margin) since the first report out of OP[2:0]=011B. This condition is reset when OP[2:0] is equal to 010B.
NOTE 5	The device may not operate properly when OP[2:0]=101B, if the DRAM Tj has gone up by more than 2 °C (Temperature Margin) since the first report out of OP[2:0]=101B. This condition is reset when OP[2:0] is equal to 100B. OP[2:0]=101B must be a temporary condition of the DRAM, to be addressed by immediately reducing the Tj of the DRAM by throttling its power, and/or the power of nearby devices.
NOTE 6	OP[7] = 0 at power-up. OP[2:0] bits are valid after initialization sequence (Te).
NOTE 7	See the section on "Temperature Sensor" for information on the recommended frequency of reading MR4
NOTE 8	Support for wide range temperature sensor ranges does not indicate that the DDR5 DRAM device may operate properly at temperature ranges above 95 °C – side effects may include loss of data integrity

3.5.7 MR5 (MA[7:0]=05_H) - IO Settings

MR5 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Pull-Down Output Driver Impedance		DM Enable	TDQS Enable	PODTM Support	Pull-up Output Driver Impedance		Data Output Disable

Function	Register Type	Operand	Data	Notes
Data Output Disable	W	OP[0]	0_B: Normal Operation (Default) 1_B: Outputs Disabled	
Pull-up Output Driver Impedance	R/W	OP[2:1]	00_B: RZQ/7 (34) 01_B: RZQ/6 (40) 10_B: RZQ/5 (48) 11_B: RFU	
Package Output Driver Test Mode Supported	R	OP[3]	0B: Function Not Supported 1B: Function Supported	
TDQS Enable	R/W	OP[4]	0B: Disable (Default) 1B: Enable	
DM Enable	R/W	OP[5]	0B: Disable (Default) 1B: Enable	
Pull-Down Output Driver Impedance	R/W	OP[7:6]	00B: RZQ/7 (34) 01B: RZQ/6 (40) 10B: RZQ/5 (48) 11B: RFU	

3.5.8 MR6 (MA[7:0]=06_H) - Write Recovery Time and tRTP

MR6 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
tRTP				Write Recovery Time			

Function	Register Type	Operand	Data	Notes
Write Recovery Time Legacy / PRAC	R/W	OP[3:0]	0000_B: 48nCK (Legacy) / 16nCK (PRAC) 0001_B: 54nCK (Legacy) / 18nCK (PRAC) 0010_B: 60nCK (Legacy) / 20nCK (PRAC) 0011_B: 66nCK (Legacy) / 22nCK (PRAC) 0100_B: 72nCK (Legacy) / 24nCK (PRAC) 0101_B: 78nCK (Legacy) / 26nCK (PRAC) 0110_B: 84nCK (Legacy) / 28nCK (PRAC) 0111_B: 90nCK (Legacy) / 30nCK (PRAC) 1000_B: 96nCK (Legacy) / 32nCK (PRAC) 1001_B: 102nCK (Legacy) / 34nCK (PRAC) 1010_B: 108nCK (Legacy) / 36nCK (PRAC) 1011_B: 114nCK (Legacy) / 38nCK (PRAC) 1100_B: 120nCK (Legacy) / 40nCK (PRAC) 1101_B: 126nCK (Legacy) / 42nCK (PRAC) 1110_B: 132nCK (Legacy) / 44nCK (PRAC) 1111_B: 138nCK (Legacy) / 46nCK (PRAC)	1
tRTP Legacy / PRAC	R/W	OP[7:4]	0000_B: 12nCK 0001_B: 14nCK 0010_B: 15nCK 0011_B: 17nCK 0100_B: 18nCK 0101_B: 20nCK 0110_B: 21nCK 0111_B: 23nCK 1000_B: 24nCK 1001_B: 26nCK 1010_B: 27nCK 1011_B: 29nCK 1100_B: 30nCK 1101_B: 32nCK 1110_B: 33nCK 1111_B: 35nCK	2

NOTE 1 tWR,min is defined in the “Timing Parameters” tables (Table 334 - Table 336). Host must operate with MR settings resulting in tCK * MR6:OP[3:0] >= tWR,min.
NOTE 2 tRTP, min is defined in the “Timing Parameters” tables (Table 328 - Table 330). Host must operate with MR settings resulting in tCK * MR6:OP[7:4]>= tRTP,min.
NOTE 3 All nCK conversions require rounding algorithm consideration.

3.5.9 MR7 (MA[7:0]=07_H) - Write Leveling Internal +0.5tCK Alignment Offset

MR7 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU						(Optional) Write Leveling Internal +0.5tCK Alignment Offset - Upper Byte	(Optional) Write Leveling Internal +0.5tCK Alignment Offset - Lower Byte

Function	Register Type	Operand	Data	Notes
(Optional) Write Leveling Internal +0.5tCK Alignment Offset - Lower Byte	R/W	OP[0]	0B: Disabled (Default) 1B: 0.5tCK	1, 2
(Optional) Write Leveling Internal +0.5tCK Alignment Offset - Upper Byte	R/W	OP[1]	0B: Disabled (Default) 1B: 0.5tCK	1, 3
RFU	RFU	OP[7:2]	RFU	

NOTE 1 The WICA 0.5 tCK offset is a positive adjustment to the target WICA value. (Ex. MR3:OP[3:0] = -3 tCK (0011B) and MR7:OP[0] = 1, WICA + WICAhalfCycle = -3 tCK + 0.5 tCK = -2.5 tCK)
NOTE 2 Lower Byte WL Internal Cycle Alignment is intended for x4, x8, and x16 configurations.
NOTE 3 Upper Byte WL Internal Cycle Alignment is intended for x16 configuration only. Although training of the Lower and Upper Bytes is independent, contact the DRAM vendor regarding recommendations for setting the WICA values to the same offset.
NOTE 4 When operating at 1980-2100 MT/s (CL=22), the host shall not apply the WICA 0.5tCK offset.

3.5.10 MR8 (MA[7:0]=08_H) - Preamble / Postamble

MR8 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Write Postamble Settings	Read Postamble Settings	RFU	Write Preamble Settings		Read Preamble Settings		

Function	Register Type	Operand	Data	Notes
Read Preamble Settings	R/W	OP[2:0]	000B: 1 tCK - 10 Pattern 001B: 2 tCK - 0010 Pattern 010B: 2 tCK - 1110 Pattern (DDR4 Style) 011B: 3 tCK - 000010 Pattern 100B: 4 tCK - 00001010 Pattern 101B: Reserved 110B: Reserved 111B: Reserved	1
Write Preamble Settings	R/W	OP[4:3]	00B: Reserved 01B: 2 tCK - 0010 Pattern (Default) 10B: 3 tCK - 000010 Pattern 11B: 4 tCK - 00001010 Pattern	
RFU	RFU	OP[5]	RFU	
Read Postamble Settings	R/W	OP[6]	0B: 0.5 tCK - 0 Pattern 1B: 1.5 tCK - 010 Pattern	
Write Postamble Settings	R/W	OP[7]	0B: 0.5 tCK - 0 Pattern 1B: 1.5 tCK - 000 Pattern	

NOTE 1 Please refer to the Preamble Specification for details on the Read Preamble modes and patterns.

3.5.11 MR9 (MA[7:0]=09H) - Writeback Suppression and TM

MR9 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TM	RFU					x4 Write	ECS Write-back

Function	Register Type	Operand	Data	Notes
ECS Writeback	R/W	OP[0]	0B: Do not suppress writeback of Data and ECC Check Bits (Default) 1B: Suppress writeback of Data and ECC Check Bits (Optional)	1
x4 Writes	R/W	OP[1]	0B: Do not suppress writeback of Data during RMW (Default) 1B: Suppress writeback of Data during RMW (Optional)	1
RFU	RFU	OP[6:2]	RFU	
TM	W	OP[7]	0B: Normal (Default) 1B: Test Mode	

NOTE 1 DDR5 SPD Byte 14 Bits[2:1] indicates if feature is supported and will also indicate whether to use MR9 or MR15 for enabling the modes.

3.5.12 MR10 (MA[7:0]=0A$_H$) - VrefDQ Calibration Value

MR10 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
VrefDQ Calibration Value							

Function	Register Type	Operand	Data	Notes
VrefDQ Cal Value	R/W	OP[7:0]	0000:0000B: --Thru-- 1111:1111B: See Table 25	

Table 25 — VrefDQ Setting Range

Function	Operand						Notes
VrefDQ Cal Value for MR10	OP	0000 0000$_B$: 97.5%	0001 1011$_B$: 84.0%	0011 0110$_B$: 70.5%	0101 0001$_B$: 57.0%	0110 1100$_B$: 43.5%	
		0000 0001$_B$: 97.0%	0001 1100$_B$: 83.5%	0011 0111$_B$: 70.0%	0101 0010$_B$: 56.5%	0110 1101$_B$: 43.0%	
		0000 0010$_B$: 96.5%	0001 1101$_B$: 83.0%	0011 1000$_B$: 69.5%	0101 0011$_B$: 56.0%	0110 1110$_B$: 42.5%	
		0000 0011$_B$: 96.0%	0001 1110$_B$: 82.5%	0011 1001$_B$: 69.0%	0101 0100$_B$: 55.5%	0110 1111$_B$: 42.0%	
		0000 0100$_B$: 95.5%	0001 1111$_B$: 82.0%	0011 1010$_B$: 68.5%	0101 0101$_B$: 55.0%	0111 0000$_B$: 41.5%	
		0000 0101$_B$: 95.0%	0010 0000$_B$: 81.5%	0011 1011$_B$: 68.0%	0101 0110$_B$: 54.5%	0111 0001$_B$: 41.0%	
		0000 0110$_B$: 94.5%	0010 0001$_B$: 81.0%	0011 1100$_B$: 67.5%	0101 0111$_B$: 54.0%	0111 0010$_B$: 40.5%	
		0000 0111$_B$: 94.0%	0010 0010$_B$: 80.5%	0011 1101$_B$: 67.0%	0101 1000$_B$: 53.5%	0111 0011$_B$: 40.0%	
		0000 1000$_B$: 93.5%	0010 0011$_B$: 80.0%	0011 1110$_B$: 66.5%	0101 1001$_B$: 53.0%	0111 0100$_B$: 39.5%	
		0000 1001$_B$: 93.0%	0010 0100$_B$: 79.5%	0011 1111$_B$: 66.0%	0101 1010$_B$: 52.5%	0111 0101$_B$: 39.0%	
		0000 1010$_B$: 92.5%	0010 0101$_B$: 79.0%	0100 0000$_B$: 65.5%	0101 1011$_B$: 52.0%	0111 0110$_B$: 38.5%	
		0000 1011$_B$: 92.0%	0010 0110$_B$: 78.5%	0100 0001$_B$: 65.0%	0101 1100$_B$: 51.5%	0111 0111$_B$: 38.0%	
		0000 1100$_B$: 91.5%	0010 0111$_B$: 78.0%	0100 0010$_B$: 64.5%	0101 1101$_B$: 51.0%	0111 1000$_B$: 37.5%	
		0000 1101$_B$: 91.0%	0010 1000$_B$: 77.5%	0100 0011$_B$: 64.0%	0101 1110$_B$: 50.5%	0111 1001$_B$: 37.0%	
		0000 1110$_B$: 90.5%	0010 1001$_B$: 77.0%	0100 0100$_B$: 63.5%	0101 1111$_B$: 50.0%	0111 1010$_B$: 36.5%	
		0000 1111$_B$: 90.0%	0010 1010$_B$: 76.5%	0100 0101$_B$: 63.0%	0110 0000$_B$: 49.5%	0111 1011$_B$: 36.0%	
		0001 0000$_B$: 89.5%	0010 1011$_B$: 76.0%	0100 0110$_B$: 62.5%	0110 0001$_B$: 49.0%	0111 1100$_B$: 35.5%	
		0001 0001$_B$: 89.0%	0010 1100$_B$: 75.5%	0100 0111$_B$: 62.0%	0110 0010$_B$: 48.5%	0111 1101$_B$: 35.0%	
		0001 0010$_B$: 88.5%	0010 1101$_B$: 75.0%	0100 1000$_B$: 61.5%	0110 0011$_B$: 48.0%	All Others: Reserved	
		0001 0011$_B$: 88.0%	0010 1110$_B$: 74.5%	0100 1001$_B$: 61.0%	0110 0100$_B$: 47.5%		
		0001 0100$_B$: 87.5%	0010 1111$_B$: 74.0%	0100 1010$_B$: 60.5%	0110 0101$_B$: 47.0%		
		0001 0101$_B$: 87.0%	0011 0000$_B$: 73.5%	0100 1011$_B$: 60.0%	0110 0110$_B$: 46.5%		
		0001 0110$_B$: 86.5%	0011 0001$_B$: 73.0%	0100 1100$_B$: 59.5%	0110 0111$_B$: 46.0%		
		0001 0111$_B$: 86.0%	0011 0010$_B$: 72.5%	0100 1101$_B$: 59.0%	0110 1000$_B$: 45.5%		
		0001 1000$_B$: 85.5%	0011 0011$_B$: 72.0%	0100 1110$_B$: 58.5%	0110 1001$_B$: 45.0%		
		0001 1001$_B$: 85.0%	0011 0100$_B$: 71.5%	0100 1111$_B$: 58.0%	0110 1010$_B$: 44.5%		
		0001 1010$_B$: 84.5%	0011 0101$_B$: 71.0%	0101 0000$_B$: 57.5%	0110 1011$_B$: 44.0%		

3.5.13 MR11 (MA[6:0]=0B$_H$) - Vref CA Calibration Value

MR11 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
VrefCA Calibration Value							

Function	Register Type	Operand	Data	Notes
VrefCA Cal Value	R	OP[6:0]	000:0000B: --Thru-- 111:1111B: See Table 26	1, 2
	R	OP[7]	V: Valid	

NOTE 1 Since VREF CA Calibration setting has an explicit command (VrefCA COMMAND), it can only be programmed via that command and its mode register is therefore read only.
NOTE 2 Since the state of CA12 is used to differentiate the VrefCA vs VrefCS command, the MR11/12 OP[7] value is defined as valid.

Table 26 — VrefCA Setting Range

Function	Operand						Notes
VrefCA Cal Value for MR11	OP	V000 0000$_B$: 97.5%	V001 1011$_B$: 84.0%	V011 0110$_B$: 70.5%	V101 0001$_B$: 57.0%	V110 1100$_B$: 43.5%	
		V000 0001$_B$: 97.0%	V001 1100$_B$: 83.5%	V011 0111$_B$: 70.0%	V101 0010$_B$: 56.5%	V110 1101$_B$: 43.0%	
		V000 0010$_B$: 96.5%	V001 1101$_B$: 83.0%	V011 1000$_B$: 69.5%	V101 0011$_B$: 56.0%	V110 1110$_B$: 42.5%	
		V000 0011$_B$: 96.0%	V001 1110$_B$: 82.5%	V011 1001$_B$: 69.0%	V101 0100$_B$: 55.5%	V110 1111$_B$: 42.0%	
		V000 0100$_B$: 95.5%	V001 1111$_B$: 82.0%	V011 1010$_B$: 68.5%	V101 0101$_B$: 55.0%	V111 0000$_B$: 41.5%	
		V000 0101$_B$: 95.0%	V010 0000$_B$: 81.5%	V011 1011$_B$: 68.0%	V101 0110$_B$: 54.5%	V111 0001$_B$: 41.0%	
		V000 0110$_B$: 94.5%	V010 0001$_B$: 81.0%	V011 1100$_B$: 67.5%	V101 0111$_B$: 54.0%	V111 0010$_B$: 40.5%	
		V000 0111$_B$: 94.0%	V010 0010$_B$: 80.5%	V011 1101$_B$: 67.0%	V101 1000$_B$: 53.5%	V111 0011$_B$: 40.0%	
		V000 1000$_B$: 93.5%	V010 0011$_B$: 80.0%	V011 1110$_B$: 66.5%	V101 1001$_B$: 53.0%	V111 0100$_B$: 39.5%	
		V000 1001$_B$: 93.0%	V010 0100$_B$: 79.5%	V011 1111$_B$: 66.0%	V101 1010$_B$: 52.5%	V111 0101$_B$: 39.0%	
		V000 1010$_B$: 92.5%	V010 0101$_B$: 79.0%	V100 0000$_B$: 65.5%	V101 1011$_B$: 52.0%	V111 0110$_B$: 38.5%	
		V000 1011$_B$: 92.0%	V010 0110$_B$: 78.5%	V100 0001$_B$: 65.0%	V101 1100$_B$: 51.5%	V111 0111$_B$: 38.0%	
		V000 1100$_B$: 91.5%	V010 0111$_B$: 78.0%	V100 0010$_B$: 64.5%	V101 1101$_B$: 51.0%	V111 1000$_B$: 37.5%	
		V000 1101$_B$: 91.0%	V010 1000$_B$: 77.5%	V100 0011$_B$: 64.0%	V101 1110$_B$: 50.5%	V111 1001$_B$: 37.0%	
		V000 1110$_B$: 90.5%	V010 1001$_B$: 77.0%	V100 0100$_B$: 63.5%	V101 1111$_B$: 50.0%	V111 1010$_B$: 36.5%	
		V000 1111$_B$: 90.0%	V010 1010$_B$: 76.5%	V100 0101$_B$: 63.0%	V110 0000$_B$: 49.5%	V111 1011$_B$: 36.0%	
		V001 0000$_B$: 89.5%	V010 1011$_B$: 76.0%	V100 0110$_B$: 62.5%	V110 0001$_B$: 49.0%	V111 1100$_B$: 35.5%	
		V001 0001$_B$: 89.0%	V010 1100$_B$: 75.5%	V100 0111$_B$: 62.0%	V110 0010$_B$: 48.5%	V111 1101$_B$: 35.0%	
		V001 0010$_B$: 88.5%	V010 1101$_B$: 75.0%	V100 1000$_B$: 61.5%	V110 0011$_B$: 48.0%	All Others: Reserved	
		V001 0011$_B$: 88.0%	V010 1110$_B$: 74.5%	V100 1001$_B$: 61.0%	V110 0100$_B$: 47.5%		
		V001 0100$_B$: 87.5%	V010 1111$_B$: 74.0%	V100 1010$_B$: 60.5%	V110 0101$_B$: 47.0%		
		V001 0101$_B$: 87.0%	V011 0000$_B$: 73.5%	V100 1011$_B$: 60.0%	V110 0110$_B$: 46.5%		
		V001 0110$_B$: 86.5%	V011 0001$_B$: 73.0%	V100 1100$_B$: 59.5%	V110 0111$_B$: 46.0%		
		V001 0111$_B$: 86.0%	V011 0010$_B$: 72.5%	V100 1101$_B$: 59.0%	V110 1000$_B$: 45.5%		
		V001 1000$_B$: 85.5%	V011 0011$_B$: 72.0%	V100 1110$_B$: 58.5%	V110 1001$_B$: 45.0%		
		V001 1001$_B$: 85.0%	V011 0100$_B$: 71.5%	V100 1111$_B$: 58.0%	V110 1010$_B$: 44.5%		
		V001 1010$_B$: 84.5%	V011 0101$_B$: 71.0%	V101 0000$_B$: 57.5%	V110 1011$_B$: 44.0%		

NOTE "V" = Valid.

3.5.14 MR12 (MA[7:0]=0C$_H$) - Vref CS Calibration Value

MR12 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
VrefCS Calibration Value							

Function	Register Type	Operand	Data	Notes
VrefCS Cal Value	R	OP[6:0]	000:0000B: --Thru-- 111:1111B: See Table 27	1, 2
	R	OP[7]	V: Valid	

NOTE 1 Since VREF CS Calibration setting has an explicit command (VrefCS COMMAND), it can only be programmed via that command and its mode register is therefore read only.
NOTE 2 Since the state of CA12 is used to differentiate the VrefCA vs VrefCS command, the MR11/12 OP[7] value is defined as valid.

Table 27 — VrefCS Setting Range

Function	Operand						Notes
VrefCS Cal Value for MR12	OP	V000 0000B: 97.5%	V001 1011B: 84.0%	V011 0110B: 70.5%	V101 0001B: 57.0%	V110 1100B: 43.5%	
		V000 0001B: 97.0%	V001 1100B: 83.5%	V011 0111B: 70.0%	V101 0010B: 56.5%	V110 1101B: 43.0%	
		V000 0010B: 96.5%	V001 1101B: 83.0%	V011 1000B: 69.5%	V101 0011B: 56.0%	V110 1110B: 42.5%	
		V000 0011B: 96.0%	V001 1110B: 82.5%	V011 1001B: 69.0%	V101 0100B: 55.5%	V110 1111B: 42.0%	
		V000 0100B: 95.5%	V001 1111B: 82.0%	V011 1010B: 68.5%	V101 0101B: 55.0%	V111 0000B: 41.5%	
		V000 0101B: 95.0%	V010 0000B: 81.5%	V011 1011B: 68.0%	V101 0110B: 54.5%	V111 0001B: 41.0%	
		V000 0110B: 94.5%	V010 0001B: 81.0%	V011 1100B: 67.5%	V101 0111B: 54.0%	V111 0010B: 40.5%	
		V000 0111B: 94.0%	V010 0010B: 80.5%	V011 1101B: 67.0%	V101 1000B: 53.5%	V111 0011B: 40.0%	
		V000 1000B: 93.5%	V010 0011B: 80.0%	V011 1110B: 66.5%	V101 1001B: 53.0%	V111 0100B: 39.5%	
		V000 1001B: 93.0%	V010 0100B: 79.5%	V011 1111B: 66.0%	V101 1010B: 52.5%	V111 0101B: 39.0%	
		V000 1010B: 92.5%	V010 0101B: 79.0%	V100 0000B: 65.5%	V101 1011B: 52.0%	V111 0110B: 38.5%	
		V000 1011B: 92.0%	V010 0110B: 78.5%	V100 0001B: 65.0%	V101 1100B: 51.5%	V111 0111B: 38.0%	
		V000 1100B: 91.5%	V010 0111B: 78.0%	V100 0010B: 64.5%	V101 1101B: 51.0%	V111 1000B: 37.5%	
		V000 1101B: 91.0%	V010 1000B: 77.5%	V100 0011B: 64.0%	V101 1110B: 50.5%	V111 1001B: 37.0%	
		V000 1110B: 90.5%	V010 1001B: 77.0%	V100 0100B: 63.5%	V101 1111B: 50.0%	V111 1010B: 36.5%	
		V000 1111B: 90.0%	V010 1010B: 76.5%	V100 0101B: 63.0%	V110 0000B: 49.5%	V111 1011B: 36.0%	
		V001 0000B: 89.5%	V010 1011B: 76.0%	V100 0110B: 62.5%	V110 0001B: 49.0%	V111 1100B: 35.5%	
		V001 0001B: 89.0%	V010 1100B: 75.5%	V100 0111B: 62.0%	V110 0010B: 48.5%	V111 1101B: 35.0%	
		V001 0010B: 88.5%	V010 1101B: 75.0%	V100 1000B: 61.5%	V110 0011B: 48.0%	All Others: Reserved	
		V001 0011B: 88.0%	V010 1110B: 74.5%	V100 1001B: 61.0%	V110 0100B: 47.5%		
		V001 0100B: 87.5%	V010 1111B: 74.0%	V100 1010B: 60.5%	V110 0101B: 47.0%		
		V001 0101B: 87.0%	V011 0000B: 73.5%	V100 1011B: 60.0%	V110 0110B: 46.5%		
		V001 0110B: 86.5%	V011 0001B: 73.0%	V100 1100B: 59.5%	V110 0111B: 46.0%		
		V001 0111B: 86.0%	V011 0010B: 72.5%	V100 1101B: 59.0%	V110 1000B: 45.5%		
		V001 1000B: 85.5%	V011 0011B: 72.0%	V100 1110B: 58.5%	V110 1001B: 45.0%		
		V001 1001B: 85.0%	V011 0100B: 71.5%	V100 1111B: 58.0%	V110 1010B: 44.5%		
		V001 1010B: 84.5%	V011 0101B: 71.0%	V101 0000B: 57.5%	V110 1011B: 44.0%		

NOTE "V" = Valid.

3.5.15 MR13 (MA [7:0] = 0DH) - SRX/NOP Clock-Sync / CS Geardown / tCCD_L / tCCD_L_WR / tCCD_L_WR2 / tDLLK

MR13 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		SRX/NOP Clock-Sync Support and Enable/Disable at next SRX (Optional)	CS Geardown Enable/ Disable at next SREF	tCCD_L / tCCD_L_WR / tCCD_L_WR2 / tDLLK			

Function	Register Type	Operand	Data	Notes
tCCD_L / tCCD_L_WR / tCCD_L_WR2 / tDLLK	R	OP[3:0]	0000B: --Thru-- 1111B: See Table Below	
CS Geardown Enable/Disable at next SREF	W/R	OP[4]	0B: CS Geardown is disabled at next SREF (Default). 1B: CS Geardown is enabled at next SREF.	
SRX/NOP Clock-Sync Support and Enable/Disable at next SRX (Optional)	SR/W	OP[5]	DRAM Status Read (SR): 0B: SRX/NOP Clock-Sync not supported (Default). 1B: SRX/NOP Clock-Sync supported. Host Write (W): 0B: Disable SRX/NOP Clock-Sync (Default). 1B: Enable SRX/NOP Clock-Sync.	1
RFU	RFU	OP[7:6]	RFU	

NOTE 1 Host shall program MR13:OP[5]=1 via MRW command to update to enable/disable the SRX/NOP Clock-Sync feature at next SRX, if needed. During the next Self-Refresh, DRAM will automatically apply the update to the function.

Table 28 — tCCD_L/tCCD_L_WR/tCCD_L_WR2/tDLLK Encoding Details

Function	OP[3:0]	tCCD_L.min (nCK)	tCCD_L_WR2. min (nCK)	tCCD_L_WR. min (nCK)	tDLLK.min (nCK)	Details	Notes
tCCD_L / tCCD_L_WR / tCCD_L_WR2/ tDLLK	0000	8	16	32	1024	1980 MT/s ≤ Data Rate ≤ 2100 MT/s & 2933 MT/s ≤ Data Rate =< 3200 MT/s	1, 2, 3
	0001	9	18	36	1024	3200 MT/s < Data Rate ≤ 3600 MT/s	
	0010	10	20	40	1280	3600 MT/s < Data Rate ≤ 4000 MT/s	
	0011	11	22	44	1280	4000 MT/s < Data Rate ≤ 4400 MT/s	
	0100	12	24	48	1536	4400 MT/s < Data Rate ≤ 4800 MT/s	
	0101	13	26	52	1536	4800 MT/s < Data Rate ≤ 5200 MT/s	
	0110	14	28	56	1792	5200 MT/s < Data Rate ≤ 5600 MT/s	
	0111	15	30	60	1792	5600 MT/s < Data Rate ≤ 6000 MT/s	
	1000	16	32	64	2048	6000 MT/s < Data Rate ≤ 6400 MT/s	
	1001	17	34	68	2048	6400 MT/s < Data Rate ≤ 6800 MT/s	
	1010	18	36	72	2304	6800 MT/s < Data Rate ≤ 7200 MT/s	
	1011	19	38	76	2304	7200 MT/s < Data Rate ≤ 7600 MT/s	
	1100	20	40	80	2560	7600 MT/s < Data Rate ≤ 8000 MT/s	
	1101	21	42	84	2560	8000 MT/s < Data Rate ≤ 8400 MT/s	
	1110	22	44	88	2816	8400 MT/s < Data Rate ≤ 8800 MT/s	
	1111	23	46	92	2816	8800MT/s< Data Rate ≤ 9200MT/s	

NOTE 1 tCCD_L /tCCD_L_WR/tCCD_L_WR2/tDLLK are programmed according to the value defined in the AC parametric table per operating frequency.
NOTE 2 The register type is “R” (read only) since MR13 is set by the “Configure tDLLK/tCCD_L/tCCD_L_WR/tCCD_L_WR2” MPC command.
NOTE 3 Data rate ranges align with Speed Bin Table definitions.

3.5.16 MR14 (MA[7:0]=0EH) - Transparency ECC Configuration

MR14 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
ECS Mode	Reset ECS Counter	Row Mode/Code Word Mode	RFU	CID3	CID2	CID1	CID0

Function	Register Type	Operand	Data	Notes
ECS Error Register Index/MBIST Rank Select	R/W	OP[3:0]	CID[3:0]	1, 2, 3, 4
RFU	RFU	OP[4]	RFU	
Code Word/Row Count	R/W	OP[5]	0B: ECS counts Rows with errors 1B: ECS counts Code words with errors	1
ECS Reset Counter	W	OP[6]	0B: Normal (Default) 1B: Reset ECC Counter	1,4
ECS Mode	R/W	OP[7]	0B: Manual ECS Mode Disabled (Default) 1B: Manual ECS Mode Enabled	1

NOTE 1 MR14:OP[3:0] must be setup by MRW to indicate which slice in the 3DS-DDR5 stack is referenced by the MRR for MR14MR20 ECS transparency data, MR22 MBIST transparency data, and MR54-MR57 hPPR resource availability. On 3DS devices that support optional MBIST/mPPR, prior to MBIST initialization via MR23:OP[4] followed by guard keys, MR14:OP[3:0] must be programmed by MRW according to the logical rank that is desired to perform MBIST.
NOTE 2 CID[3:0] encoding is based on the stack height of the device and varies depending on the number of dies in the stack.
NOTE 3 For Monolithic DDR5, CID[3:0] should be set to 0.
NOTE 4 ECS stands for Error Check Scrub operation.

3.5.17 MR15 (MA[7:0]=0F$_H$) - Transparency ECC Threshold per Gb of Memory Cells and Automatic ECS in Self Refresh

MR15 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
x4 Writes	ECS Writeback	RFU		Automatic ECS in Self Refresh	ECS Error Threshold Count (ETC)		

Function	Register Type	Operand	Data	Notes
ECS Error Threshold Count (ETC)	R/W	OP[2:0]	000B: 4 001B: 16 010B: 64 011B: 256 (Default) 100B: 1024 101B: 4096 110B: RFU 111B: RFU	
Automatic ECS in Self Refresh	W	OP[3]	0B: Automatic ECS disabled in Self-Refresh in Manual ECS mode (default) 1B: Automatic ECS enabled in Self-Refresh in Manual ECS mode	
RFU	RFU	OP[5:4]	RFU	
ECS Writeback	R/W	OP[6]	0B: Do not suppress writeback of Data and ECC Check Bits (Default) 1B: Suppress writeback of Data and ECC Check Bits (Optional)	4
x4 Writes	R/W	OP[7]	0B: Do not suppress writeback of Data during RMW (Default) 1B: Suppress writeback of Data during RMW (Optional)	4

NOTE 1 MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR14 through MR20 transparency data.
NOTE 2 DDR5 performs Automatic ECS operation while in Self-Refresh mode either by enabling MR15:OP[3]=1_B (Automatic ECS in Self-Refresh enable) or disabling MR14:OP[7]=0_B (Automatic ECS mode enable).
NOTE 3 If the Automatic ECS in Self-Refresh is enabled, transparency mode-registers updated cannot be controlled by the number of Manual ECS operation MPC command since the ECS counter is increased by both manual ECS command and the Automatic ECS Operation in Self-Refresh mode.
NOTE 4 DDR5 SPD Byte 14 Bits[2:1] indicates if feature is supported and will also indicate whether to use MR9 or MR15 for enabling the modes.

3.5.18 MR16 (MA [7:0] = 10_H) - Row Address with Max Errors 1

MR16 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
R7	R6	R5	R4	R3	R2	R1	R0

Function	Register Type	Operand	Data	Notes
Max Row Error Address R[7:0]	R	OP[7:0]	Contains 8 bits of the row address with the highest error count	1
NOTE 1 MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR14 through MR20 transparency data				

3.5.19 MR17 (MA [7:0] = 11_H) - Row Address with Max Errors 2

MR17 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
R15	R14	R13	R12	R11	R10	R9	R8

Function	Register Type	Operand	Data	Notes
Max Row Error Address R[15:8]	R	OP[7:0]	Contains 8 bits of the row address with the highest error count	1
NOTE 1 MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR14 through MR20 transparency data				

3.5.20 MR18 (MA [7:0] = 12_H) - Row Address with Max Errors 3

MR18 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	BG2	BG1	BG0	BA1	BA0	R17	R16

Function	Register Type	Operand	Data	Notes
Max Row Error Address BG[2:0],BA[1,0], R[17,16]	R	OP[6:0]	Contains 7 bits of the row address with the highest error count	1, 2, 3, 4, 5
RFU	RFU	OP[7]	RFU	
NOTE 1 MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR14 through MR20 transparency data. NOTE 2 BG2 is don't care for x16. NOTE 3 BA1 is don't care for 8 Gb. NOTE 4 R16 is don't care for 8 Gb and 16 Gb. NOTE 5 R17 is don't care for 8 Gb, 16 Gb, 24 Gb, and 32 Gb.				

3.5.21 MR19 (MA [7:0] = 13_H) - Max Row Error Count

MR19 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PASR	RFU	REC5	REC4	REC3	REC2	REC1	REC0

Function	Register Type	Operand	Data	Notes
Max Row Error Count REC[5:0]	R	OP[5:0]	Contains number of errors within the row with the most errors	1
RFU	RFU	OP[6]	RFU	
PASR	R	OP[7]	0 = PASR not supported 1 = PASR supported	2

NOTE 1 MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR14 through MR20 transparency data.
NOTE 2 Support of PASR has been deprecated starting with spec working revision 1.90 of JESD79-5C-v1.30.

3.5.22 MR20 (MA [7:0] = 14_H) - Error Count (EC)

MR20 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

Function	Register Type	Operand	Data	Notes
Error Count EC[7:0]	R	OP[7:0]	Contains the error count range data	1

NOTE 1 MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR14 through MR20 transparency data.

3.5.23 MR21 (MA [7:0] = 15_H) - Rx CTLE Control Setting (DQS)

MR21 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	RFU	Rx DQS CTLE Control (Optional)		

Function	Register Type	Operand	Data	Notes
Rx DQS CTLE Control (Optional)	W	OP[2:0]	000B: Vendor Optimized Setting (Default) 001B: Vendor defined 010B: Vendor defined 011B: Vendor defined 100B: Vendor defined 101B: Vendor defined 110B: Vendor defined 111B: Vendor defined	1, 2, 3, 4, 5
RFU	RFU	OP[7:3]	RFU	

NOTE 1 Rx CTLE is an optional feature on DDR5. It may be needed for DRAMs that operate at >=6000Mbps. MR22:OP[3] indicates host whether Rx CTLE is supported or not.
NOTE 2 Refer to the vendor data sheets for more information regarding Rx CTLE Control Settings.
NOTE 3 Since CTLE circuits can not be typically bypassed, a disable option is not provided. Instead, a vendor optimized setting is given. It should be noted that the settings are not specifically linear in relationship to the vendor optimized setting, so the host may opt to instead walk through all the provided options and use the setting that works best in their environment.
NOTE 4 The host can step through all possible combinations of MR bit allocation and choose the settings that is best optimized for the system based on the performance metric of interest.
NOTE 5 MR21:OP[2:0] controls both upper and lower DQS (U/LDQS) for X16 DRAMs.

3.5.24 MR22 (MA [7:0] = 16_H) - MBIST/mPPR Transparency, Rx CTLE Control Setting (Support Indicator, CA, and CS_n)

MR22 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Rx CS_n CTLE Control (Optional)		Rx CA CTLE Control (Optional)		Rx CTLE Support	MBIST/mPPR Transparency (Optional)		

Function	Register Type	Operand	Data	Notes
MBIST/mPPR Transparency (Optional)	R	OP[2:0]	000B: MBIST hasn't run since INIT OR no fails remain after most recent run (Default)	1, 2
			001B: Fails remain	2
			010B: Unrepairable fails remain	2
			011B: MBIST should be run again	2
			100B-111B: Reserved	2
Rx CTLE Support	R	OP[3]	0B: Rx CTLE not supported 1B: Rx CTLE supported	3
Rx CA CTLE Control	R/W	OP[5:4]	00B: Vendor Optimized Setting (Default) 01B: Vendor defined 10B: Vendor defined 11B: Vendor defined	3, 4, 5, 6
Rx CS CTLE Control	R/W	OP[7:6]	00B: Vendor Optimized Setting (Default) 01B: Vendor defined 10B: Vendor defined 11B: Vendor defined	3, 4, 5, 6

NOTE 1 The host should track whether MBIST has run since INIT. If MBIST is run and finds no fails, this transparency state will remain set to 000_B.
NOTE 2 MR14:OP[3:0] must be programmed by MRW to indicate which slice in the 3DS-DDR5 stack is referenced by the MRR for reading MR22 MBIST transparency data.
NOTE 3 Rx CTLE is an optional feature on DDR5. It may be needed for DRAMs that operate at >=6000Mbps. MR22:OP[3] indicates host whether Rx CTLE is supported or not.
NOTE 4 Refer to the vendor data sheets for more information regarding Rx CTLE Control Settings.
NOTE 5 Since CTLE circuits can not be typically bypassed, a disable option is not provided. Instead, a vendor optimized setting is given. It should be noted that the settings are not specifically linear in relationship to the vendor optimized setting, so the host may opt to instead walk through all the provided options and use the setting that works best in their environment.
NOTE 6 The host can step through all possible combinations of MR bit allocation and choose the settings that is best optimized for the system based on the performance metric of interest.

3.5.25 MR23 (MA [7:0] = 17_H) - MBIST/PPR Settings

MR23 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		RFU	MBIST (Optional)	mPPR (Optional)	sPPR		hPPR

Function	Register Type	Operand	Data	Notes
hPPR	R/W	OP[0]	0B: Disable 1B: Enable	1
sPPR	R/W	OP[1]	0B: Disable 1B: Enable See OP[2] for definition with sPPR Undo/Lock Implemented	1
	SR/W	OP[2]	DRAM Status Read (SR): 0B: Not Implemented (Default) 1B: sPPR Undo/Lock Implemented Host Write (W) for OP[2:1] 00B: Disabled (Normal Operation) 01B: sPPR Enabled 10B: sPPR Undo Enabled 11B: sPPR Lock Enabled	
mPPR	W	OP[3]	0B: Disable 1B: Enable (Optional)	1
MBIST	SR/W	OP[4]	DRAM Status Read (SR): 0B: No MBIST/mPPR Support 1B: Supports MBIST/mPPR (Optional) Host Write (W): 0B: MBIST Disabled 1B: MBIST Enable	1,2
RFU	RFU	OP[7:5]	RFU	

NOTE 1 Only one of these opcode bits may be programmed by the host to 1 at any given time. If any one of these opcode bits are enabled, the remaining bits must be programmed to 0.
NOTE 2 DRAM will automatically write to 0 when MBIST completes. Therefore, the host is not required to program to zero before performing MBIST again.
NOTE 3 For 3DS-DDR5 devices, MBIST Enable (MR23:OP[4]=1) is only enabled on the target logical rank designated by CID[3:0] and programmed by MRW via MR14:OP[3:0].

3.5.26 MR24 (MA [7:0] = 18_H) - PPR Guard Key

MR24 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PPR Guard Key							

Function	Register Type	Operand	Data	Notes
PPR Guard Key	W	OP[7:0]	See PPR Section for Sequence	

3.5.27 MR25 (MA[7:0]=19_H) - Read Training Mode Settings

MR25 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				Continuous Burst Mode	LFSR1 Pattern Option	LFSR0 Pattern Option	Read Training Pattern Format

Function	Register Type	Operand	Data	Notes
Read Training Pattern Format	R/W	OP[0]	0B: Serial 1B: LFSR	
LFSR0 Pattern Option	R/W	OP[1]	0B: LFSR 1B: Clock	
LFSR1 Pattern Option	R/W	OP[2]	0B: LFSR 1B: Clock	
Continuous Burst Mode	R/W	OP[3]	0B: MRR command based (Default) 1B: Continuous Burst Output	
RFU	RFU	OP[7:4]	RFU	

3.5.28 MR26 (MA[7:0]=1A$_H$) - Read Pattern Data0 / LFSR0

MR26 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Read Training Pattern Data0 / LFSR0 Seed							

Function	Register Type	Operand	Data	Notes
Read Pattern / LFSR Seed UI 0	R/W	OP[0]	UI<7:0> data for serial mode, LFSR0 seed for LFSR mode	1
Read Pattern / LFSR Seed UI 1	R/W	OP[1]		
Read Pattern / LFSR Seed UI 2	R/W	OP[2]		
Read Pattern / LFSR Seed UI 3	R/W	OP[3]		
Read Pattern / LFSR Seed UI 4	R/W	OP[4]		
Read Pattern / LFSR Seed UI 5	R/W	OP[5]		
Read Pattern / LFSR Seed UI 6	R/W	OP[6]		
Read Pattern / LFSR Seed UI 7	R/W	OP[7]		
NOTE 1 The default value for the **Read Training Pattern Data0/LFSR0** register setting is: 0x5A.				

3.5.29 MR27 (MA[7:0]=1B$_H$) - Read Pattern Data1 / LFSR1

MR27 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Read Training Pattern Data1 / LFSR1 Seed							

Function	Register Type	Operand	Data	Notes
Read Pattern / LFSR Seed UI 8	R/W	OP[0]	UI<15:8> data for serial mode, LFSR1 seed for LFSR mode	1
Read Pattern / LFSR Seed UI 9	R/W	OP[1]		
Read Pattern / LFSR Seed UI 10	R/W	OP[2]		
Read Pattern / LFSR Seed UI 11	R/W	OP[3]		
Read Pattern / LFSR Seed UI 12	R/W	OP[4]		
Read Pattern / LFSR Seed UI 13	R/W	OP[5]		
Read Pattern / LFSR Seed UI 14	R/W	OP[6]		
Read Pattern / LFSR Seed UI 15	R/W	OP[7]		
NOTE 1 The default value for the Read Training Pattern Data1/LFSR1 register setting is: 0x3C.				

3.5.30 MR28 (MA[7:0]=1C$_H$) - Read Pattern Invert DQL7:0 (DQ7:0)

MR28 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Read Training Pattern Invert DQL7:0 (DQ7:0)							

Function	Register Type	Operand	Data	Notes
DQ Invert (Lower DQ Bits)	R/W	OP[0]	DQL0 (DQ0) 0B: Normal 1B: Invert	1
	R/W	OP[1]	DQL1 (DQ1) 0B: Normal 1B: Invert	
	R/W	OP[2]	DQL2 (DQ2) 0B: Normal 1B: Invert	
	R/W	OP[3]	DQL3 (DQ3) 0B: Normal 1B: Invert	
	R/W	OP[4]	DQL4 (DQ4) 0B: Normal 1B: Invert	
	R/W	OP[5]	DQL5 (DQ5) 0B: Normal 1B: Invert	
	R/W	OP[6]	DQL6 (DQ6) 0B: Normal 1B: Invert	
	R/W	OP[7]	DQL7 (DQ7) 0B: Normal 1B: Invert	

NOTE 1 The default value for the **Read Training Pattern Invert DQL7:0 (DQ7:0)** register setting is: 0x00.

3.5.31 MR29 (MA[7:0]= D_H) - Read Pattern Invert DQU7:0 (DQ15:8)

MR29 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Read Training Pattern Invert DQU7:0 (DQ15:8)							

Function	Register Type	Operand	Data	Notes
DQ Invert (Upper DQ Bits)	R/W	OP[0]	DQU0 (DQ8) 0B: Normal 1B: Invert	1
	R/W	OP[1]	DQU1 (DQ9) 0B: Normal 1B: Invert	
	R/W	OP[2]	DQU2 (DQ10) 0B: Normal 1B: Invert	
	R/W	OP[3]	DQU3 (DQ11 0B: Normal 1B: Invert	
	R/W	OP[4]	DQU4 (DQ12) 0B: Normal 1B: Invert	
	R/W	OP[5]	DQLU5 (DQ13) 0B: Normal 1B: Invert	
	R/W	OP[6]	DQU6 (DQ14) 0B: Normal 1B: Invert	
	R/W	OP[7]	DQU7 (DQ15) 0B: Normal 1B: Invert	

NOTE 1 The default value for the **Read Training Pattern Invert DQU7:0 (DQ15:8)** register setting is: 0x00.

3.5.32 MR30 (MA[7:0]=1E$_H$) - Read LFSR Assignments

MR30 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
LFSR Assignment DQL7/ DQU7	LFSR Assignment DQL6/ DQU6	LFSR Assignment DQL5/ DQU5	LFSR Assignment DQL4/ DQU4	LFSR Assignment DQL3/ DQU3	LFSR Assignment DQL2/ DQU2	LFSR Assignment DQL1/ DQU1	LFSR Assignment DQL0/ DQU0

Function	Register Type	Operand	Data	Notes
LFSR Assignment DQL0/DQU0	R/W	OP[0]	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**	1
LFSR Assignment DQL1/DQU1	R/W	OP[1]	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**	
LFSR Assignment DQL2/DQU2	R/W	OP[2]	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**	
LFSR Assignment DQL3/DQU3	R/W	OP[3]	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**	
LFSR Assignment DQL4/DQU4	R/W	OP[4]	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**	
LFSR Assignment DQL5/DQU5	R/W	OP[5]	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**	
LFSR Assignment DQL6/DQU6	R/W	OP[6]	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**	
LFSR Assignment DQL7/DQU7	R/W	OP[7]	NOTE 10B: Read Pattern Data0/LFSR0 1B: Read Pattern Data1/LFSR1	
NOTE 1 The default value for the **Read LFSR Assignments** register setting is: 0xFE.				

3.5.33 MR31 (MA[7:0]=1F$_H$) - Read Training Pattern Address

MR31 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Read Training Pattern Address							

Function	Register Type	Operand	Data	Notes
Read Training Pattern Address	R	OP[7:0]	This MR address is reserved. There are no specific register fields associated with this address. In response to the MRR to this address the DRAM shall send the BL16 read training pattern. All 8 bits associated with this MR address are reserved.	

3.5.34 MR32 (MA[7:0]=20H) - CK and CS ODT

MR32 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	CA_ODT Strap Value	CS ODT			CK ODT		

Function	Register Type	Operand	Data	Notes
CK ODT	R	OP[2:0]	000_B: RTT_OFF (Disable) Group A default 001_B: RZQ/0.5 (480) 010_B: RZQ/1 (240) 011_B: RZQ/2 (120) 100_B: RZQ/3 (80) 101_B: RZQ/4 (60) 110_B: RFU 111_B: RZQ/6 (40) Group B default	1, 2
CS ODT	R	OP[5:3]	000_B: RTT_OFF (Disable) Group A default 001_B: RZQ/0.5 (480) 010_B: RZQ/1 (240) 011_B: RZQ/2 (120) 100_B: RZQ/3 (80) 101_B: RZQ/4 (60) 110_B: RFU 111_B: RZQ/6 (40) Group B default	1, 2
CA_ODT Strap Value	R	OP[6]	0_B: Strap Configured to Group A 1_B: Strap Configured to Group B	3
RFU	RFU	OP[7]	RFU	

NOTE 1 This mode register is programmed via an explicit MPC command only.
NOTE 2 CK ODT RZQ/2 (120 Ω) and CS ODT RZQ/2 (120 Ω) are only supported at >5200 MT/s data rates.
NOTE 3 Strapping for ODT on Command and Address. The DRAM applies to Group A settings if the CA_ODT pin is connected to VSS and applies Group B settings if the pin is connected to VDD. This MR is used to confirm the DRAM's setting for that config.

3.5.35 MR33 (MA[7:0]=21H) - CA and DQS_PARK ODT

MR33 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		DQS_RTT_PARK			CA ODT		

Function	Register Type	Operand	Data	Notes
CA ODT	R	OP[2:0]	000B: RTT_OFF (Disable) Group A default 001B: RZQ/0.5 (480) 010B: RZQ/1 (240) 011B: RZQ/2 (120) 100B: RZQ/3 (80) Group B default 101B: RZQ/4 (60) 110B: RFU 111B: RZQ/6 (40)	1,2
DQS_RTT_PARK	R	OP[5:3]	000B: RTT_OFF default 001B: RZQ (240) 010B: RZQ/2 (120) 011B: RZQ/3 (80) 100B: RZQ/4 (60) 101B: RZQ/5 (48) 110B: RZQ/6 (40) 111B: RZQ/7 (34)	1
RFU	RFU	OP[7:6]	RFU	

NOTE 1 This mode register is programmed via an explicit MPC command only.
NOTE 2 CA ODT RZQ/2 (120Ω) is only supported at >5200 MT/s data rates.

3.5.36 MR34 (MA[7:0]=22_H) - RTT_PARK and RTT_WR

MR34 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		RTT_WR			RTT_PARK		

Function	Register Type	Operand	Data	Notes
RTT_PARK	R	OP[2:0]	000_B: RTT_OFF default 001_B: RZQ (240) 010_B: RZQ/2 (120) 011_B: RZQ/3 (80) 100_B: RZQ/4 (60) 101_B: RZQ/5 (48) 110_B: RZQ/6 (40) 111_B: RZQ/7 (34)	1
RTT_WR	R/W	OP[5:3]	000_B: RTT_OFF 001_B: RZQ (240) default 010_B: RZQ/2 (120) 011_B: RZQ/3 (80) 100_B: RZQ/4 (60) 101_B: RZQ/5 (48) 110_B: RZQ/6 (40) 111_B: RZQ/7 (34)	
RFU	RFU	OP[7:6]	RFU	

NOTE 1 This mode register is programmed via an explicit MPC command only.

3.5.37 MR35 (MA[7:0]=23_H) - RTT_NOM_WR and RTT_NOM_RD

MR35 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		RTT_NOM_RD			RTT_NOM_WR		

Function	Register Type	Operand	Data	Notes
RTT_NOM_WR	R/W	OP[2:0]	000B: RTT_OFF 001B: RZQ (240) 010B: RZQ/2 (120) 011B: RZQ/3 (80) default 100B: RZQ/4 (60) 101B: RZQ/5 (48) 110B: RZQ/6 (40) 111B: RZQ/7 (34)	
RTT_NOM_RD	R/W	OP[5:3]	000B: RTT_OFF 001B: RZQ (240) 010B: RZQ/2 (120) 011B: RZQ/3 (80) default 100B: RZQ/4 (60) 101B: RZQ/5 (48) 110B: RZQ/6 (40) 111B: RZQ/7 (34)	
RFU	RFU	OP[7:6]	RFU	

3.5.38 MR36 (MA[7:0]=24_H) - RTT Loopback

MR36 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU					RTT Loopback		

Function	Register Type	Operand	Data	Notes
RTT Loopback	R/W	OP[2:0]	000B: RTT_OFF Default 001B: RFU 010B: RFU 011B: RFU 100B: RFU 101B: RZQ/5 (48) 110B: RFU 111B: RFU	1, 2
RFU	RFU	OP[7:3]	RFU	

NOTE 1 When Loopback is disabled, both LBDQS and LBDQ pins are either at HiZ or Termination Mode this configuration. When Loopback is enabled, it is in driver mode.

3.5.39 MR37 (MA[7:0]= 25_H) - ODTL Write Control Offset

MR37 Register Information

This byte is setup to allow the host controller to push out or pull in the Write RTT enable time (tODTLon_WR) or the Write RTT disable time (tODTLoff_WR) outside of the default setting. The default state is based on internal DRAM design and is defined in Table 184 in the ODT Configuration section. The DRAM is not responsible for inappropriate states set by the host controller using this register.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		ODTLoff_WR_Offset			ODTLon_WR_Offset		

Function	Register Type	Operand	Data	Notes
ODTLon_WR_Offset	R/W	OP[2:0]	000B: RFU 001B: -4 Clocks 010B: -3 Clocks 011B: -2 Clocks 100B: -1 Clock - Default 101B: 0 Clock 110B: +1 Clock 111B: +2 Clocks	1
ODTLoff_WR_Offset	R/W	OP[5:3]	000B: RFU 001B: +4 Clocks 010B: +3 Clocks 011B: +2 Clocks 100B: +1 Clock 101B: 0 Clock - Default 110B: -1 Clock 111B: -2 Clocks	1
RFU	RFU	OP[7:6]	RFU	

NOTE 1 The Write ODTLon -4 offset and ODTLoff +4 offset is not allowed for 1980-2100 data rates.

3.5.40 MR38 (MA[7:0]=26_H) - ODTL NT Write Control Offset

MR38 Register Information

This byte is setup to allow the host controller to push out or pull in the Non-Target Write RTT enable time (tODTLon_WR_NT) or the Non-Target Write RTT disable time (tODTLoff_WR_NT) outside of the default setting. The default state is based on internal DRAM design and is defined in Table 184 in the ODT Configuration section. The DRAM is not responsible for inappropriate states set by the host controller using this register.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		ODTLoff_WR_NT_Offset			ODTLon_WR_NT_Offset		

Function	Register Type	Operand	Data	Notes
ODTLon_WR_NT_Offset	R/W	OP[2:0]	000B: RFU 001B: -4 Clocks 010B: -3 Clocks 011B: -2 Clocks 100B: -1 Clock - Default 101B: 0 Clock 110B: +1 Clock 111B: +2 Clocks	1
ODTLoff_WR_NT_Offset	R/W	OP[5:3]	000B: RFU 001B: +4 Clocks 010B: +3 Clocks 011B: +2 Clocks 100B: +1 Clock 101B: 0 Clock - Default 110B: -1 Clock 111B: -2 Clocks	1
RFU	RFU	OP[7:6]	RFU	

NOTE 1 The Write NT ODTLon -4 offset and ODTLoff +4 offset is not allowed for 1980-2100 data rates.

3.5.41 MR39 (MA[7:0]=27_H) - ODTL NT Read Control Offset

MR39 Register Information

This byte is setup to allow the host controller to push out or pull in the Non-Target Read RTT enable time (tODTLon_RD_NT) or the Non-Target Read RTT disable time (tODTLoff_RD_NT) outside of the default setting. The default state is based on internal DRAM design and is defined in Table 184 in the ODT Configuration section. The DRAM is not responsible for inappropriate states set by the host controller using this register.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		ODTLoff_RD_NT_Offset			ODTLon_RD_NT_Offset		

Function	Register Type	Operand	Data	Notes
ODTLon_RD_NT_Offset	R/W	OP[2:0]	000_B: RFU 001_B: RFU 010_B: -3 Clocks 011_B: -2 Clocks 100_B: -1 Clock - Default 101_B: 0 Clock 110_B: +1 Clock 111_B: RFU	
ODTLoff_RD_NT_Offset	R/W	OP[5:3]	000_B: RFU 001_B: RFU 010_B: +3 Clocks 011_B: +2 Clocks 100_B: +1 Clock 101_B: 0 Clock - Default 110_B: -1 Clock 111_B: RFU	
RFU	RFU	OP[7:6]	RFU	

3.5.42 MR40 (MA[7:0]=28_H) - Read DQS Offset Timing

MR40 Register Information

This byte is used for configuring the DRAM to support different HOST receiver designs.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU					Read DQS offset timing		

Function	Register Type	Operand	Data	Notes
Read DQS offset timing	R/W	OP[2:0]	000_B: 0 Clock (DEFAULT) 001_B: 1 Clock 010_B: 2 Clocks 011_B: 3 Clocks 100_B: RFU 101_B: RFU 110_B: RFU 111_B: RFU	
RFU	RFU	OP[7:3]	RFU	
NOTE 1 When operating at low speed (CL <= 30), tRPRE + Read DQS Offset >= 5 Clocks cannot be supported.				

	tRPRE \ DQS Offset	0	1	2	3
When CL <= 30	1	O	O	O	O
	2	O	O	O	X
	3	O	O	X	X
	4	O	X	X	X

3.5.43 MR41 (MA[7:0]=29_H) - RFU

MR41 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU							

Function	Register Type	Operand	Data	Notes

3.5.44 MR42 (MA[7:0]=2A$_H$) - DCA Types Supported

MR42 Register Information

This byte is used for configuring DCA

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DCA Training Assist Mode II (Optional)				DCA Training Assist Mode I		DCA Types Supported	

MR42 Table

Function	Register Type	Operand	Data	Notes
DCA Types Supported	R	OP[1:0]	00_B: Device does not support DCA 01_B: Device supports DCA for single/two-phase internal clock(s) 10_B: Device supports DCA for 4-phase internal clocks 11_B: RFU	
DCA Training Assist Mode I	R/W	OP[3:2]	00_B: Disable (default) 01_B: MRR (or Read) synchronized with IBCLK is blocked 10_B: MRR (or Read) synchronized with ICLK is blocked 11_B: RFU	1, 2, 3, 4, 5, 6, 9
DCA Training Assist Mode II (Optional)	R/W	OP[6:4]	000_B: Disable (default) 001_B: DQ fires 0001 data pattern 010_B: DQ fires 0011 data pattern 011_B: DQ fires 0111 data pattern 100_B: DQ fires 1000 data pattern 101_B: DQ fires 1100 data pattern 110_B: DQ fires 1110 data pattern 111_B: RFU	3, 4, 5, 7, 8, 9, 10,11
	SR/W	OP[7]	DRAM Status Read (SR) 0_B: DCA Training Assist Mode II is not supported 1_B: DCA Training Assist Mode II is supported Host Write (W): 0_B: MRR based (Default) 1_B: Continuous Burst output	

MR42 Table (cont'd)

NOTE 1	When "MRR (or Read) synchronized with IBCLK is blocked" is set by MR42 OP[3:2]=01b, DQs caused by MRR (or Read) synchronized with IBCLK are driven HIGH.
NOTE 2	When "MRR (or Read) synchronized with ICLK is blocked" is set by MR42 OP[3:2]=10b, DQs caused by MRR (or Read) synchronized with ICLK are driven HIGH.
NOTE 3	DQS_t/DQS_c output normal toggling waveforms meaning that DQS_t/DQS_c are not affected by the settings of DCA Assist Mode MR42 OP[3:2].
NOTE 4	The CRC function is not supported during DCA Training Assist Mode.
NOTE 5	DCA Training Assist Mode is only supported by DRAMs with DCAs that have 4-phase internal clocks
NOTE 6	If MR42:OP[3:2] is set to either 01B or 10B, odd-gap READ or odd-gap Mode Register Read Pattern commands should follow the tMRR timing spec.
NOTE 7	The MRR based mode of DCA Training Assist Mode II is enabled when the host sets MR42 OP[6:4]≠000 & OP[7]=0. DRAM will provide selected predefined pattern when the host issues MRR to MR42 command to the DRAM. For MRR, issuing any MRR other than to MR42 is invalid and may result in unexpected DQ behavior, requiring the host to issue a Reset to exit MRR based mode and restart the training with an MRR to MR42.The returned data will be a predefined pattern instead of the contents of a mode register. The timing of the read data return is the same as for an MRR command, including the operation of the strobes (DQS_t, DQS_c). The host can issue MRW to MR42:OP[6:4]≠000_B to change data pattern during MRR based mode. The host needs to issue MRW to MR42:OP[6:4]=000_B to exit the MRR based mode.
NOTE 8	Continuous burst output mode is available for DCA Training Assist Mode II and is enabled with MRW to MR42 OP[6:4]≠000_B & OP[7]=1. Once this mode is enabled, MRR to MR42 will start the pattern output and will automatically continue to output the appropriate pattern until it is stopped by either a system reset or issuing an MRW MR42 OP[7]=0 command that reverts it to the "MRR based (Default)" mode. Issuing any MRR other than to MR42 is invalid and may result in unexpected DQ behavior, requiring the host to issue a Reset to exit continuous burst output mode and restart the training with an MRR to MR42. Once the MR42 OP[7]=0 "MRR based (Default)" is registered by the DRAM, it will stop all pattern traffic by tCont_Exit. Since there is no min time for tCont_Exit, the DRAM may stop the pattern prior to tCont_Exit, potentially truncating any current burst pattern. To ensure that the DRAM's state-machine doesn't get into some meta-stability while turning off the output pattern, the host must issue a second MR42 OP[7]=0 "MRR based (Default)" after waiting tMRR, which will then start tCont_Exit_delay. After tCont_Exit_delay has expired, any other valid command is then legal. Issuing any MRW other than MRW to MR 42 OP[7]=0 during Continuous Burst Mode after predefined pattern output started is invalid and may result in unexpected DQ behavior, requiring the host to issue a Reset to exit continuous burst output mode and restart the training with an MRR to MR 42
NOTE 9	The DCA Training Assist Mode I and II can not be enabled at the same time by the host. That is, while the DCA Training Assist Mode II is enabled, the DCA Training Assist Mode I shall be disabled by Host and vice versa.
NOTE 10	Depending on relationship of internal clocks and MRR command, DRAM may start outputting from the 3rd bit of data pattern. The data pattern is defined with ICLK bases (1st=ICLK, 2nd=QCLK, 3rd=IBCLK and 4th=QBCLK), but MRR burst may start from IBCLK.
NOTE 11	In DCA Assist Mode II, MRR to MR42 outputs the repetitive data pattern through all DQ bits for a 16-bit burst. For example, if MR42:OP[7:4]=0010B, and MRR to MR42 is issued, all DQs output the same 0011001100110011 data pattern.

3.5.45 MR43 (MA[7:0]=2B$_H$) - DCA Settings 1

MR43 Register Information

This byte is used for configuring DCA

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Sign Bit for OP[6:4]	DCA for IBCLK in 4-phase clocks			Sign Bit for OP[2:0]	DCA for single/two-phase clock(s) or QCLK in 4-phase clocks		

Function	Register Type	Operand	Data	Notes
DCA for single/two-phase clock(s) or QCLK in 4-phase clocks	W	OP[2:0]	000_B: DCA step +0 (default) 001_B: DCA step +1 010_B: DCA step +2 011_B: DCA step +3 100_B: DCA step +4 101_B: DCA step +5 110_B: DCA step +6 111_B: DCA step +7	1
Sign Bit for OP[2:0]	W	OP[3]	0_B: Positive Offset (default) 1_B: Negative Offset	1
DCA for IBCLK in 4-phase clocks	W	OP[6:4]	000_B: DCA step +0 (default) 001_B: DCA step +1 010_B: DCA step +2 011_B: DCA step +3 100_B: DCA step +4 101_B: DCA step +5 110_B: DCA step +6 111_B: DCA step +7	2
Sign Bit for OP[6:4]	W	OP[7]	0_B: Positive Offset (default) 1_B: Negative Offset	2

NOTE 1 These settings can only be applied if MR42:OP[1:0] =**01_B** or 1**0_B**.
NOTE 2 These settings can only be applied if MR42:OP[1:0] =1**0_B**.

3.5.46 MR44 (MA[7:0]=2C$_H$) - DCA Settings 2

MR44 Register Information

This byte is used for configuring DCA

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				Sign Bit for QBCLK in 4-phase clocks	DCA for QBCLK in 4-phase clocks		

Function	Register Type	Operand	Data	Notes
DCA for QBCLK in 4-phase clocks	W	OP[2:0]	000B: DCA step +0 (default) 001B: DCA step +1 010B: DCA step +2 011B: DCA step +3 100B: DCA step +4 101B: DCA step +5 110B: DCA step +6 111B: DCA step +7	1
Sign Bit for QBCLK in 4-phase clocks	W	OP[3]	0B: Positive Offset (default) 1B: Negative Offset	1
RFU	RFU	OP[7:4]	RFU	

NOTE 1 These settings can only be applied if MR42 OP[1:0]=10$_B$.

3.5.47 MR45 (MA[7:0]=2D$_H$) - DQS Interval Control

MR45 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Interval Timer Run Time							

Function	Register Type	Operand	Data	Notes
DQS Interval Timer Run Time	W	OP[7:0]	0000 0000B: DQS interval timer stop via MPC Command (Default) 0000 0001B: DQS timer stops automatically at 16th clocks after timer start 0000 0010B: DQS timer stops automatically at 32nd clocks after timer start 0000 0011B: DQS timer stops automatically at 48th clocks after timer start 0000 0100B: DQS timer stops automatically at 64th clocks after timer start ---------- Thru ---------- 0011 1111B: DQS timer stops automatically at (63X16)th clocks after timer start 01XX XXXXB: DQS timer stops automatically at 2048th clocks after timer start 10XX XXXXB: DQS timer stops automatically at 4096th clocks after timer start 11XX XXXXB: DQS timer stops automatically at 8192nd clocks after timer start	1, 2

NOTE 1 MPC command with OP[7:0]=0000 0110$_B$ (Stop DQS Interval Oscillator) stops DQS interval timer in case of MR45:OP[7:0] = 00000000$_B$.

NOTE 2 MPC command with OP[7:0]=0000 0110$_B$ (Stop DQS Interval Oscillator) is illegal with non-zero values in MR45:OP[7:0].

3.5.48 MR46 (MA[7:0]=2E$_H$) - DQS Osc Count - LSB

MR46 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Oscillator Count - LSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator Count - LSB	R	OP[7:0]	0 - 255 LSB DRAM DQS Oscillator Count	

NOTE 1 MR46 reports the LSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.

NOTE 2 Both MR46 and MR47 must be read (MRR) and combined to get the value of the DQS Oscillator count.

NOTE 3 A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR46/MR47.

3.5.49 MR47 (MA[7:0]=2F$_H$) - DQS Osc Count - MSB

MR47 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Oscillator Count - MSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator Count - MSB	R	OP[7:0]	0 - 255 MSB DRAM DQS Oscillator Count	

NOTE 1 MR47 reports the MSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.

NOTE 2 Both MR46 and MR47 must be read (MRR) and combined to get the value of the DQS Oscillator count.

NOTE 3 A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR46/MR47.

3.5.50 MR48 (MA[7:0]=30_H) - Write Pattern Mode

MR48 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Write Pattern Mode							

Function	Register Type	Operand	Data	Notes
DQL0/DQU0	R/W	OP[0]	Valid	1, 2
DQL1/DQU1	R/W	OP[1]		
DQL2/DQU2	R/W	OP[2]		
DQL3/DQU3	R/W	OP[3]		
DQL4/DQU4	R/W	OP[4]		
DQL5/DQU5	R/W	OP[5]		
DQL6/DQU6	R/W	OP[6]		
DQL7/DQU7	R/W	OP[7]		

NOTE 1 OP[7:0] can be independently programmed with either “0” or “1”.
NOTE 2 Default is all zeros for OP[7:0]

3.5.51 MR50 (MA[7:0]=32_H) - Write CRC Settings

MR50 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	Write CRC auto-disable status	Write CRC auto-dis-able enable	Write CRC error status	Write CRC enable upper nibble	Write CRC enable lower nibble	Read CRC enable

Function	Register Type	Operand	Data	Notes
Read CRC enable	R/W	OP[0]	0B: Disable (Default) 1B: Enable	
Write CRC enable lower nibble	R/W	OP[1]	0B: Disable (Default) 1B: Enable	1
Write CRC enable upper nibble	R/W	OP[2]	0B: Disable (Default) 1B: Enable	1
Write CRC error status	R/W	OP[3]	0B: Clear 1B: Error	2
Write CRC auto-disable enable	R/W	OP[4]	0B: Disable (Default) 1B: Enable	
Write CRC auto-disable status	R/W	OP[5]	0B: Not triggered 1B: Triggered	
RFU	RFU	OP[6]	RFU	
RFU	RFU	OP[7]	RFU	

NOTE 1 When at least one of the two write CRC enable bits is set to '1' in x8, the timing of write CRC enable mode is applied to the entire device (i.e. both nibbles). When write CRC is enabled in one nibble and disabled in the other nibble in x8, then the DRAM does not check CRC errors on the disabled nibble, and hence the ALERT_n signal and any internal status bit related to CRC error is not impacted by the disabled nibble.

NOTE 2 The host shall disable Write CRC, if it was enabled, prior to entering Write Leveling Training mode.

3.5.52 MR51 (MA[7:0]=33_H) - Write CRC Auto-Disable Threshold

MR51 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]

Function	Register Type	Operand	Data	Notes
Write CRC auto-disable threshold	R/W	OP[6:0]	0000000B: 0 ... 1111111B: 127	
RFU	RFU	OP[7]	RFU	

3.5.53 MR52 (MA[7:0]=34_H) - Write CRC Auto-Disable Window

MR52 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]

Function	Register Type	Operand	Data	Notes
Write CRC auto-disable window	R/W	OP[6:0]	0000000B: 0 ... 1111111B: 127	
RFU	RFU	OP[7]	RFU	

3.5.54 MR53 (MA[7:0]=35_H) - Loopback

MR53 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Loopback Output Mode	Loopback Select Phase		Loopback Output Select				

Function	Register Type	Operand	Data	Notes
Loopback Output Select	R/W	OP[4:0]	00000B: Loopback Disabled (Default) 00001B: Loopback DML (X8 and X16 only) 00010B: Loopback DMU (X16 only) 00011B: Vendor Specific 00100B: Vendor Specific 00101B: RFU ...thru 01111B: RFU 10000B: Loopback DQL0 10001B: Loopback DQL1 10010B: Loopback DQL2 10011B: Loopback DQL3 10100B: Loopback DQL4 (X8 and X16 only) 10101B: Loopback DQL5 (X8 and X16 only) 10110B: Loopback DQL6 (X8 and X16 only) 10111B: Loopback DQL7 (X8 and X16 only) 11000B: Loopback DQU0 (X16 only) 11001B: Loopback DQU1 (X16 only) 11010B: Loopback DQU2 (X16 only) 11011B: Loopback DQU3 (X16 only) 11100B: Loopback DQU4 (X16 only) 11101B: Loopback DQU5 (X16 only) 11110B: Loopback DQU6 (X16 only) 11111B: Loopback DQU7 (X16 only)	1, 2, 5
Loopback Select Phase	R/W	OP[6:5]	00B: Loopback Select Phase A 01B: Loopback Select Phase B (4-way and 2-way interleave only) 10B: Loopback Select Phase C (4-way interleave only) 11B: Loopback Select Phase D (4-way interleave only)	3
Loopback Output Mode	R/W	OP[7]	0B: Normal Output (Default) 1B: Write Burst Output	4

NOTE 1 When Loopback is disabled, both LBDQS and LBDQ pins are either at HiZ or Termination Mode per MR36:OP[2:0]. Loopback Termination default value is 48 ohms

NOTE 2 When Loopback is enabled, both LBDQS and LBDQ pins are in driver mode using default RON of 34 ohms

NOTE 3 Phase A through D selects which bit in the multiplexer is being selected for Loopback output

NOTE 4 This configures the DRAM Loopback output to either send data out every time the DQS toggles in Normal Output Mode, or to only send data out when enabled by the Write command, so that only write burst data is send out via Loopback.

NOTE 5 The DM function shall be enabled (MR5:OP[5]=1) when loopback output from the DML or DMU pin is selected for Loopback measurement (MR53:OP[4:0]=00001_B or 00010_B).

3.5.55 MR54 (MA[7:0]=36H) - hPPR Resources

With hPPR, DDR5 can correct one Row address per Bank Group and the Electrical-fuse cannot be switched back to un-fused states once it is programmed. The controller should prevent unintended the hPPR mode entry and repair. (i.e. During the Command/Address training period). Entry into hPPR is through a register enable, ACT command is used to transmit the bank and row address of the row to be replaced in DRAM. After tRCD time, a WR command is used to select the individual DRAM through the DQ bits and to transfer the repair address to the DRAM. After program time, and PRE, the hPPR mode can be exited and normal operation can resume.

MR54 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
hPPR Resource BG1 Bank 3	hPPR Resource BG1 Bank 2	hPPR Resource BG1 Bank 1	hPPR Resource BG1 Bank 0	hPPR Resource BG0 Bank 3	hPPR Resource BG0 Bank 2	hPPR Resource BG0 Bank 1	hPPR Resource BG0 Bank 0

Function	Register Type	Operand	Data	Notes
hPPR Resource BG0 Bank 0	R	OP[0]	0B: hPPR Resource is not available 1B: hPPR Resource is available	3
hPPR Resource BG0 Bank 1		OP[1]	0B: hPPR Resource is not available 1B: hPPR Resource is available	3
hPPR Resource BG0 Bank 2		OP[2]	0B: hPPR Resource is not available 1B: hPPR Resource is available	1, 3
hPPR Resource BG0 Bank 3		OP[3]	0B: hPPR Resource is not available 1B: hPPR Resource is available	1, 3
hPPR Resource BG1 Bank 0		OP[4]	0B: hPPR Resource is not available 1B: hPPR Resource is available	3
hPPR Resource BG1 Bank 1		OP[5]	0B: hPPR Resource is not available 1B: hPPR Resource is available	3
hPPR Resource BG1 Bank 2		OP[6]	0B: hPPR Resource is not available 1B: hPPR Resource is available	1, 3
hPPR Resource BG1 Bank 3		OP[7]	0B: hPPR Resource is not available 1B: hPPR Resource is available	1, 3

NOTE 1 Don't care for 8 Gb.
NOTE 2 Don't care for x16. (This note is not used in the table above but left for consistency across MR54-57 hPPR Resources).
NOTE 3 MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS DDR5 Stack is referenced in the MR54 through MR57 hPPR resource information.

3.5.56 MR55 (MA[7:0]=37H) - hPPR Resources

MR55 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
hPPR Resource BG3 Bank 3	hPPR Resource BG3 Bank 2	hPPR Resource BG3 Bank 1	hPPR Resource BG3 Bank 0	hPPR Resource BG2 Bank 3	hPPR Resource BG2 Bank 2	hPPR Resource BG2 Bank 1	hPPR Resource BG2 Bank 0

Function	Register Type	Operand	Data	Notes
hPPR Resource BG2 Bank 0	R	OP[0]	0B: hPPR Resource is not available 1B: hPPR Resource is available	3
hPPR Resource BG2 Bank 1		OP[1]	0B: hPPR Resource is not available 1B: hPPR Resource is available	3
hPPR Resource BG2 Bank 2		OP[2]	0B: hPPR Resource is not available 1B: hPPR Resource is available	1, 3
hPPR Resource BG2 Bank 3		OP[3]	0B: hPPR Resource is not available 1B: hPPR Resource is available	1, 3
hPPR Resource BG3 Bank 0		OP[4]	0B: hPPR Resource is not available 1B: hPPR Resource is available	3
hPPR Resource BG3 Bank 1		OP[5]	0B: hPPR Resource is not available 1B: hPPR Resource is available	3
hPPR Resource BG3 Bank 2		OP[6]	0B: hPPR Resource is not available 1B: hPPR Resource is available	1, 3
hPPR Resource BG3 Bank 3		OP[7]	0B: hPPR Resource is not available 1B: hPPR Resource is available	1, 3

NOTE 1 Don't care for 8 Gb.

NOTE 2 Don't care for x16. (This note is not used in the table above but left for consistency across MR54-57 hPPR Resources).

NOTE 3 MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS DDR5 Stack is referenced in the MR54 through MR57 hPPR resource information.

3.5.57 MR56 (MA[7:0]=38H) - hPPR Resources

MR56 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
hPPR Resource BG5 Bank 3	hPPR Resource BG5 Bank 2	hPPR Resource BG5 Bank 1	hPPR Resource BG5 Bank 0	hPPR Resource BG4 Bank 3	hPPR Resource BG4 Bank 2	hPPR Resource BG4 Bank 1	hPPR Resource BG4 Bank 0

Function	Register Type	Operand	Data	Notes
hPPR Resource BG4 Bank 0	R	OP[0]	0B: hPPR Resource is not available 1B: hPPR Resource is available	2, 3
hPPR Resource BG4 Bank 1		OP[1]	0B: hPPR Resource is not available 1B: hPPR Resource is available	2, 3
hPPR Resource BG4 Bank 2		OP[2]	0B: hPPR Resource is not available 1B: hPPR Resource is available	1, 2, 3
hPPR Resource BG4 Bank 3		OP[3]	0B: hPPR Resource is not available 1B: hPPR Resource is available	1, 2, 3
hPPR Resource BG5 Bank 0		OP[4]	0B: hPPR Resource is not available 1B: hPPR Resource is available	2, 3
hPPR Resource BG5 Bank 1		OP[5]	0B: hPPR Resource is not available 1B: hPPR Resource is available	2, 3
hPPR Resource BG5 Bank 2		OP[6]	0B: hPPR Resource is not available 1B: hPPR Resource is available	1, 2, 3
hPPR Resource BG5 Bank 3		OP[7]	0B: hPPR Resource is not available 1B: hPPR Resource is available	1, 2, 3

NOTE 1 Don't care for 8Gb.

NOTE 2 Don't care for x16.

NOTE 3 MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS DDR5 Stack is referenced in the MR54 through MR57 hPPR resource information.

3.5.58 MR57 (MA[7:0]=39H) - hPPR Resources

MR57 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
hPPR Resource BG7 Bank 3	hPPR Resource BG7 Bank 2	hPPR Resource BG7 Bank 1	hPPR Resource BG7 Bank 0	hPPR Resource BG6 Bank 3	hPPR Resource BG6 Bank 2	hPPR Resource BG6 Bank 1	hPPR Resource BG6 Bank 0

Function	Register Type	Operand	Data	Notes
hPPR Resource BG6 Bank 0	R	OP[0]	0B: hPPR Resource is not available 1B: hPPR Resource is available	2, 3
hPPR Resource BG6 Bank 1		OP[1]	0B: hPPR Resource is not available 1B: hPPR Resource is available	2, 3
hPPR Resource BG6 Bank 2		OP[2]	0B: hPPR Resource is not available 1B: hPPR Resource is available	1, 2, 3
hPPR Resource BG6 Bank 3		OP[3]	0B: hPPR Resource is not available 1B: hPPR Resource is available	1, 2, 3
hPPR Resource BG7 Bank 0		OP[4]	0B: hPPR Resource is not available 1B: hPPR Resource is available	2, 3
hPPR Resource BG7 Bank 1		OP[5]	0B: hPPR Resource is not available 1B: hPPR Resource is available	2, 3
hPPR Resource BG7 Bank 2		OP[6]	0B: hPPR Resource is not available 1B: hPPR Resource is available	1, 2, 3
hPPR Resource BG7 Bank 3		OP[7]	0B: hPPR Resource is not available 1B: hPPR Resource is available	1, 2, 3

NOTE 1 Don't care for 8 Gb.

NOTE 2 Don't care for x16.

NOTE 3 MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS DDR5 Stack is referenced in the MR54 through MR57 hPPR resource information.

3.5.59 MR58 (MA[7:0]=3A$_H$) - Refresh Management

MR58 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RAAMMT[2:0]			RAAIMT[3:0]				RFM Required

Function	Register Type	Operand	Data	Notes
RFM Required	R	OP[0]	0B: Refresh Management not required 1B: Refresh Management required	1
Rolling Accumulated ACT Initial Management Threshold (RAAIMT)	R	OP[4:1]	0000B- 0011B: RFU 0100B: 32 (Normal), 16 (FGR) 0101B: 40 (Normal), 20 (FGR) ... 1001B: 72 (Normal), 36 (FGR) 1010B: 80 (Normal), 40 (FGR) 1011B-1111B: RFU	1, 2
Rolling Accumulated ACT Maximum Management Threshold (RAAMMT)	R	OP[7:5]	000B-010B: RFU 011B: 3x (Normal), 6x (FGR) 100B: 4x (Normal), 8x (FGR) 101B: 5x (Normal), 10x (FGR) 110B: 6x (Normal), 12x (FGR) 111B: RFU	1, 2

NOTE 1 Refresh Management settings are vendor specific by the MR settings.

NOTE 2 Only applicable if the Refresh Management Required bit is set to “1” (MR58 OP[0]=1)

3.5.60 MR59 (MA[7:0]=3B$_H$) - DRFM, ARFM, RFM RAA Counter

MR59 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFM RAA Counter		ARFM		BRC Suppor Level	Bounded Refresh Configuration		DRFE

Function	Register Type	Operand	Data	Note
DRFM Enable (DRFE)	SR/W	OP[0]	DRAM Status Read (SR): 0B: DRFM not implemented (Default) 1B: DRFM implemented Host Write (W): 0B: DRFM disable (Default) 1B: DRFM enable	3 (Host Write)
Bounded Refresh Configuration (BRC)	R/W	OP[2:1]	00B: BRC 2 (default) 01B: BRC 3 10B: BRC 4 11B: RFU	3
BRC Support Level	R	OP[3]	0B: BRC2, 3, 4 (Default) 1B: BRC2 Only	3
Adaptive RFM (ARFM)	R/W	OP[5:4]	00B: Default - RAAIMT, RAAMMT, RAADEC 01B: Level A - RAAIMT-A, RAAMMT-A, RAADEC-A 10B: Level B - RAAIMT-B, RAAMMT-B, RAADEC-B 11B: Level C - RAAIMT-C, RAAMMT-C, RAADEC-C	1
RAA Counter Decrement per REF Command	R	OP[7:6]	00B: RAAIMT 01B: RAAIMT * 0.5 10B: RFU 11B: RFU	1, 2

NOTE 1 Refresh Management settings are vendor specific by the MR settings.
NOTE 2 Only applicable if the Refresh Management Required bit is set to “1” (MR58 OP[0]=1).
NOTE 3 Only applicable if the DRFM function is supported (Status Read MR59:OP[0]=1).

3.5.61 MR60 Partial Array Self Refresh

PASR has been deprecated starting with spec working revision 1.90, JESD79-5C-v1.30. All MR60 bits will behave as RFU on devices that do not support PASR.

MR60 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PASR Segment Mask							

Function	Register Type	Operand	Data	Notes
Segment 0 (000)	W	OP0	0=Normal, 1=Masked	
Segment 1 (001)	W	OP1	0=Normal, 1=Masked	
Segment 2 (010)	W	OP2	0=Normal, 1=Masked	
Segment 3 (011)	W	OP3	0=Normal, 1=Masked	
Segment 4 (100)	W	OP4	0=Normal, 1=Masked	
Segment 5 (101)	W	OP5	0=Normal, 1=Masked	
Segment 6 (110)	W	OP6	0=Normal, 1=Masked	Must be 0 for 24Gbit and 48 Gbit devices.
Segment 7 (111)	W	OP7	0=Normal, 1=Masked	Must be 0 for 24Gbit and 48 Gbit devices.

3.5.62 MR61 (MA[7:0]=3D$_H$) - Package Output Driver Test Mode

MR61 Register Information

This MR is used for the characterization of the DRAM package. Refer to the Package Output Driver Test Mode function for more details.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RSVD			Package Output Driver Test Mode				

Function	Register Type	Operand	Data	Notes
Package Output Driver Test Mode	W	OP[4:0]	00000B: Package Test Disabled (Default) 00001B: Package Test DML 00010B: Package Test DMU (X16 only) 00011B: RFU 00100B: RFU 00101B: RFU ...thru 01111B: RFU 10000B: Package Test DQL0 10001B: Package Test DQL1 10010B: Package Test DQL2 10011B: Package Test DQL3 10100B: Package Test DQL4 (X8 and X16 only) 10101B: Package Test DQL5 (X8 and X16 only) 10110B: Package Test DQL6 (X8 and X16 only) 10111B: Package Test DQL7 (X8 and X16 only) 11000B: Package Test DQU0 (X16 only) 11001B: Package Test DQU1 (X16 only) 11010B: Package Test DQU2 (X16 only) 11011B: Package Test DQU3 (X16 only) 11100B: Package Test DQU4 (X16 only) 11101B: Package Test DQU5 (X16 only) 11110B: Package Test DQU6 (X16 only) 11111B: Package Test DQU7 (X16 only)	
RSVD	W	OP[7:5]	Must be programmed to 000	

3.5.63 MR62 (MA[7:0]=3E$_H$) - Vendor Specified

MR62 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Vendor Specified							

Function	Register Type	Operand	Data	Notes

3.5.64 MR63 (MA[7:0]=3F$_H$) - DRAM Scratch Pad

MR63 Register Information

This MR is used by the host controller to read back Control Words from the RCD. Control Words are the RCD equivalent of the DRAM MR registers. The DRAM implements MR63 as a simple read/write register, writable via an MRW to address 3Fh, and readable via an MRR to address 3Fh.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DRAM Scratch Pad							

Function	Register Type	Operand	Data	Notes
DRAM Scratch Pad	R/W	OP[7:0]	Any value is valid	1

NOTE 1 The contents of this register have no function in the DRAM. Details for this function can be found in the DDR5 RCD01 standard.

The following data are just for reference and are not part of the DRAM standard.

3.5.64.1 RCD Control Word Usage Example

The method to read an RCD Control Word is as follows:

- The host controller writes to the RCD's CW Read Pointer, which selects the RCD control word to be read.
- The host controller then does an MRW to DRAM MR63. This MRW passes through the RCD to the DRAMs, but is modified by the RCD. The RCD will detect this write to MR63 and replace the data from the host controller with the contents of the RCD register pointed to by the CW Read Pointer.
- The host controller will then read the DRAM's MR63, which now contains the value from the desired RCD control word. All DRAMs in the rank will return this same value to the host controller

3.5.65 MR64 (MA[7:0]=40_H) - NVRAM Paging (RFU)

MR64 Register Information

This MR is reserved for NVRAM paging.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU							

Function	Register Type	Operand	Data	Notes

3.5.66 MR65 (MA[7:0]=41_H) - Serial Number 1

MR65 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial Number 1							

Function	Register Type	Operand	Data	Notes
Serial Number 1	R	OP[7:0]	Serial Number 1	1, 2
NOTE 1 The serial number of 0x00 in all bytes is not allowed				
NOTE 2 This byte definition is optional feature, but expect mandatory implementation upon next DDR5 DRAM die release.				

3.5.67 MR66 (MA[7:0]=42_H) - Serial Number 2

MR66 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial Number 2							

Function	Register Type	Operand	Data	Notes
Serial Number 2	R	OP[7:0]	Serial Number 2	1, 2
NOTE 1 The serial number of 0x00 in all bytes is not allowed				
NOTE 2 This byte definition is optional feature, but expect mandatory implementation upon next DDR5 DRAM die release.				

3.5.68 MR67 (MA[7:0]=43_H) - Serial Number 3

MR67 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial Number 3							

Function	Register Type	Operand	Data	Notes
Serial Number 3	R	OP[7:0]	Serial Number 3	1, 2

NOTE 1 The serial number of 0x00 in all bytes is not allowed

NOTE 2 This byte definition is optional feature, but expect mandatory implementation upon next DDR5 DRAM die release.

3.5.69 MR68 (MA[7:0]=44_H) - Serial Number 4

MR68 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial Number 4							

Function	Register Type	Operand	Data	Notes
Serial Number 4	R	OP[7:0]	Serial Number 4	1, 2

NOTE 1 The serial number of 0x00 in all bytes is not allowed

NOTE 2 This byte definition is optional feature, but expect mandatory implementation upon next DDR5 DRAM die release.

3.5.70 MR69 (MA[7:0]=45_H) - Serial Number 5

MR69 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial Number 5							

Function	Register Type	Operand	Data	Notes
Serial Number 5	R	OP[7:0]	Serial Number 5	1, 2

NOTE 1 The serial number of 0x00 in all bytes is not allowed

NOTE 2 This byte definition is optional feature, but expect mandatory implementation upon next DDR5 DRAM die release.

3.5.71 MR70 (MA[7:0]=46_H) thru MR75 (MA[7:0]=$4B_H$)

MR70 thru MR75 Register Information

These Mode Registers are used when optional feature PRAC is enabled. Detailed Mode Register information can be found from Section 16.10.

3.5.72 Mode Register Definitions for DFE

The following mode registers are used to configure the Decision Feedback Equalization (DFE), Per Bit Duty Cycle Adjuster and Per Bit VrefDQ features of the DRAM. The Mode Registers MA[7:0]=70-FF_H are organized in a way such that mode registers for programming of DFE, DCA & VrefDQ configuration per DQ or DM are grouped together. For example:

DQL0 starts at MA[7:0]=80_H, MR128
DQL1 starts at MA[7:0]=88_H, MR136
:
DQU6 starts at MA[7:0]=$F0_H$, MR240
DQU7 starts at MA[7:0]=$F8_H$, MR248

Looking further into the 8-bit binary encoding, MA[6:3] is defined as a direct mapping for DQL0 to DQU7, i.e.,
MA[7:0]=1000:0XXXb for DQ0,
MA[7:0]=1000:1XXXb for DQ1,
:
MA[7:0]=1111:0XXXb for DQU6
MA[7:0]=1111:1XXXb for DQU7.

Table 29 — Visual Representation of DFE, per Bit DCA, and per Bit VrefDQ Mode Register Mapping

MRW Address, Binary	Function	MRW address bits [2:0]							
		000b	001b	010b	011b	100b	101b	110b	111b
0111-0XXX	DML	Gain	Tap1	Tap2	Tap3	Tap4	MR Address Space not currently used		
0111-1XXX	DMU								
1000-0XXX	DQL0								
1000-1XXX	DQL1								
1001-0XXX	DQL2								
1001-1XXX	DQL3								
1010-0XXX	DQL4								
1010-1XXX	DQL5								
1011-0XXX	DQL6								
1011-1XXX	DQL7								
1100-0XXX	DQU0								
1100-1XXX	DQU1								
1101-0XXX	DQU2								
1101-1XXX	DQU3								
1110-0XXX	DQU4								
1110-1XXX	DQU5								
1111-0XXX	DQU6								
1111-1XXX	DQU7								

3.5.73 MR103 (MA[7:0]=67_H) - DQSL_t DCA for IBCLK and QCLK

MR103 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQSL_t IBCLK Sign	RFU	DQSL_t DCA for IBCLK		DQSL_t QCLK sign	RFU	DQSL_t DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQSL_t DCA for QCLK	W	OP[1:0]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQSL_t QCLK sign	W	OP[3]	0_B: positive (Default) 1_B: negative	
DQSL_t DCA for IBCLK	W	OP[5:4]	00_B: disable (Default) 01_B: step +1 10_B: step +2 11_B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQSL_t IBCLK sign	W	OP[7]	0_B: positive (Default) 1_B: negative	

3.5.74 MR104 (MA[7:0]=68_H) - DQSL_t DCA for QBCLK

MR104 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				DQSL_t QBCLK Sign	RFU	DQSL_t DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQSL_t DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQSL_t QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
RFU		OP[7:4]		

3.5.75 MR105 (MA[7:0]=69_H) - DQSL_c DCA for IBCLK and QCLK

MR105 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQSL_c IBCLK Sign	RFU	DQSL_c DCA for IBCLK		DQSL_c QCLK sign	RFU	DQSL_c DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQSL_c DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQSL_c QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQSL_c DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQSL_c IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.76 MR106 (MA[7:0]=$6A_H$) - DQSL_c DCA for QBCLK

MR106 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				DQSL_c QBCLK Sign	RFU	DQSL_c DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQSL_c DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQSL_c QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
RFU		OP[7:4]		

3.5.77 MR107 (MA[7:0]=6B$_H$) - DQSU_t DCA for IBCLK and QCLK

MR107 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQSU_t IBCLK Sign	RFU	DQSU_t DCA for IBCLK		DQSU_t QCLK sign	RFU	DQSU_t DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQSU_t DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQSU_t QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQSU_t DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQSU_t IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.78 MR108 (MA[7:0]=6C$_H$) - DQSU_t DCA for QBCLK

MR108 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				DQSU_t QBCLK Sign	RFU	DQSU_t DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQSU_t DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQSU_t QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
RFU		OP[7:4]		

3.5.79 MR109 (MA[7:0]=6D$_H$) - DQSU_c DCA for IBCLK and QCLK

MR109 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQSU_c IBCLK Sign	RFU	DQSU_c DCA for IBCLK		DQSU_c QCLK sign	RFU	DQSU_c DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQSU_c DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQSU_c QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQSU_c DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQSU_c IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.80 MR110 (MA[7:0]=6E$_H$) - DQSU_c DCA for QBCLK

MR110 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				DQSU_c QBCLK Sign	RFU	DQSU_c DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQSU_c DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQSU_c QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
RFU		OP[7:4]		

3.5.81 MR111 (MA[7:0]=6F$_H$) - DFE Global Settings

MR111 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU			Global DFE Tap-4 Enable	Global DFE Tap-3 Enable	Global DFE Tap-2 Enable	Global DFE Tap-1 Enable	Global DFE Gain Enable

Function	Register Type	Operand	Data	Notes
Global DFE Gain Enable	R/W	OP[0]	0B: DFE Gain Enabled (DEFAULT) 1B: DFE Gain Disabled	1, 2
Global DFE Tap-1 Enable	R/W	OP[1]	0B: DFE Tap-1 Enabled (DEFAULT) 1B: DFE Tap-1 Disabled	1, 2
Global DFE Tap-2 Enable	R/W	OP[2]	0B: DFE Tap-2 Enabled (DEFAULT) 1B: DFE Tap-2 Disabled	1, 2
Global DFE Tap-3 Enable	R/W	OP[3]	0B: DFE Tap-3 Enabled (DEFAULT) 1B: DFE Tap-3 Disabled	1, 2
Global DFE Tap-4 Enable	R/W	OP[4]	0B: DFE Tap-4 Enabled (DEFAULT) 1B: DFE Tap-4 Disabled	1, 2
RFU	RFU	OP[7:5]	RFU	

NOTE 1 This bit applies to all DM and DQ pins.

NOTE 2 Setting MR111:OP[4:0] = 11111_B disables the DFE.

3.5.82 MR112 (MA[7:0]=70_H) thru MR248 (MA[7:0]=$F8_H$) - DFE Gain Bias

MR112 Register Information

This definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Gain Bias. The MRs are positioned every 8 MRs (MR112, MR120, MR128, etc.) until all pins are covered. Refer to Mode Register Assignment table for details.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				Sign Bit Gain Bias	DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DFE Gain Bias	R/W	OP[2:0]	000B: DFE Gain Bias Step 0 (Default) 001B: DFE Gain Bias Step 1 010B: DFE Gain Bias Step 2 011B: DFE Gain Bias Step 3 100B: RFU 101B: RFU 111B: RFU	1, 2, 3, 4
Sign Bit Gain Bias	R/W	OP[3]	0B: Positive DFE Gain Bias (Default) 1B: Negative DFE Gain Bias	4
RFU	RFU	OP[7:4]	RFU	

NOTE 1 Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance, and Range values
NOTE 2 The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
NOTE 3 The number of step size, step values and range are speed dependent
NOTE 4 Setting all DFE Gain Bias bits (MR112, MR120, MR128, etc.) OP[3:0]=0000_B and all DFE Tap 1-4 Bias bits (MR113, MR114, MR115, MR116, etc.) OP[7:0]=00000000_B disables DFE.

3.5.83 MR113 (MA[7:0]=71_H) thru MR249 (MA[7:0]=$F9_H$) - DFE Tap-1

MR113 Register Information

This definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Tap-1. The MRs are positioned every 8 MRs (MR113, MR121, MR129, etc.) until all pins are covered. Refer to Mode Register Assignment table for details.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/Disable DFE Tap-1	Sign Bit DFE Tap-1 Bias	DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DFE Tap-1 Bias	R/W	OP[5:0]	000000B: DFE Tap-1 Bias Step 0 (Default) 000001B: DFE Tap-1 Bias Step 1 000010B: DFE Tap-1 Bias Step 2 000011B: DFE Tap-1 Bias Step 3 000100B: DFE Tap-1 Bias Step 4 000101B: DFE Tap-1 Bias Step 5 : 100110B: DFE Tap-1 Bias Step 38 100111B: DFE Tap-1 Bias Step 39 101000B: DFE Tap-1 Bias Step 40 101001B: RFU : 111111B: RFU	1, 2, 3, 4
Sign Bit DFE Tap-1 Bias	R/W	OP[6]	0B: Positive DFE Tap-1 Bias (Default) 1B: Negative DFE Tap-1 Bias	4
Enable/Disable DFE Tap-1	R/W	OP[7]	0B: DFE Tap-1 Disable (Default) 1B: DFE Tap-1 Enable	4

NOTE 1 Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance, and Range values

NOTE 2 The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables

NOTE 3 The number of step size, step values and range are speed dependent

NOTE 4 Setting all DFE Gain Bias bits (MR112, MR120, MR128, etc.) OP[3:0]=0000_B and all DFE Tap 1-4 Bias bits (MR113, MR114, MR115, MR116, etc.) OP[7:0]=00000000_B disables DFE.

3.5.84 MR114 (MA[7:0]=72_H) thru MR250 (MA[7:0]=FA_H) - DFE Tap-2

MR114 Register Information

This definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Tap-2. The MRs are positioned every 8 MRs (MR114, MR122, MR130, etc.) until all pins are covered. Refer to Mode Register Assignment table for details.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/Disable DFE Tap-2	Sign Bit DFE Tap-2 Bias	DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DFE Tap-2 Bias	R/W	OP[5:0]	000000B: DFE Tap-2 Bias Step 0 (Default) 000001B: DFE Tap-2 Bias Step 1 000010B: DFE Tap-2 Bias Step 2 000011B: DFE Tap-2 Bias Step 3 000100B: DFE Tap-2 Bias Step 4 000101B: DFE Tap-2 Bias Step 5 : 001101B: DFE Tap-2 Bias Step 13 001110B: DFE Tap-2 Bias Step 14 001111B: DFE Tap-2 Bias Step 15 010000B: RFU : 111111B: RFU	1, 2, 3, 4
Sign Bit DFE Tap-2 Bias	R/W	OP[6]	0B: Positive DFE Tap-2 Bias (Default) 1B: Negative DFE Tap-2 Bias	4
Enable/Disable DFE Tap-2	R/W	OP[7]	0B: DFE Tap-2 Disable (Default) 1B: DFE Tap-2 Enable	4

NOTE 1 Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance, and Range values

NOTE 2 The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables

NOTE 3 The number of step size, step values and range are speed dependent

NOTE 4 Setting all DFE Gain Bias bits (MR112, MR120, MR128, etc.) OP[3:0]=0000_B and all DFE Tap 1-4 Bias bits (MR113, MR114, MR115, MR116, etc.) OP[7:0]=00000000_B disables DFE.

3.5.85 MR115 (MA[7:0]=73_H) thru MR251 (MA[7:0]=FB_H) - DFE Tap-3

MR115 Register Information

This definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Gain Bias. The MRs are positioned every 8 MRs (MR115, MR123, MR131, etc.) until all pins are covered. Refer to Mode Register Assignment table for details.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/Disable DFE Tap-3	Sign Bit DFE Tap-3 Bias	DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DFE Tap-3 Bias	R/W	OP[5:0]	000000B: DFE Tap-3 Bias Step 0 (Default) 000001B: DFE Tap-3 Bias Step 1 000010B: DFE Tap-3 Bias Step 2 000011B: DFE Tap-3 Bias Step 3 000100B: DFE Tap-3 Bias Step 4 000101B: DFE Tap-3 Bias Step 5 : 001010B: DFE Tap-3 Bias Step 10 001011B: DFE Tap-3 Bias Step 11 001100B: DFE Tap-3 Bias Step 12 001101B: RFU : 111111B: RFU	1, 2, 3, 4
Sign Bit DFE Tap-3 Bias	R/W	OP[6]	0B: Positive DFE Tap-3 Bias (Default) 1B: Negative DFE Tap-3 Bias	4
Enable/Disable DFE Tap-3	R/W	OP[7]	0B: DFE Tap-3 Disable (Default) 1B: DFE Tap-3 Enable	4

NOTE 1 Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance, and Range values
NOTE 2 The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
NOTE 3 The number of step size, step values and range are speed dependent
NOTE 4 Setting all DFE Gain Bias bits (MR112, MR120, MR128, etc.) OP[3:0]=0000_B and all DFE Tap 1-4 Bias bits (MR113, MR114, MR115, MR116, etc.) OP[7:0]=00000000_B disables DFE.

3.5.86 MR116 (MA[7:0]=74_H) thru MR252 (MA[7:0]=FC_H) - DFE Tap-4

MR116 Register Information

This definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Tap-4. The MRs are positioned every 8 MRs (MR116, MR124, MR132, etc.) until all pins are covered. Refer to Mode Register Assignment table for details.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/Disable DFE Tap-4	Sign Bit DFE Tap-4 Bias	DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DFE Tap-4 Bias	R/W	OP[5:0]	000000B: DFE Tap-4 Bias Step 0 (Default) 000001B: DFE Tap-4 Bias Step 1 000010B: DFE Tap-4 Bias Step 2 000011B: DFE Tap-4 Bias Step 3 000100B: DFE Tap-4 Bias Step 4 000101B: DFE Tap-4 Bias Step 5 000110B: DFE Tap-4 Bias Step 6 000111B: DFE Tap-4 Bias Step 7 001000B: DFE Tap-4 Bias Step 8 001001B: DFE Tap-4 Bias Step 9 001010B: RFU : 111111B: RFU	1, 2, 3, 4
Sign Bit DFE Tap-4 Bias	R/W	OP[6]	0B: Positive DFE Tap-4 Bias (Default) 1B: Negative DFE Tap-4 Bias	4
Enable/Disable DFE Tap-4	R/W	OP[7]	0B: DFE Tap-4 Disable (Default) 1B: DFE Tap-4 Enable	4

NOTE 1 Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance, and Range values

NOTE 2 The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables

NOTE 3 The number of step size, step values and range are speed dependent

NOTE 4 Setting all DFE Gain Bias bits (MR112, MR120, MR128, etc.) OP[3:0]=0000_B and all DFE Tap 1-4 Bias bits (MR113, MR114, MR115, MR116, etc.) OP[7:0]=00000000_B disables DFE.

3.5.87 MR117 (MA[7:0]=75_H) - RFU

3.5.88 MR118 (MA[7:0]=76_H) - DML VrefDQ Offset

MR118 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DML VREFDQ sign	DML VREFDQ Offset			RFU			

Function	Register Type	Operand	Data	Notes
RFU		OP[3:0]		
DML VREFDQ Offset	W	OP[6:4]	000B: disable (Default) 001B: step +1 010B: step +2 011B: step +3 100B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DML VREFDQ sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.89 MR126 (MA[7:0]=$7E_H$) - DMU VrefDQ Offset

MR126 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DMU VREFDQ sign	DMU VREFDQ Offset			RFU			

Function	Register Type	Operand	Data	Notes
RFU		OP[3:0]		
DMU VREFDQ Offset	W	OP[6:4]	000B: disable (Default) 001B: step +1 010B: step +2 011B: step +3 100B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DMU VREFDQ sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.90 MR133 (MA[7:0]=85_H) - DQL0 DCA for IBCLK and QCLK

MR133 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL0 IBCLK Sign	RFU	DQL0 DCA for IBCLK		DQL0 QCLK sign	RFU	DQL0 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQL0 DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL0 QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQL0 DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQL0 IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.91 MR134 (MA[7:0]=86_H) - DQL0 DCA for QBCLK and DQL0 VrefDQ Offset

MR134 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL0 VREFDQ sign	DQL0 VREFDQ Offset			DQL0 QBCLK Sign	RFU	DQL0 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQL0 DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL0 QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQL0 VREFDQ Offset	W	OP[6:4]	000B: disable (Default) 001B: step +1 010B: step +2 011B: step +3 100B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQL0 VREFDQ sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.92 MR141 (MA[7:0]=8D$_H$) - DQL1 DCA for IBCLK and QCLK

MR141 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL1 IBCLK Sign	RFU	DQL1 DCA for IBCLK		DQL1 QCLK sign	RFU	DQL1 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQL1 DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL1 QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQL1 DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQL1 IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.93 MR142 (MA[7:0]=8E$_H$) - DQL1 DCA for QBCLK and DQL1 VrefDQ Offset

MR142 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL1 VREFDQ sign	DQL1 VREFDQ Offset			DQL1 QBCLK Sign	RFU	DQL1 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQL1 DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL1 QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQL1 VREFDQ Offset	W	OP[6:4]	000B: disable (Default) 001B: step +1 010B: step +2 011B: step +3 100B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQL1 VREFDQ sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.94 MR149 (MA[7:0]=95_H) - DQL2 DCA for IBCLK and QCLK

MR149 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL2 IBCLK Sign	RFU	DQL2 DCA for IBCLK		DQL2 QCLK sign	RFU	DQL2 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQL2 DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL2 QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQL2 DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQL2 IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.95 MR150 (MA[7:0]=96_H) - DQL2 DCA for QBCLK and DQL2 VrefDQ Offset

MR150 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL2 VREFDQ sign	DQL2 VREFDQ Offset			DQL2 QBCLK Sign	RFU	DQL2 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQL2 DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL2 QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQL2 VREFDQ Offset	W	OP[6:4]	000B: disable (Default) 001B: step +1 010B: step +2 011B: step +3 100B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQL2 VREFDQ sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.96 MR157 (MA[7:0]=9D$_H$) - DQL3 DCA for IBCLK and QCLK

MR157 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL3 IBCLK Sign	RFU	DQL3 DCA for IBCLK		DQL3 QCLK sign	RFU	DQL3 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQL3 DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL3 QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQL3 DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQL3 IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.97 MR158 (MA[7:0]=9E$_H$) - DQL3 DCA for QBCLK and DQL3 VrefDQ Offset

MR158 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL3 VREFDQ sign	DQL3 VREFDQ Offset			DQL3 QBCLK Sign	RFU	DQL3 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQL3 DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL3 QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQL3 VREFDQ Offset	W	OP[6:4]	000B: disable (Default) 001B: step +1 010B: step +2 011B: step +3 100B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQL3 VREFDQ sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.98 MR165 (MA[7:0]=$A5_H$) - DQL4 DCA for IBCLK and QCLK

MR165 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL4 IBCLK Sign	RFU	DQL4 DCA for IBCLK		DQL4 QCLK sign	RFU	DQL4 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQL4 DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL4 QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQL4 DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQL4 IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.99 MR166 (MA[7:0]=$A6_H$) - DQL4 DCA for QBCLK and DQL4 VrefDQ Offset

MR166 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL4 VREFDQ sign	DQL3 VREFDQ Offset			DQL3 QBCLK Sign	RFU	DQL3 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQL4 DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL4 QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQL4 VREFDQ Offset	W	OP[6:4]	000B: disable (Default) 001B: step +1 010B: step +2 011B: step +3 100B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQL4 VREFDQ sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.100 MR173 (MA[7:0]=AD_H) - DQL5 DCA for IBCLK and QCLK

MR173 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL5 IBCLK Sign	RFU	DQL5 DCA for IBCLK		DQL5 QCLK sign	RFU	DQL5 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQL5 DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL5 QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQL5 DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQL5 IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.101 MR174 (MA[7:0]=AE_H) - DQL5 DCA for QBCLK and DQL5 VrefDQ Offset

MR174 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL5 VREFDQ sign	DQL5 VREFDQ Offset			DQL5 QBCLK Sign	RFU	DQL5 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQL5 DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL5 QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQL5 VREFDQ Offset	W	OP[6:4]	000B: disable (Default) 001B: step +1 010B: step +2 011B: step +3 100B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQL5 VREFDQ sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.102 MR181 (MA[7:0]=$B5_H$) - DQL6 DCA for IBCLK and QCLK

MR181 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL6 IBCLK Sign	RFU	DQL6 DCA for IBCLK		DQL6 QCLK sign	RFU	DQL6 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQL6 DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL6 QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQL6 DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQL6 IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.103 MR182 (MA[7:0]=$B6_H$) - DQL6 DCA for QBCLK and DQL6 VrefDQ Offset

MR182 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL6 VREFDQ sign	DQL6 VREFDQ Offset			DQL6 QBCLK Sign	RFU	DQL6 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQL6 DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL6 QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQL6 VREFDQ Offset	W	OP[6:4]	000B: disable (Default) 001B: step +1 010B: step +2 011B: step +3 100B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQL6 VREFDQ sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.104 MR189 (MA[7:0]=BD_H) - DQL7 DCA for IBCLK and QCLK

MR189 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL7 IBCLK Sign	RFU	DQL7 DCA for IBCLK		DQL7 QCLK sign	RFU	DQL7 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQL7 DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL7 QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQL7 DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQL7 IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.105 MR190 (MA[7:0]=BE_H) - DQL7 DCA for QBCLK and DQL7 VrefDQ Offset

MR190 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL7 VREFDQ sign	DQL7 VREFDQ Offset			DQL7 QBCLK Sign	RFU	DQL7 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQL7 DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQL7 QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQL7 VREFDQ Offset	W	OP[6:4]	000B: disable (Default) 001B: step +1 010B: step +2 011B: step +3 100B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQL7 VREFDQ sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.106 MR197 (MA[7:0]=$C5_H$) - DQU0 DCA for IBCLK and QCLK

MR197 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU0 IBCLK Sign	RFU	DQU0 DCA for IBCLK		DQU0 QCLK sign	RFU	DQU0 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQU0 DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU0 QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQU0 DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQU0 IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.107 MR198 (MA[7:0]=$C6_H$) - DQU0 DCA for QBCLK and DQU0 VrefDQ Offset

MR198 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU0 VREFDQ sign	DQU0 VREFDQ Offset			DQU0 QBCLK Sign	RFU	DQU0 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQU0 DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU0 QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQU0 VREFDQ Offset	W	OP[6:4]	000B: disable (Default) 001B: step +1 010B: step +2 011B: step +3 100B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQU0 VREFDQ sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.108 MR205 (MA[7:0]=CD_H) - DQU1 DCA for IBCLK and QCLK

MR205 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU1 IBCLK Sign	RFU	DQU1 DCA for IBCLK		DQU1 QCLK sign	RFU	DQU1 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQU1 DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU1 QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQU1 DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQU1 IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.109 MR206 (MA[7:0]=CE_H) - DQU1 DCA for QBCLK and DQU1 VrefDQ Offset

MR206 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU1 VREFDQ sign	DQU1 VREFDQ Offset			DQU1 QBCLK Sign	RFU	DQU1 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQU1 DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU1 QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQU1 VREFDQ Offset	W	OP[6:4]	000B: disable (Default) 001B: step +1 010B: step +2 011B: step +3 100B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQU1 VREFDQ sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.110 MR213 (MA[7:0]=$D5_H$) - DQU2 DCA for IBCLK and QCLK

MR213 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU2 IBCLK Sign	RFU	DQU2 DCA for IBCLK		DQU2 QCLK sign	RFU	DQU2 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQU2 DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU2 QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQU2 DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQU2 IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.111 MR214 (MA[7:0]=$D6_H$) - DQU2 DCA for QBCLK and DQU2 VrefDQ Offset

MR214 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU2 VREFDQ sign	DQU2 VREFDQ Offset			DQU2 QBCLK Sign	RFU	DQU2 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQU2 DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU2 QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQU2 VREFDQ Offset	W	OP[6:4]	000B: disable (Default) 001B: step +1 010B: step +2 011B: step +3 100B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQU2 VREFDQ sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.112 MR221 (MA[7:0]=DD_H) - DQU3 DCA for IBCLK and QCLK

MR221 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU3 IBCLK Sign	RFU	DQU3 DCA for IBCLK		DQU3 QCLK sign	RFU	DQU3 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQU3 DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU3 QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQU3 DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQU3 IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.113 MR222 (MA[7:0]=DE_H) - DQU3 DCA for QBCLK and DQU3 VrefDQ Offset

MR222 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU3 VREFDQ sign	DQU3 VREFDQ Offset			DQU3 QBCLK Sign	RFU	DQU3 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQU3 DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU3 QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQU3 VREFDQ Offset	W	OP[6:4]	000B: disable (Default) 001B: step +1 010B: step +2 011B: step +3 100B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQU3 VREFDQ sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.114 MR229 (MA[7:0]=$E5_H$) - DQU4 DCA for IBCLK and QCLK

MR229 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU4 IBCLK Sign	RFU	DQU4 DCA for IBCLK		DQU4 QCLK sign	RFU	DQU4 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQU4 DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU4 QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQU4 DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQU4 IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.115 MR230 (MA[7:0]=$E6_H$) - DQU4 DCA for QBCLK and DQU4 VrefDQ Offset

MR230 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU4 VREFDQ sign	DQU4 VREFDQ Offset			DQU4 QBCLK Sign	RFU	DQU4 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQU4 DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU4 QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQU4 VREFDQ Offset	W	OP[6:4]	000B: disable (Default) 001B: step +1 010B: step +2 011B: step +3 100B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQU4 VREFDQ sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.116 MR237 (MA[7:0]=ED_H) - DQU5 DCA for IBCLK and QCLK

MR237 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU5 IBCLK Sign	RFU	DQU5 DCA for IBCLK		DQU5 QCLK sign	RFU	DQU5 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQU5 DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU5 QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQU5 DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQU5 IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.117 MR238 (MA[7:0]=EE_H) - DQU5 DCA for QBCLK and DQU5 VrefDQ Offset

MR238 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU5 VREFDQ sign	DQU5 VREFDQ Offset			DQU5 QBCLK Sign	RFU	DQU5 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQU5 DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU5 QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQU5 VREFDQ Offset	W	OP[6:4]	000B: disable (Default) 001B: step +1 010B: step +2 011B: step +3 100B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQU5 VREFDQ sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.118 MR245 (MA[7:0]=F5$_H$) - DQU6 DCA for IBCLK and QCLK

MR245 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU6 IBCLK Sign	RFU	DQU6 DCA for IBCLK		DQU6 QCLK sign	RFU	DQU6 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQU6 DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU6 QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQU6 DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQU6 IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.119 MR246 (MA[7:0]=F6$_H$) - DQU6 DCA for QBCLK and DQU6 VrefDQ Offset

MR246 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU6 VREFDQ sign	DQU6 VREFDQ Offset			DQU6 QBCLK Sign	RFU	DQU6 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQU6 DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU6 QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQU6 VREFDQ Offset	W	OP[6:4]	000B: disable (Default) 001B: step +1 010B: step +2 011B: step +3 100B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQU6 VREFDQ sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.120 MR253 (MA[7:0]=FD_H) - DQU7 DCA for IBCLK and QCLK

MR253 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU7 IBCLK Sign	RFU	DQU7 DCA for IBCLK		DQU7 QCLK sign	RFU	DQU7 DCA for QCLK	

Function	Register Type	Operand	Data	Notes
DQU7 DCA for QCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU7 QCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQU7 DCA for IBCLK	W	OP[5:4]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[6]		
DQU7 IBCLK sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.121 MR254 (MA[7:0]=FE_H) - DQU7 DCA for QBCLK and DQU7 VrefDQ Offset

MR254 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQU7 VREFDQ sign	DQU7 VREFDQ Offset			DQU7 QBCLK Sign	RFU	DQU7 DCA for QBCLK	

Function	Register Type	Operand	Data	Notes
DQU7 DCA for QBCLK	W	OP[1:0]	00B: disable (Default) 01B: step +1 10B: step +2 11B: step +3	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
RFU		OP[2]		
DQU7 QBCLK sign	W	OP[3]	0B: positive (Default) 1B: negative	
DQU7 VREFDQ Offset	W	OP[6:4]	000B: disable (Default) 001B: step +1 010B: step +2 011B: step +3 100B ~ 111B: RFU	Range: -3 ~ +3 LSB Codes Step Size: 1LSB
DQU7 VREFDQ sign	W	OP[7]	0B: positive (Default) 1B: negative	

3.5.122 Undefined Mode Registers Spaced in DFE, per Bit DCA, and per Bit VrefDQ Section

MR117
MR119
MR125
MR127
MR135
MR143
MR155
MR159
MR167
MR175
MR183
MR191
MR199
MR207
MR215
MR223
MR231
MR239
MR247
MR255

There are currently no plans to utilize these MR addresses.

4 DDR5 SDRAM Command Description and Operation

4.1 Command Truth Table

(a) Notes 1, 2, and 14 apply to the entire Command truth table
(b) To improve command decode time, the table has been optimized to orient all 1-cycle commands together and all 2-cycle commands together; allowing CA1 to be used to identify the difference between a 1-cycle and a 2-cycle command.

[BG=Bank Group Address, BA=Bank Address, R=Row Address, C=Column Address, MRA=Mode Register Address, OP=Op Code, CID=Chip ID, CW=Control Word, X=Don't Care, V=Valid].

Table 30 — Command Truth Table

Function	Abbreviation	CS_n	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Activate	ACT	L	L	L	R0	R1	R2	R3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	11, 17, 20
		H	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	CID3/R17	
RFU	RFU	L	H	L	L	L	L	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
RFU	RFU	L	H	L	L	L	H	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
Write Pattern	WRP	L	H	L	L	H	L	H	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	11, 15, 18,19, 20
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V	H	H	V	CID3	
Write Pattern w/ Auto Precharge	WRPA	L	H	L	L	H	L	H	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	11, 15, 18,19, 20
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V or DRFM=L	AP=L	H	V	CID3	
RFU	RFU	L	H	L	L	H	H	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
Mode Register Write	MRW	L	H	L	H	L	L	MRA0	MRA1	MRA2	MRA3	MRA4	MRA5	MRA6	MRA7	V	8, 11, 13, 20
		H	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V	V	CW	V	V	V	
Mode Register Read	MRR	L	H	L	H	L	H	MRA0	MRA1	MRA2	MRA3	MRA4	MRA5	MRA6	MRA7	V	8, 13, 21, 20
		H	L	L	V	V	V	V	V	V	V	V	CW	V	V	V	
Write	WR	L	H	L	H	H	L	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8, 12, 15, 19, 20
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V	H	WR_Partial=L	V	CID3	
Write w/Auto Precharge	WRA	L	H	L	H	H	L	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8, 12, 15, 19, 20
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V or DRFM=L	AP=L	WR_Partial=L	V	CID3	
Read	RD	L	H	L	H	H	H	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8, 15, 19, 20
		H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V	H	V	V	CID3	
Read w/Auto Precharge	RDA	L	H	L	H	H	H	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8, 15, 19, 20
		H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V or DRFM=L	AP=L	V	V	CID3	
VrefCA Command	VrefCA	L	H	H	L	L	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	L	V	
VrefCS Command	VrefCS	L	H	H	L	L	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	H	V	
Refresh All	REFab	L	H	H	L	L	H	CID3	V	V	V or RIR	V or H	L	CID0	CID1	CID2	3, 23, 24
Refresh Management All	RFMab	L	H	H	L	L	H	CID3 or DRFM=L	V	V	V	L	L	CID0	CID1	CID2	3, 20
Refresh Same Bank	REFsb	L	H	H	L	L	H	CID3	BA0	BA1	V or RIR	V or H	H	CID0	CID1	CID2	4, 20, 23, 24
Refresh Management Same Bank	RFMsb	L	H	H	L	L	H	CID3 or DRFM=L	BA0	BA1	V	L	H	CID0	CID1	CID2	4, 20
Precharge All	PREab	L	H	H	L	H	L	CID3	V	V	V	V	L	CID0	CID1	CID2	5, 20
Precharge Same Bank	PREsb	L	H	H	L	H	L	CID3	BA0	BA1	V	V	H	CID0	CID1	CID2	6, 20
Precharge	PREpb	L	H	H	L	H	H	CID3 or DRFM=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	7, 20
RFU	RFU	L	H	H	H	L	L	V	V	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	L	H	H	H	L	H	V	V	V	V	H	L	V	V	V	9
Self Refresh Entry w/Frequency Change	SREF	L	H	H	H	L	H	V	V	V	V	L	L	V	V	V	9
Power Down Entry	PDE	L	H	H	H	L	H	V	V	V	V	V	H	ODT=L	V	V	10,16

Table 30 — Command Truth Table (cont'd)

Function	Abbreviation	CS_n	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
MPC	MPC	L	H	H	H	H	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V	20
NOP	NOP	L	H	H	H	H	H	V	V	V	V	V	V	V	V	V	26
Power Down Exit	PDX	L	H	H	H	H	H	V	V	V	V	V	V	V	V	V	
Deselect	DES	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
Reserved		L	L	H	Reserved												

NOTE 1 V means H or L (a defined logic level). X means don't care in which case the signal may be floated.

NOTE 2 Bank group addresses BG[2:0] and Bank addresses BA[1:0] determine which bank is to be operated upon in a specific bank group.

NOTE 3 The Refresh All and Refresh Management All commands are applied to all banks in all bank groups. CA6 and CA7 are required to be valid ("V")

NOTE 4 The Refresh Same Bank and Refresh Management Same Bank commands refresh the same bank in all bank group bits. The bank bits, BA0 and BA1 on CA6 and CA7, respectively, specify the bank within each bank group.

NOTE 5 The Precharge All command applies to all open banks in all bank groups.

NOTE 6 The Precharge Same Bank command applies to the same bank in all bank groups. The bank bits specify the bank within each bank group.

NOTE 7 The Precharge command applies to a single bank as specified by bank address and bank group bits.

NOTE 8 CS_n=LOW during the 2nd cycle of a two cycle command controls ODT in non-target ranks for WR, RD and MRR commands.

NOTE 9 The SRE command places the DRAM in self refresh state

NOTE 10 The PDE command places the DRAM in power down state

NOTE 11 Two cycle commands with no ODT control (ACT, MRW, WRP). DRAM does not execute the command if it receives CS as LOW on 2nd cycle.

NOTE 12 WR command with WR_Partial (WR_P) = Low indicates a partial write command. This is to help DRAM start an internal read for 'read modify write'.

NOTE 13 If CW=Low during the MRW command then DRAM should execute the command, Mode Register will be written. If CW=HIGH then DRAM ignores the MRW command, and the Mode Register is not changed. If CW=Low, DRAM should execute the MRR command. If CW=High, DRAM may or may not execute MRR command.

NOTE 14 CID[3:0] bits are used for 3DS stacking support. When CID[3:0] bits are not used, they are required to be Valid ("V").

NOTE 15 If CA5:BL*=L, the command places the DRAM into the alternate Burst mode described by MR0[1:0] instead of the default Burst Length 16 mode.

NOTE 16 ODT=L is defined to allow On Die Termination (ODT) to persist when the device is in Power Down Mode.

NOTE 17 CID3/R17 is a multi-mode pin allowing for either 16H 3DS stacking with the CID3 bit usage or R17 for high bit density monolithic usage. These usages are mutually exclusive.

NOTE 18 Write Pattern only supports BL16 and BL32.

NOTE 19 When CID3 is not used, its required to be Valid ("V").

NOTE 20 In the case of a DRAM where the density or stacking doesn't require CA[13] the ball location for that function (considering the state of MIR) shall be connected to VDDQ, and the DRAM shall decode CA[13]=L so that the proper selection of die and RA is provided.

NOTE 21 CA[0:1] =[L:L] on the second cycle for burst ordering.

NOTE 22 When host issue MRR with CRC enabled, data comes out with CRC bit.

NOTE 23 If the Refresh Management Required bit is "0" (MR58 OP[0]=0), CA9 is only required to be valid ("V") for a REF command, and the DRAM will treat a RFM command as a REF command. If MR58 OP[0]=1, a REF command requires CA9=H.

NOTE 24 If the Refresh Interval Rate indicator bit is disabled (MR4:OP[3]=0) by the host, CA8 is only required to be valid ("V"). If the Refresh Interval Rate indicator bit is enabled (MR4:OP[3]=1) by the host, the host is required to set CA8=H for REF commands issued at the 1x refresh interval rate and CA8=L for REF commands issued at the 2x refresh interval rate. If the host issues 2x REF commands with CA8=L while MR4:OP[3]=1, but the Refresh rate requirement is 1x as determined internally by the DRAM, the DRAM may internally align to the 1x refresh rate.

NOTE 25 Command Truth Table bits such as BG2, BA1, R16, R17, C10, and CID[3:0] which are unused based on a device's density, configuration width, and stacking options, the CA decode is defined as VALID when in these unused states.

NOTE 26 Unlike DES, NOP is considered a *valid command*, and timing from a preceding valid command must satisfy any associated command timings.

4.1.1 2-Cycle Command Cancel

DDR5 DRAM commands ACT, WRP, WRPA and MRW are 2-cycle commands without associated ODT control requirements. The DRAMwill not execute these2-cycle commands if the CS_n is LOW on the 2nd cycle (command cancel). If the RCD detects a parity error on the 2nd cycle of two-cycle command, the CS_n will remain LOW for both 1st and 2nd cycle of the command. If the command is either Read, Write or MRR, then it will be converted to non-target termination command in the DRAM. If the command is either ACT, WRP, WRPA or MRW, then the erroneous command will be canceled in the DRAM. Command cancel is not intended by the host rather it is a result of CA parity error detected by the RCD. So the relationship between canceled command and the next valid command shall not be illegal. For example, MRR cannot be issued after canceled ACT even with tCMD_cancel satisfied. In that case, the host is supposed to issue PRE first before issuing MRR.

4.1.1 2-Cycle Command Cancel (cont'd)

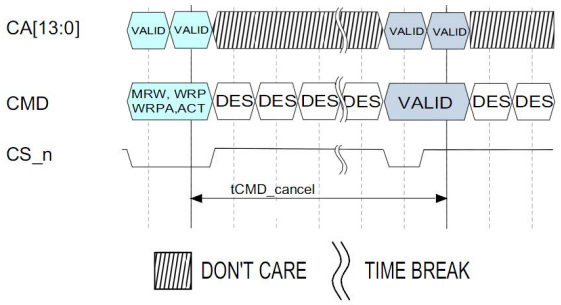


Figure 11 — Command Cancel Timing

Table 31 — Command Cancel Timing

Parameter	Symbol	DDR5 3200 ~ 6400		DDR5 6800 ~ 9200		Unit
		Min	Max	Min	Max	
Command cancel timing for ACT, WRP, WRPA, MRW when CS_n is low on 2nd cycle	tCMD_cancel	8	-	8	-	nCK

4.2 Burst Length, Type, and Order

Accesses within a given burst is currently limited to only sequential, interleaved is not supported. The ordering of accesses within a burst is determined by the burst length and the starting column address as shown in Table . The burst length is defined by bits OP[1:0] of Mode Register MR0. Burst length options include BC8 OTF, BL16, BL32 (optional) and BL32 OTF.

Table 32 — Burst Type and Burst Order for READ

Burst Length	Burst Type	C3	C2	C1	C0	Read Burst Cycle and Burst Address Sequence															
						1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
BC8	SEQ	0	0	V	V	0	1	2	3	4	5	6	7	T	T	T	T	T	T	T	T
		0	1	V	V	4	5	6	7	0	1	2	3	T	T	T	T	T	T	T	T
		1	0	V	V	8	9	A	B	C	D	E	F	T	T	T	T	T	T	T	T
		1	1	V	V	C	D	E	F	8	9	A	B	T	T	T	T	T	T	T	T
BL16	SEQ	0	0	V	V	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		0	1	V	V	4	5	6	7	0	1	2	3	C	D	E	F	8	9	A	B
		1	0	V	V	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1	1	V	V	C	D	E	F	8	9	A	B	4	5	6	7	0	1	2	3

Table 33 — Burst Type and Burst Order for WRITE

Burst Length	Burst Type	C3	C2	C1	C0	Write Burst Cycle and Burst Address Sequence															
						1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
BC8	SEQ	0	V	V	V	0	1	2	3	4	5	6	7	X	X	X	X	X	X	X	X
		1	V	V	V	8	9	A	B	C	D	E	F	X	X	X	X	X	X	X	X
BL16	SEQ	V	V	V	V	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
NOTE 1 T: Output driver for data and strobes are in RTT_PARK.																					
NOTE 2 V: A valid logic level (0 or 1), but respective buffer input ignores level on input pins.																					
NOTE 3 X: Don't Care.																					

4.2.1 Burst Type and Burst Order for Optional BL32 Mode

DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

Table 34 — Burst Type and Burst Order for READ BL32

Burst Length	Burst Type	C10	C3	C2	C1	C0	Read Burst Cycle and Burst Address Sequence							
							1-4	5-8	9-12	13-16	17-20	21-24	25-28	29-32
BL32	SEQ	0	0	0	V	V	0-3	4-7	8-B	C-F	10-13	14-17	18-1B	1C-1F
		0	0	1	V	V	4-7	0-3	C-F	8-B	14-17	10-13	1C-1F	18-1B
		0	1	0	V	V	8-B	C-F	0-3	4-7	18-1B	1C-1F	10-13	14-17
		0	1	1	V	V	C-F	8-B	4-7	0-3	1C-1F	18-1B	14-17	10-13
		1	0	0	V	V	10-13	14-17	18-1B	1C-1F	0-3	4-7	8-B	C-F
		1	0	1	V	V	14-17	10-13	1C-1F	18-1B	4-7	0-3	C-F	8-B
		1	1	0	V	V	18-1B	1C-1F	10-13	14-17	8-B	C-F	0-3	4-7
		1	1	1	V	V	1C-1F	18-1B	14-17	10-13	C-F	8-B	4-7	0-3
BL16 in BL32 OTF		0	0	0	V	V	0-3	4-7	8-B	C-F	X	X	X	X
		0	0	1	V	V	4-7	0-3	C-F	8-B	X	X	X	X
		0	1	0	V	V	8-B	C-F	0-3	4-7	X	X	X	X
		0	1	1	V	V	C-F	8-B	4-7	0-3	X	X	X	X
		1	0	0	V	V	10-13	14-17	18-1B	1C-1F	X	X	X	X
		1	0	1	V	V	14-17	10-13	1C-1F	18-1B	X	X	X	X
		1	1	0	V	V	18-1B	1C-1F	10-13	14-17	X	X	X	X
		1	1	1	V	V	1C-1F	18-1B	14-17	10-13	X	X	X	X

Table 35 — Burst Type and Burst Order for WRITE BL32

Burst Length	Burst Type	C10	C3	C2	C1	C0	Write Burst Cycle and Burst Address Sequence			
							1-8	9-16	17-24	25-32
BL32	SEQ	0	V	V	V	V	0-7	8-F	17-24	25-32
BL16 in BL32 OTF		0	V	V	V	V	0-7	8-F	X	X
		1	V	V	V	V	10-17	18-1F	X	X

NOTE 1 In case of BL16 in BL32 OTF mode by setting MR0[OP1:0=11], the internal write operation starts eight cycles earlier than for BL32 mode. This means that the starting point for tWR and tWTR shall be pulled in by eight clocks.

NOTE 2 T: Output driver for data and strobes are in high impedance.

NOTE 3 V: A valid logic level (0 or 1), but respective buffer input ignores level on input pins.

NOTE 4 X: Don't Care.

4.3 Precharge Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) shall be available for a subsequent row activation a specified time (tRP) after the PRECHARGE command is issued. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period shall be determined by the last PRECHARGE command issued to the bank.

If CA10 on the 2nd pulse of a Read or Write command is LOW, (shown as AP=L in the command truth table) then the auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS latency) thus improving system performance for random data access. The RAS lockout circuit internally delays the precharge operation until the array restore operation has been completed (tRAS satisfied) so that the auto precharge command may be issued with any read. Auto-precharge is also implemented during Write commands. The precharge operation engaged by the Auto precharge command shall not begin until the last data of the burst write sequence is properly stored in the memory array. The bank shall be available for a subsequent row activation a specified time (tRP) after hidden PRECHARGE command (AutoPrecharge) is issued to that bank.

The precharge to precharge delay is defined by tPPD in the core timing tables. tPPD applies to any combination of precharge commands (PREab, PREsb, PREpb). tPPD also applies to any combination of precharge commands to a different die in a 3DS DDR5 SDRAM.

4.3.1 Precharge Command Modes

DDR5 supports three different types of precharge commands: Precharge, Precharge All and Precharge Same Bank

The Precharge Command (PREpb) applies precharge to a specific bank defined by BA[1:0] {if applicable} in a specific bank group defined by BG[2:0], while a Precharge All (PREab) applies precharge to all banks in all bank groups and a Precharge Same Bank (PREsb) applies precharge to a specific bank defined by BA[1:0] in all bank groups. In the case of a 3DS DDR5 SDRAM device, CID[3:0] shall also be selected to identify the target die.

Table 36 shows the different encodes for PREpb, PREab, and PREsb.

Table 36 — Precharge Encodings

Function	Abbreviation	CS_n	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Precharge All	PREab	L	H	H	L	H	L	CID3	V	V	V	V	L	CID0	CID1	CID2	
Precharge Same Bank	PREsb	L	H	H	L	H	L	CID3	BA0	BA1	V	V	H	CID0	CID1	CID2	
Precharge	PREpb	L	H	H	L	H	H	CID3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	
NOTE See Command Truth Table for details																	

4.4 Programmable Preamble and Postamble

DDR5 shall support programmable preambles and postambles.

4.4.1 Read Preamble and Postamble

DDR5 supports a programmable read preamble and postamble. Read Preamble is configured as 1tCK, 2tCK (two unique modes), 3tCK and 4tCK via MR8:OP[2:0].

Function	Register Type	Operand	Data
Read Preamble Settings	R/W	OP[2:0]	000B: 1 tCK - 10 Pattern 001B: 2 tCK - 0010 Pattern 010B: 2 tCK - 1110 Pattern (DDR4 Style) 011B: 3 tCK - 000010 Pattern 100B: 4 tCK - 00001010 Pattern 101B: Reserved 110B: Reserved 111B: Reserved

Read Postamble is configured as 0.5tCK or 1.5tCK via MR8:OP[6]

NOTE: DQS shall have an option to drive early by x-tCK to accommodate different HOST receiver designs as controlled by the Read DQS Offset in MR40:OP[2:0].

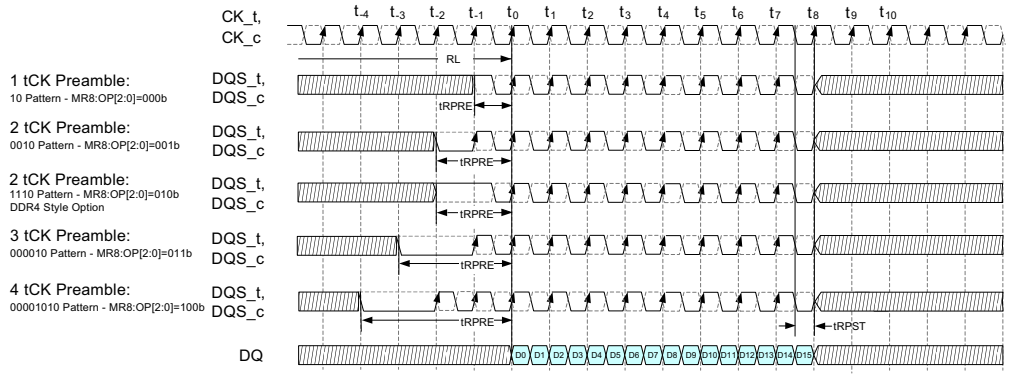


Figure 12 — Example of Read Preamble Modes (Default) with 0.5 tCK Postamble

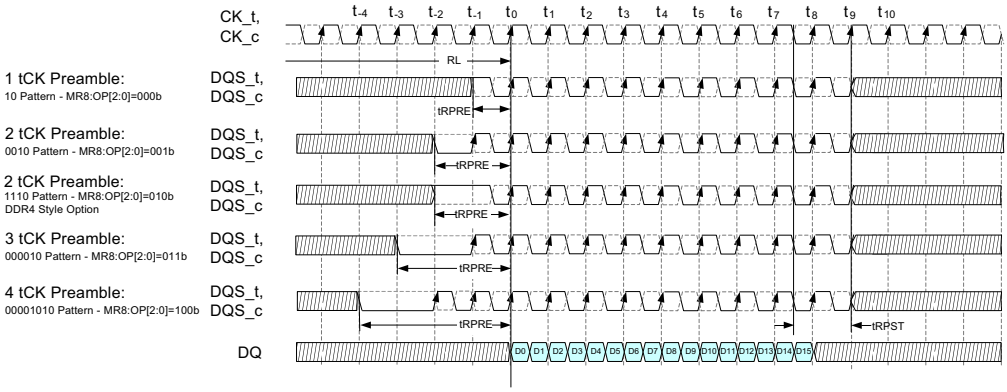


Figure 13 — Example of Read Preamble Modes (Default) with 1.5 tCK Postamble

4.4.1 Read Preamble and Postamble (cont'd)

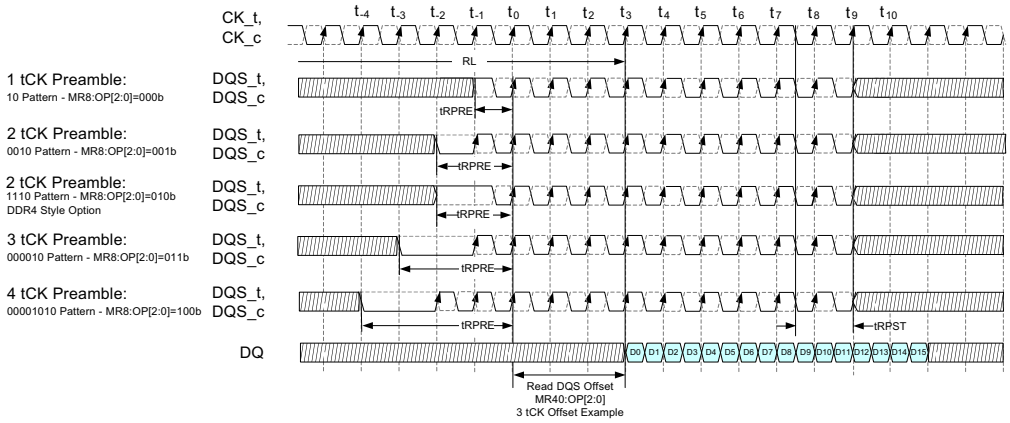


Figure 14 — Example of Read Preamble Modes with 3tCK DQS Offset and with 1.5 tCK Postamble

4.4.2 Write Preamble and Postamble

DDR5 supports a programmable write preamble and postamble.

Write Preamble is configured as 2tCK, 3tCK, and 4tCK via MR8:OP[4:3]

Write Postamble is configured as 0.5tCK or 1.5tCK via MR8:OP[7]

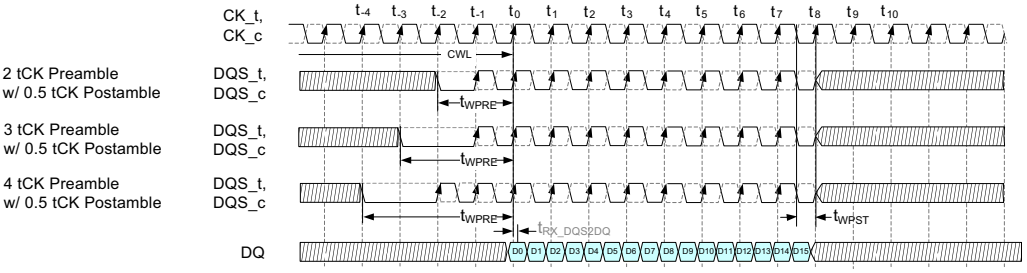


Figure 15 — Example of Write Preamble Modes (Default) with 0.5tCK Postamble

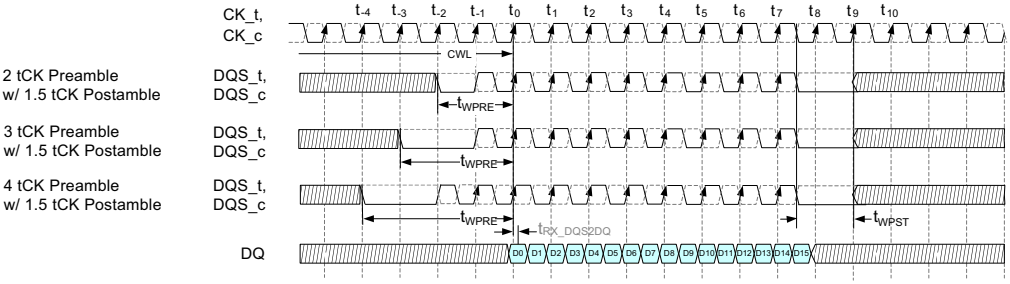
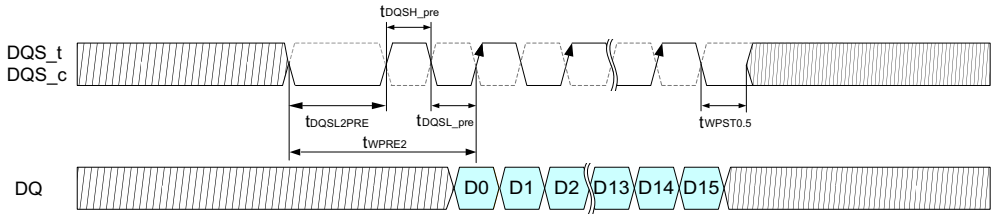


Figure 16 — Example of Write Preamble Modes (Default) with 1.5tCK Postamble

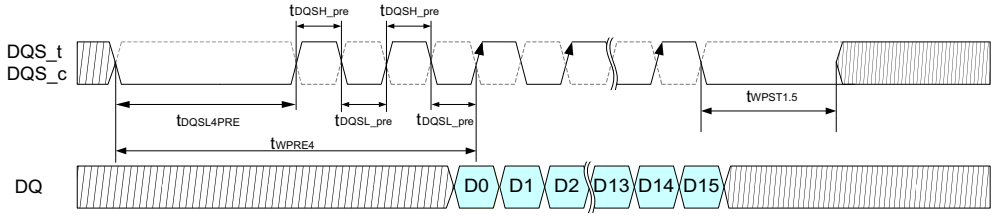
4.4.3 Read and Write Preamble and Postamble Timings

During Read and Write operations, the input receiver strobe shall be aligned with the DQ according to the Preamble and Postamble settings, and the strobe shall meet the specified timing requirements to guarantee enough timing margin by setting the window for the strobe during the Preamble and Postamble time frame. When the DRE is enabled, the DQs shall be high for a minimum of 4-UI prior to the first Write data bit to ensure propoer DFE synchronization. Read Preamble is set by MR8:OP[2:0], and Write Preamble is set by MR8 OP[4:3]. Read Postamble is set by MR8:OP[6], and Write Postamble is set by MR8:OP[7].



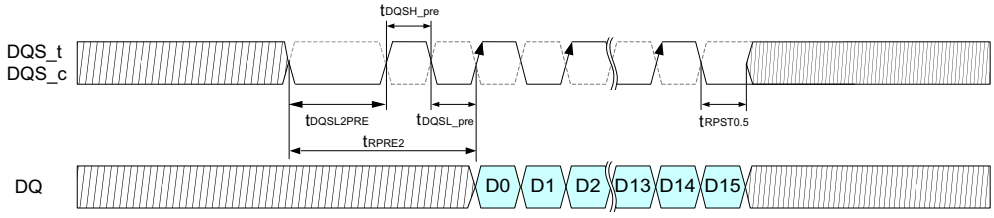
NOTES:
1. BL=16.
2. tDQSH_pre and tDQSL_pre are shown, and apply to all toggles during the Preamble.
3. 2nd Preamble during Write to Write operation shall follow the same requirement.

Figure 17 — DQS Timing while 2tCK Write Preamble and 0.5tCK Postamble



NOTES:
1. BL=16
2. tDQSH_pre and tDQSL_pre are shown, and apply to all toggles during the Preamble.
3. 2nd Preamble during Write to Write operation shall follow the same requirement.

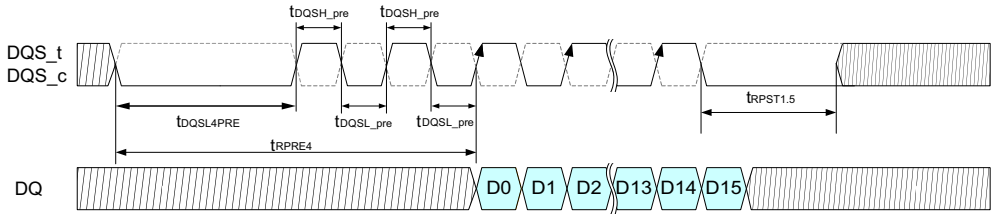
Figure 18 — DQS Timing while 4tCK Write Preamble and 1.5tCK Postamble



NOTES:
1. BL=16.
2. tDQSH_pre and tDQSL_pre are shown, and apply to all toggles during the Preamble.
3. 2nd Preamble during Read to Read operation shall follow the same requirement.

Figure 19 — DQS Timing while 2tCK Read Preamble and 0.5tCK Postamble

4.4.3 Read and Write Preamble and Postamble Timings (cont'd)



NOTES:

1. BL=16.
2. tDQSH_pre and tDQSL_pre are shown, and apply to all toggles during the Preamble.
3. 2nd Preamble during Read to Read operation shall follow the same requirement.

Figure 20 — DQS Timing while 4tCK Read Preamble and 1.5tCK Postamble

4.4.3 Read and Write Preamble and Postamble Timings (cont'd)

Table 37 — Strobe Preamble and Postamble Timing Parameters for DDR5-3200 to 4800

Parameter	Symbol	DDR5 3200 - 3600		DDR5 4000 - 4400		DDR5 4800		Unit
		Min	Max	Min	Max	Min	Max	
DQS_t, DQS_c differential READ Preamble (1tCK Preamble)	tRPRE1	0.900	-	-	-	-	-	tCK(avg)
DQS_t, DQS_c differential READ Preamble (2tCK Preamble)	tRPRE2	1.800	-	1.800	-	1.800	-	tCK(avg)
DQS_t, DQS_c differential READ Preamble DDR4 (2tCK Preamble)	tRPRE2_D4	1.800	-	1.800	-	1.800	-	tCK(avg)
DQS_t, DQS_c differential READ Preamble (3tCK Preamble)	tRPRE3	-	-	2.700	-	2.700	-	tCK(avg)
DQS_t, DQS_c differential READ Preamble (4tCK Preamble)	tRPRE4	-	-	-	-	-	-	tCK(avg)
DQS_t, DQS_c differential READ Postamble (0.5tCK Postamble)	tRPST0.5	0.450	-	0.450	-	0.450	-	tCK(avg)
DQS_t, DQS_c differential READ Postamble (1.5tCK Postamble)	tRPST1.5	1.200	-	1.200	-	1.200	-	tCK(avg)
DQS_t, DQS_c differential WRITE Preamble (2tCK Preamble)	tWPRE2	1.800	-	1.800	-	1.800	-	tCK(avg)
DQS_t, DQS_c differential WRITE Preamble (3tCK Preamble)	tWPRE3	-	-	2.700	-	2.700	-	tCK(avg)
DQS_t, DQS_c differential WRITE Preamble (4tCK Preamble)	tWPRE4	-	-	3.600	-	3.600	-	tCK(avg)
DQS_t, DQS_c differential WRITE Postamble (0.5tCK Postamble)	tWPST0.5	0.45	-	0.45	-	0.45	-	tCK(avg)
DQS_t, DQS_c differential WRITE Postamble (1.5tCK Postamble)	tWPST1.5	-	-	1.20	-	1.20	-	tCK(avg)
DQS_t, DQS_c differential high toggle pulse width during DDR4 READ Preamble (2tCK Preamble)	tDQSH2PRE_D4	1.350	-	1.350	-	1.350	-	tCK(avg)
DQS_t, DQS_c differential initial low pulse width during Preamble (2tCK Preamble)	tDQSL2PRE	0.900	-	0.900	-	0.900	-	tCK(avg)
DQS_t, DQS_c differential initial low pulse width during Preamble (3tCK Preamble)	tDQSL3PRE	-	-	1.800	-	1.800	-	tCK(avg)
DQS_t, DQS_c differential initial low pulse width during READ Preamble (4tCK Preamble)	tDQSL4PRE	-	-	-	-	-	-	tCK(avg)
DQS_t, DQS_c differential initial low pulse width during WRITE Preamble (4tCK Preamble)	tDQSL4PRE	-	-	1.800	-	1.800	-	tCK(avg)
DQS_t, DQS_c differential high toggle pulse width during WRITE Preamble	tDQSH_pre	0.395	0.605	0.395	0.605	0.430	0.570	tCK(avg)
DQS_t, DQS_c differential low toggle pulse width during WRITE Preamble	tDQSL_pre	0.395	0.605	0.395	0.605	0.430	0.570	tCK(avg)

NOTES:

1. The 1tCK Read Preamble is valid for the DDR5-3200/3600 speed grades.
2. The 2tCK Read and Write Preamble is valid for the DDR5-3200/3600/4000/4400/4800 speed grades.
3. The 2tCK DDR4 Read Preamble is valid for the DDR5-3200/3600/4000/4400/4800 speed grades.
4. The 3tCK Read and Write Preamble is valid for the DDR5-4000/4400/4800/5200/5600/6000/6400 speed grades.
5. The 4tCK Read Preamble is valid for the 5600/6000/6400/6800/7200/7600/8000/8400/8800/9200 speed grades.
6. The 4tCK Write Preamble is valid for the 4000/4400/4800/5200/5600/6000/6400/6800/7200/7600/8000/8400/8800/9200 speed grades.
6. The 0.5tCK Read and Write Postamble is valid for the DDR5-3200/3600/4000/4400/4800 speed grades.
7. The 1.5tCK Read Postamble is valid for the DDR5-3200/3600/4000/4400/4800/5200/5600/6000/6400/6800/7200/7600/8000/8400/8800/9200 speed grades.
8. The 1.5tCK Write Postamble is valid for the DDR5-4000/4400/4800/5200/5600/6000/6400/6800/7200/7600/8000/8400/8800/9200 speed grades.
9. The strobe preamble and postamble timing parameter values shall follow the operating frequency.

4.4.3 Read and Write Preamble and Postamble Timings (cont'd)

Table 38 — Strobe Preamble and Postamble Timing Parameters for DDR5-5200 to 9200

Parameter	Symbol	DDR5 5200		DDR5 5600 - 6400		DDR5 6800 - 7200		DDR5 7600- 9200		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
DQS_t, DQS_c differential READ Preamble (1tCK Preamble)	tRPRE1	-	-	-	-	-	-	-	-	tCK(avg)
DQS_t, DQS_c differential READ Preamble (2tCK Preamble)	tRPRE2	-	-	-	-	-	-	-	-	tCK(avg)
DQS_t, DQS_c differential READ Preamble DDR4 (2tCK Preamble)	tRPRE2_D4	2.700	-	2.700	-	-	-	-	-	tCK(avg)
DQS_t, DQS_c differential READ Preamble (3tCK Preamble)	tRPRE3	2.700	-	2.700	-	-	-	-	-	tCK(avg)
DQS_t, DQS_c differential READ Preamble (4tCK Preamble)	tRPRE4	-	-	3.600	-	3.600	-	3.600	-	tCK(avg)
DQS_t, DQS_c differential READ Postamble (0.5tCK Preamble)	tRPST0.5	-	-	-	-	-	-	-	-	tCK(avg)
DQS_t, DQS_c differential READ Postamble (1.5tCK Preamble)	tRPST1.5	1.200	-	1.200	-	1.200	-	1.300	-	tCK(avg)
DQS_t, DQS_c differential WRITE Preamble (2tCK Preamble)	tWPRE2	-	-	-	-	-	-	-	-	tCK(avg)
DQS_t, DQS_c differential WRITE Preamble (3tCK Preamble)	tWPRE3	2.700	-	2.700	-	-	-	-	-	tCK(avg)
DQS_t, DQS_c differential WRITE Preamble (4tCK Preamble)	tWPRE4	3.600	-	3.600	-	3.600	-	3.600	-	tCK(avg)
DQS_t, DQS_c differential WRITE Postamble (0.5tCK Postamble)	tWPST0.5	-	-	-	-	-	-	-	-	tCK(avg)
DQS_t, DQS_c differential WRITE Postamble (1.5tCK Postamble)	tWPST1.5	1.200	-	1.200	-	1.200	-	1.200	-	tCK(avg)
DQS_t, DQS_c differential high toggle pulse width during DDR4 READ Preamble (2tCK Preamble)	tDQSH2PRE_D4	-	-	-	-	-	-	-	-	tCK(avg)
DQS_t, DQS_c differential initial low pulse width during WRITE Preamble (2tCK Preamble)	tDQSL2PRE	-	-	-	-	-	-	-	-	tCK(avg)
DQS_t, DQS_c differential initial low pulse width during Preamble (3tCK Preamble)	tDQSL3PRE	1.800	-	1.800	-	-	-	-	-	tCK(avg)
DQS_t, DQS_c differential initial low pulse width during READ Preamble (4tCK Preamble)	tDQSL4PRE	-	-	1.800	-	1.800	-	1.800	-	tCK(avg)
DQS_t, DQS_c differential initial low pulse width during WRITE Preamble (4tCK Preamble)	tDQSL4PRE	1.800	-	1.800	-	1.800	-	1.800	-	tCK(avg)
DQS_t, DQS_c differential high toggle pulse width during WRITE Preamble	tDQSH_pre	0.430	0.570	0.430	0.570	0.450	0.550	0.450	0.550	tCK(avg)
DQS_t, DQS_c differential low toggle pulse width during WRITE Preamble	tDQSL_pre	0.430	0.570	0.430	0.570	0.450	0.550	0.450	0.550	tCK(avg)

NOTES:

1. The 1tCK Read Preamble is valid for the DDR5-3200/3600 speed grades.
2. The 2tCK Read and Write Preamble is valid for the DDR5-3200/3600/4000/4400/4800 speed grades.
3. the 2tCK DDR4 Read Preamble is valid for the DDR5-3200/3600/4000/4400/4800 speed grades.
4. The 3tCK Read and Write Preamble is valid for the DDR5-4000/4400/4800/5200/5600/6000/6400 speed grades.
5. The 4tCK Read Preamble is valid for the DDR5-5600/6000/6400/6800/7200/7600/8000/8400/8800/9200 speed grades.
6. The 4tCK Write Preamble is valid for the DDR5-4000/4400/4800/5200/5600/6000/6400/6800/7200/7600/8000/8400/8800/9200 speed grades.
7. The 0.5tCK Read and Write Postamble is valid for the DDR5-3200/3600/4000/4400/4800 speed grades.
8. The 1.5tCK Read Postamble is valid for the DDR5-3200/3600/4000/4400/4800/5200/5600/6000/6400/6800/7200/7600/8000/8400/8800/9200 speed grades.
9. The 1.5tCK Write Postamble is valid for the DDR5-4000/4400/4800/5200/5600/6000/6400/6800/7200/7600/8000/8400/8800 speed grades.
10. The strobe preamble and postamble timing parameter values shall follow the operating frequency.

4.4.4 tWPRE and tRRPE Measurement

tWPRE and tRPRE are measured from a starting point at VswM HIGH or LOW (as defined in the table below) to the differential crossing point of DQS_t/DQS_c corresponding to the first burst bit of data as the ending point. The method is applicable for all programmable Preamble durations.

Examples of the method for measuring the duration of tWPRE and tRPRE are shown in Figure 21:

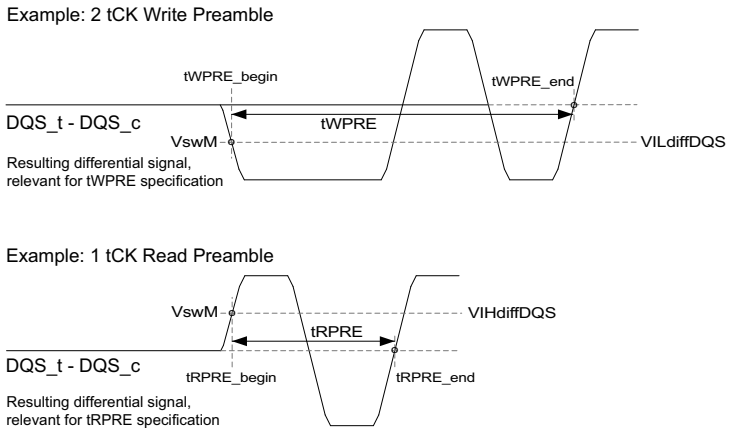


Figure 21 — Method for Measuring Preamble Start and End Points

Table 39 — VswM Reference Voltages for Preamble and Postamble Timing Measurements

Measured Parameter	Reference	Unit
VswM HIGH	VIHdiffDQS	mV
VswM LOW	VILdiffDQS	mV

4.4.5 WPST and tRPST Measurement

tWPST and tRPST are measured from a starting point at the differential crossing point of DQS_t/DQS_c corresponding to the last burst bit of data to the VswM LOW ending point. The method is applicable for all programmable Postamble durations.

Examples of the method for measuring the duration of tWPST and tRPST are shown in the Figure 22:

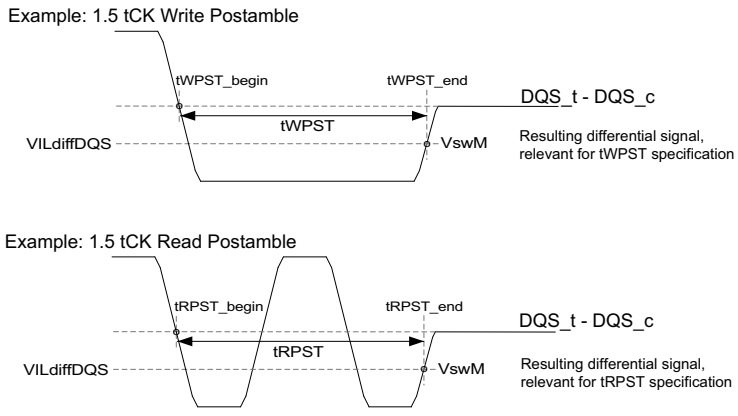


Figure 22 — Method for Measuring Postamble Start and End Points

4.5 Interamble

The DQS strobe for the device requires a preamble prior to the first latching edge (the rising edge of DQS_t with data valid), and it requires a postamble after the last latching edge. The preamble and postamble options are set via Mode Register Write commands. Additionally, the postamble and preamble configured size shall NOT force the HOST to add command gaps in the command interval just to satisfy postamble or preamble settings. (i.e., Preamble=4tCK + Postamble=1.5tCK shall not force tCCD+5).

4.5.1 Read Interamble Timing Diagrams

In Read to Read operations with tCCD=BL/2, postamble for 1st command and preamble for 2nd command shall disappear to create consecutive DQS latching edge for seamless burst operations.

In the case of Read to Read operations with command interval of tCCD+1, tCCD+2, etc., if the postamble and preambles overlap, the toggles take precedence over static preambles.

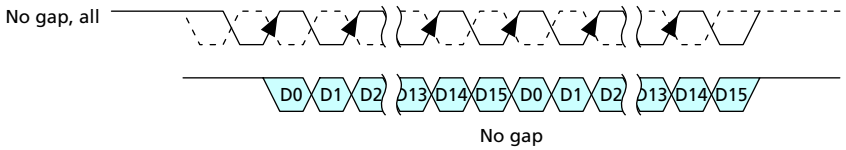


Figure 23 — Example of Seamless Reads Operation: tCCD=Min

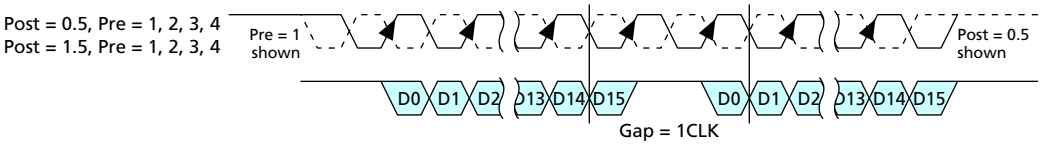


Figure 24 — Example of Consecutive Reads Operation: tCCD=Min+1

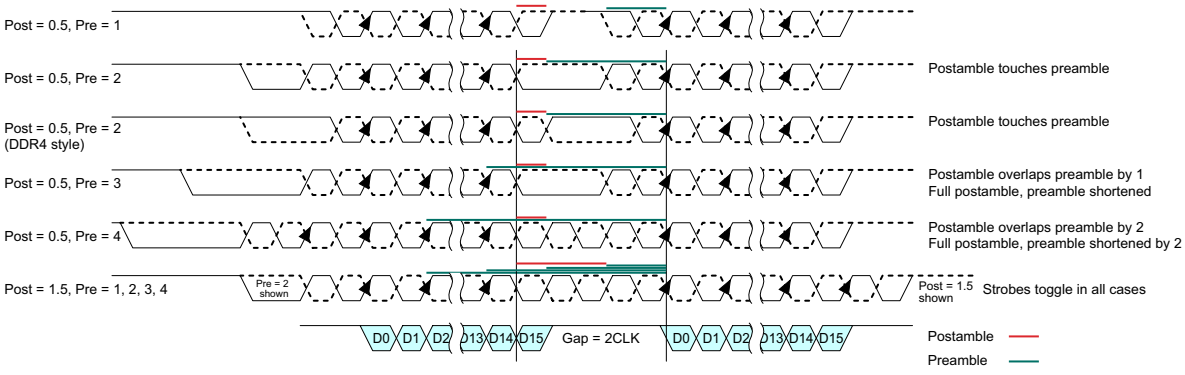


Figure 25 — Example of Consecutive Reads Operation: tCCD=Min+2

4.5.1 Read Interamble Timing Diagrams (cont'd)

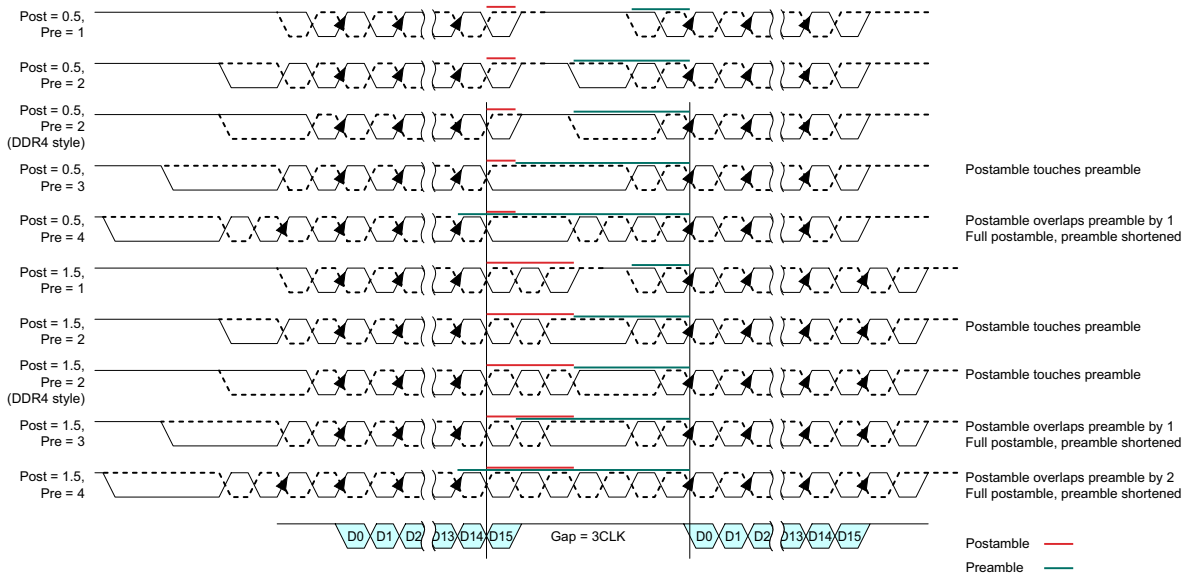


Figure 26 — Example of Consecutive Reads Operation: tCCD=Min+3

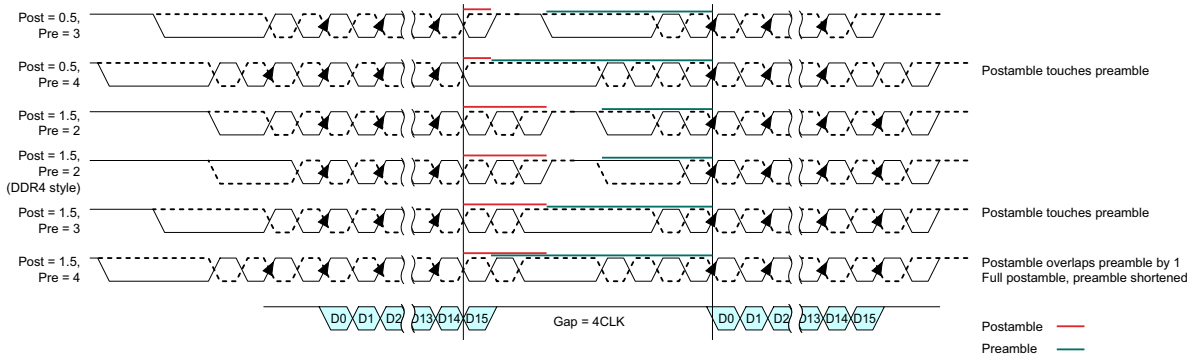


Figure 27 — Example of Consecutive Reads Operation: tCCD=Min+4

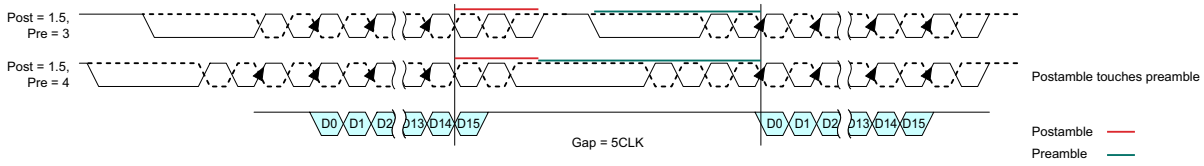


Figure 28 — Example of Consecutive Reads Operation: tCCD=Min+5

4.5.2 Write Interamble Timing Diagrams

In Write to Write operations with tCCD=BL/2, postamble for 1st command and preamble for 2nd command shall disappear to create consecutive DQS latching edge for seamless burst operations.

In the case of Write to Write operations with command interval of tCCD+1, tCCD+2, etc., if the postamble and preambles overlap, the toggles take precedence over static preambles.

When the DFE is enabled, the DQs shall be high during Interamble for a minimum of 4UI prior to the first Write data bit of the second Write command. If there are 4UI or less and DFE is enabled, the host shall drive DQs high during the full Write Interamble period.

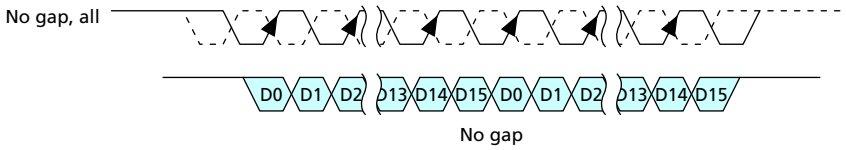


Figure 29 — Example of Seamless Writes Operation: tCCD=Min

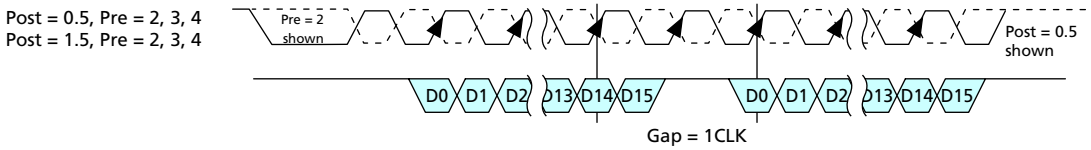


Figure 30 — Example of Consecutive Writes Operation: tCCD=Min+1

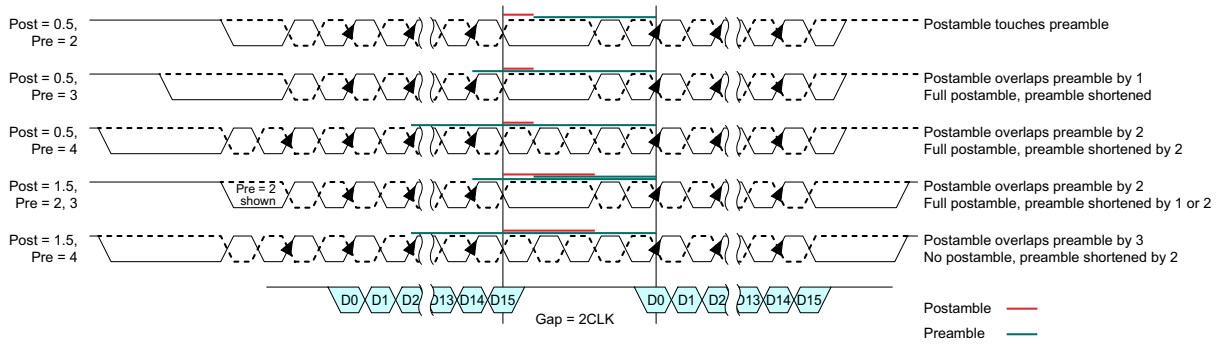


Figure 31 — Example of Consecutive Writes Operation: tCCD=Min+2

4.5.2 Write Interamble Timing Diagrams (cont'd)

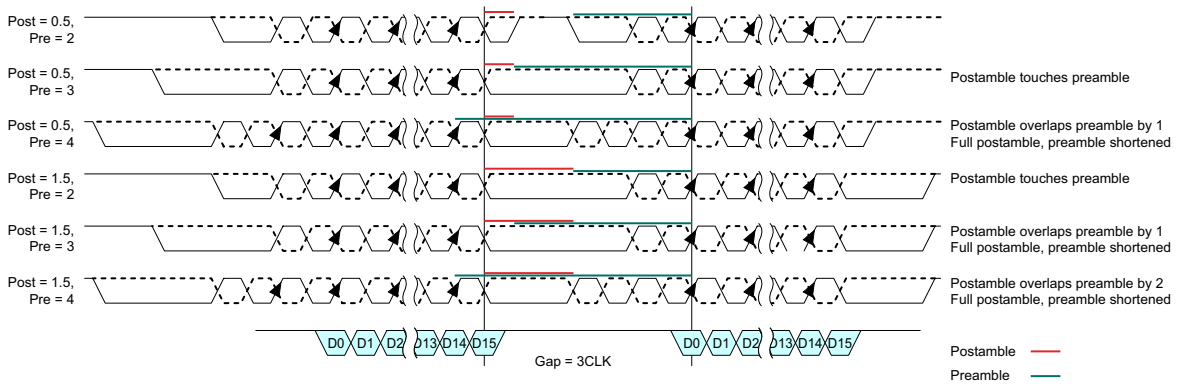


Figure 32 — Example of Consecutive Writes Operation: tCCD=Min+3

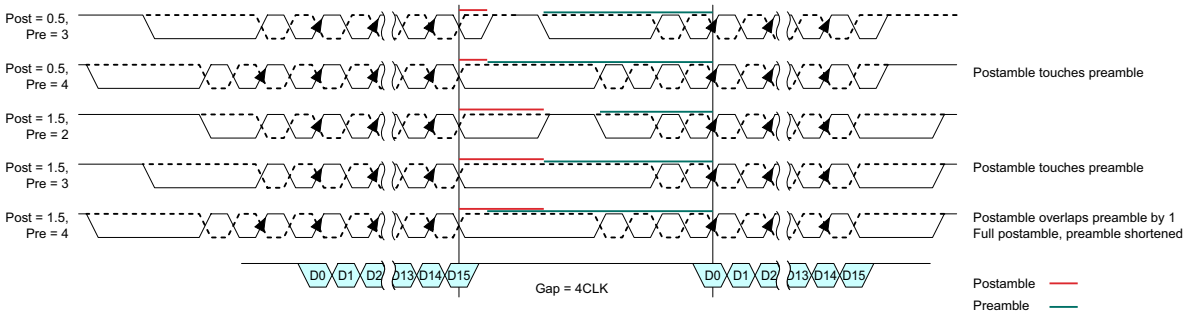


Figure 33 — Example of Consecutive Writes Operation: tCCD=Min+4

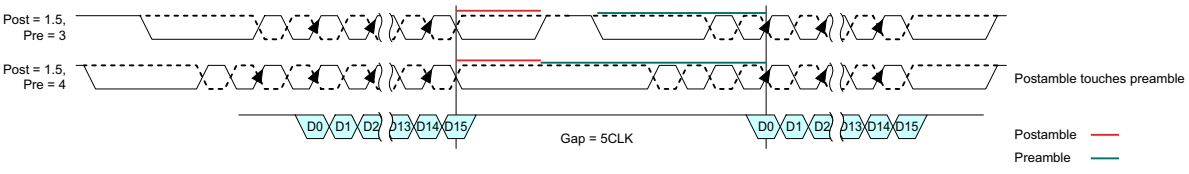


Figure 34 — Example of Consecutive Writes Operation: tCCD=Min+5

4.6 Activate Command

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BG[2:0] in X4/8 and BG[1:0] in X16 select the bankgroup; BA[1:0] inputs selects the bank within the bankgroup, and the address provided on the appropriate CA pins for R[17:0] to select the row (see Table 40 below). In the case of a 3DS DDR5 SDRAM device, the CID[3:0] shall also be selected to identify the correct die in the stack. This row remains active (or open) for accesses until a precharge command is issued to that bank or a precharge all command is issued. A bank must be precharged before opening a different row in the same bank.

Bank-to-bank command timing for ACTIVATE commands uses two different timing parameters, depending on whether the banks are in the same or different bank group. tRRD_S (short) is used for timing between banks located in different bank groups. tRRD_L (long) is used for timing between banks located in the same bank group. Consecutive ACTIVATE commands, allowed to be issued at tRRDmin, are restricted to a maximum of four within the time period tFAW (four activate window).

Table 40 — Activate Command (for Reference)

Function	Abbre-viation	CS_n	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Activate	ACT	L	L	L	R0	R1	R2	R3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	1
		H	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	CID3/R17	
NOTE 1 See Command Truth Table for details																	

4.6.1 Non-Binary Density Considerations

An ACT command with row address inputs which violate the 'MSB address bit “HIGH”, MSB-1 address bit “LOW”' non-binary density address restriction shall follow all timing and protocol rules as though the ACT were valid.

Any RD or RDA command following an ACT to the invalid address space within the same bank shall drive the DQS strobes with normal timing but shall not output data on the DQs that can be used to learn about data stored in cells with valid addresses. DQ data that coincidentally matches cell array data is permissible (for example: always sending the all 1s and cell data sometimes being all 1s). Consistently exposing data from a previous read or previous activate is not permissible.

Any WR, WRA, WRP or WRPA command following an ACT to the invalid address space within the same bank shall not result in new databeing written anywhere within the DRAM.

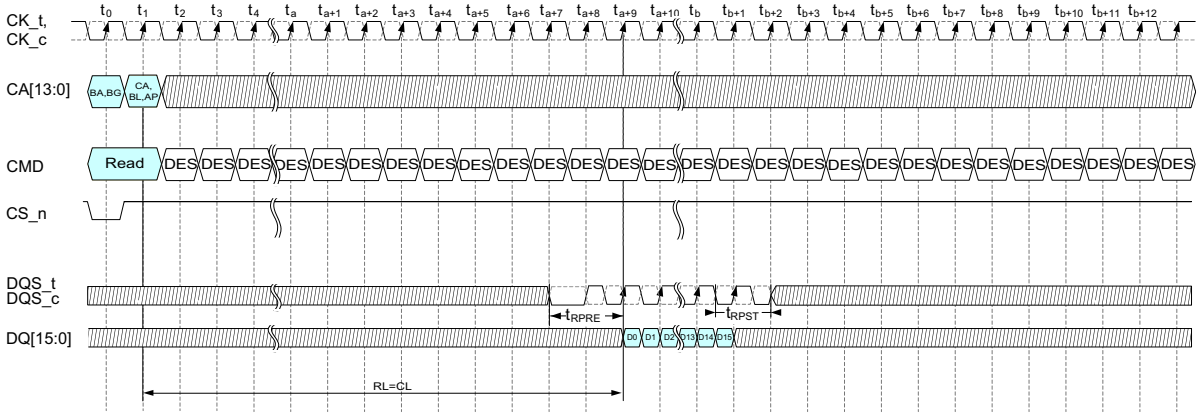
The DRAM will operate normally for Read and Write commands to banks which have pages open for valid rows.

4.7 Read Operation

The Read Operation causes the DRAM to retrieve and output data stored in its array. The Read Operation is initiated by the Read Command during which the beginning column address and bank/group address for the data to be retrieved from the array is provided. The data is driven by the DRAM on its DQ pins RL (CL) cycles after the Read Command along with the proper waveform on the DQS inputs. Read Latency (RL or CL) is defined from the Read command to data and is not affected by the Read DQS offset timing (MR40 OP[2:0]).

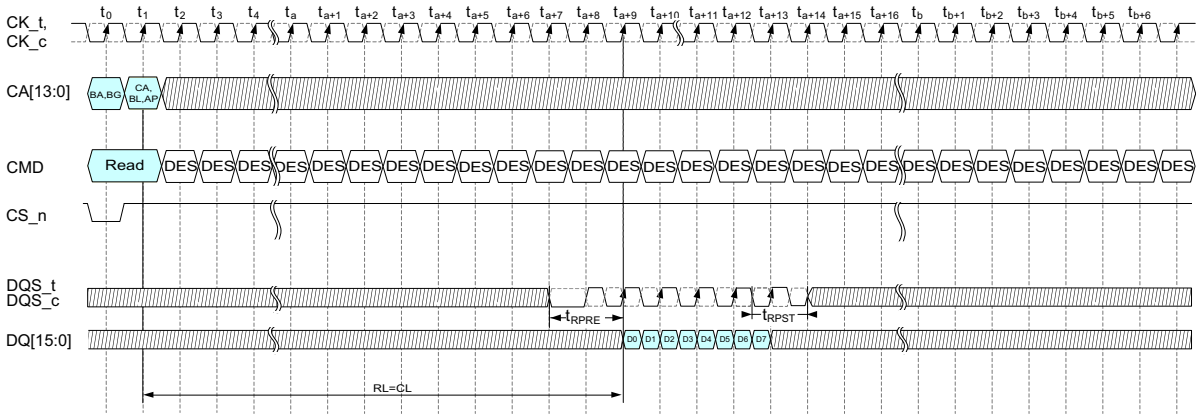
4.7.1 READ Burst Operation

During a READ or WRITE command, DDR5 shall support BC8, BL16, BL32 (optional) and BL32 OTF (optional) during the READ or WRITE. MR0[1:0] is used to select burst operation mode.



NOTES:
1. BL=16, Preamble = 2tCK - 0010 Pattern Preamble, 1.5tCK Postamble
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. In this example, Read DQS Offset Timing is set to 0 Clocks.

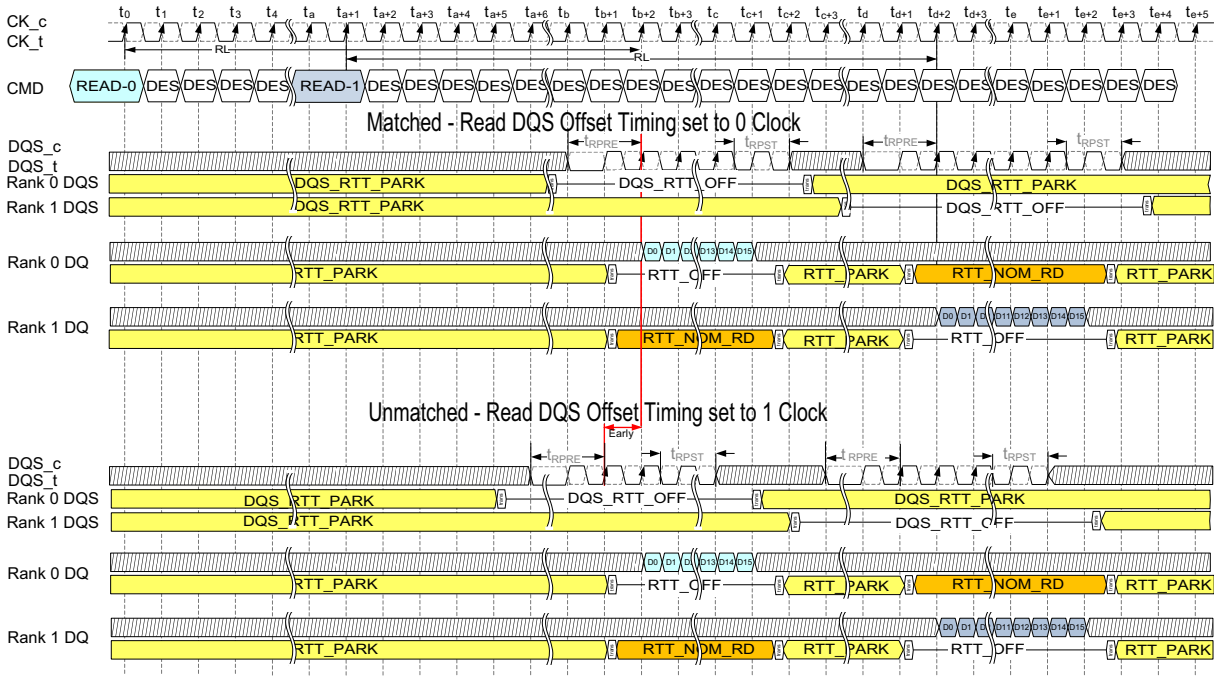
Figure 35 — READ Burst Operation (BL16)



NOTES:
1. BC=8, Preamble = 2tCK - 0010 Pattern Preamble, 1.5tCK Postamble
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. In this example, Read DQS Offset Timing is set to 0 Clocks
4. In non-CRC mode, DQS_t and DQS_c stop toggling at the completion of the BC8 data bursts, plus the postamble.

Figure 36 — Read Burst Operation (BC8)

4.7.1 READ Burst Operation (cont'd)



NOTES:

1. BL=16, Preamble = 2tCK - 0010 Pattern Preamble, 1.5tCK Postamble
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. Two different examples are shown side by side, the top with the default setting for Read DQS Offset = 0 Clock, the lower with a 1 Clock setting. In the lower case, the DQS is started 1 clock earlier than normal with respect to RL (CL).
4. In both cases, the Data does not move

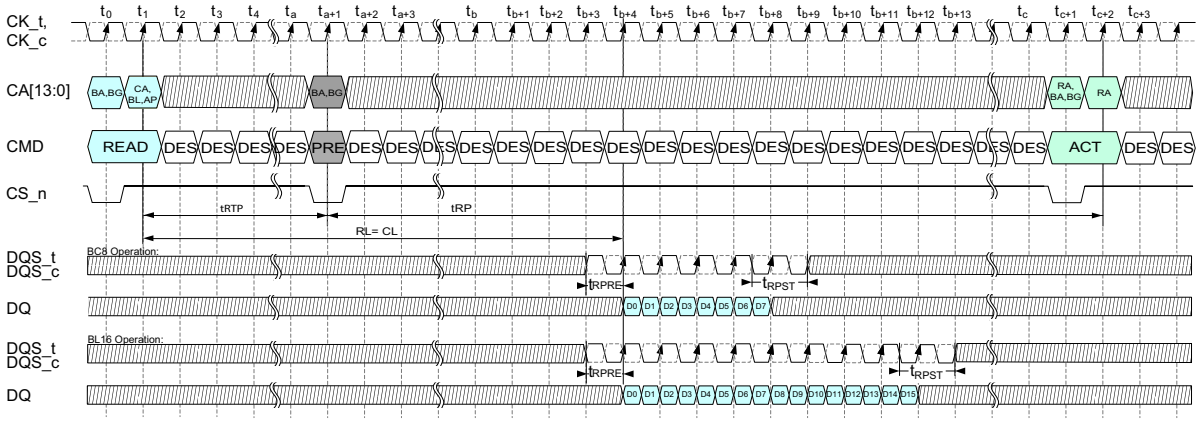
Figure 37 — READ to READ, Different Ranks Operation with Read DQS Offset Usage (BL16)

4.7.2 Burst Read Operation Followed by a Precharge

The minimum external Read command to Precharge command spacing to the same bank is equal to tRTP with tRTP being the Internal Read Command to Precharge Command Delay. Note that the minimum ACT to PRE timing, tRAS, must be satisfied as well. The minimum value for the Internal Read Command to Precharge Command Delay is given by tRTP.min. A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

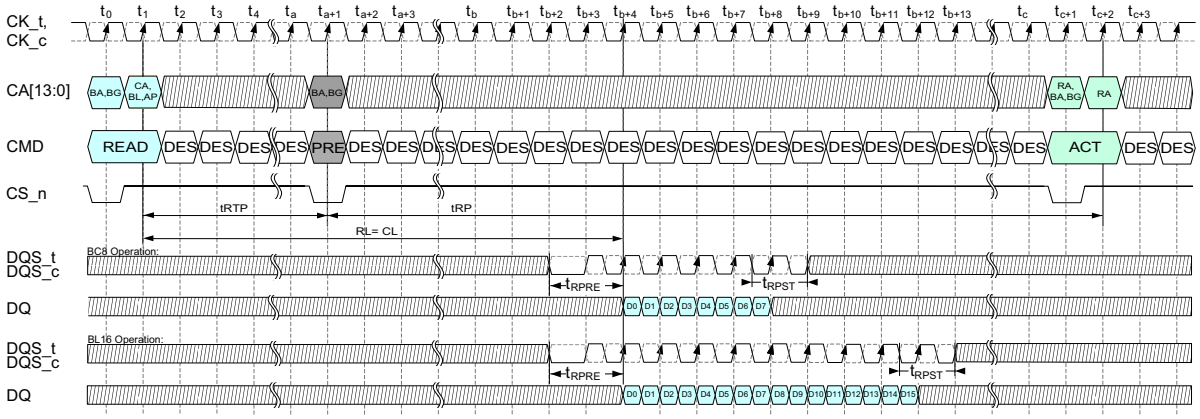
1. The minimum RAS precharge time (tRP.MIN) has been satisfied from the clock at which the precharge begins.
2. The minimum RAS cycle time (tRC.MIN) from the previous bank activation has been satisfied.

Examples of Read commands followed by Precharge are shown in Figure 38 and Figure 39.



NOTES:
1. BL = 16, 1tCK Preamble, 1.5tCK Postamble
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. The example assumes tRAS. MIN is satisfied at Precharge command time(ta+1) and that tRC. MIN is satisfied at the next Active command time(tc+2).

Figure 38 — READ to PRECHARGE with 1tCK Preamble



NOTES:
1. BL = 16, 2tCK - 0010 Pattern Preamble, 1.5tCK Postamble,
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. The example assumes tRAS. MIN is satisfied at Precharge command time(ta+1) and that tRC. MIN is satisfied at the next Active command time(tc+2).

Figure 39 — READ to PRECHARGE with 2tCK Preamble

4.7.2.1 CLK to Read DQS Timing Parameters

Following parameters shall be defined for CK to read DQS timings.

Table 41 — CLK to Read DQS Timing Parameters DDR5-3200 to DDR5-4800

Speed		DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	tDQSCK	-0.240	0.240	-0.252	0.252	-0.270	0.270	-0.286	0.286	-0.300	0.300	tCK	1, 4, 5
DQS_t, DQS_c rising edge output variance window	tDQSCKi	-	0.410	-	0.430	-	0.460	-	0.475	-	0.490	tCK	2, 3, 4, 5, 6

NOTE 1 Measured over full VDD and Temperature spec ranges.
NOTE 2 Measured for a given DRAM part, and for each DQS_t/DQS_c pair in case of x16 (part variation is excluded).
NOTE 3 These parameters are verified by design and characterization, and may not be subject to production test.
NOTE 4 Assume no jitter on input clock signals to the DRAM.
NOTE 5 Refer to Clause 4.7.1 READ Timing Definitions.
NOTE 6 Measured at a fixed and constant VDD and Temperature condition.

Table 42 — CLK to Read DQS Timing Parameters DDR5-5200 to DDR5-6800

Speed		DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		DDR5-6800		Units	NOTE
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	tDQSCK	-0.313	0.313	-0.325	0.325	-0.337	0.337	-0.348	0.348	-0.359	0.359	tCK	1, 4, 5
DQS_t, DQS_c rising edge output variance window	tDQSCKi	-	0.510	-	0.530	-	0.549	-	0.567	-	0.585	tCK	2, 3, 4, 5, 6

NOTE 1 Measured over full VDD and Temperature spec ranges.
NOTE 2 Measured for a given DRAM part, and for each DQS_t/DQS_c pair in case of x16 (part variation is excluded).
NOTE 3 These parameters are verified by design and characterization, and may not be subject to production test.
NOTE 4 Assume no jitter on input clock signals to the DRAM.
NOTE 5 Refer to Clause 4.7.1 READ Timing Definitions.
NOTE 6 Measured at a fixed and constant VDD and Temperature condition.

Table 43 — CLK to Read DQS Timing Parameters DDR5-7200 to DDR5-9200

Speed		DDR5-7200		DDR5-7600		DDR5-8000		DDR5-8400		DDR5-8800		DDR5-9200		Units	NOTE
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	tDQSCK	-0.370	0.370	-0.380	0.380	-0.390	0.390	-0.400	0.400	-0.410	0.410	-0.420	0.420	tCK	1, 4, 5
DQS_t, DQS_c rising edge output variance window	tDQSCKi	-	0.602	-	0.619	-	0.635	-	0.651	-	0.667	-	0.682	tCK	2, 3, 4, 5, 6

NOTE 1 Measured over full VDD and Temperature spec ranges.
NOTE 2 Measured for a given DRAM part, and for each DQS_t/DQS_c pair in case of x16 (part variation is excluded).
NOTE 3 These parameters are verified by design and characterization, and may not be subject to production test.
NOTE 4 Assume no jitter on input clock signals to the DRAM.
NOTE 5 Refer to Clause 4.7.1 READ Timing Definitions.
NOTE 6 Measured at a fixed and constant VDD and Temperature condition.

4.7.2.1 CLK to Read DQS Timing Parameters (cont'd)

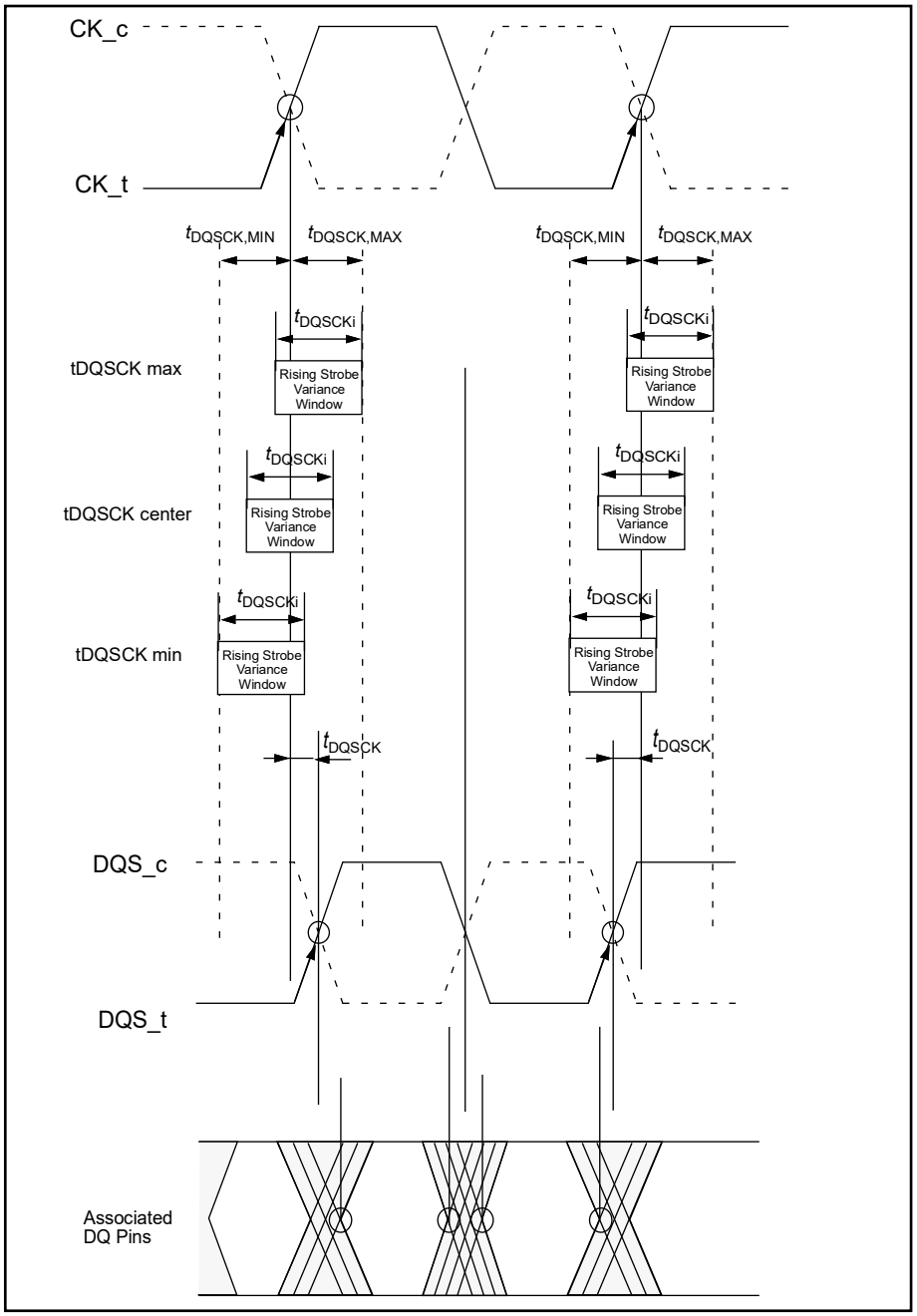


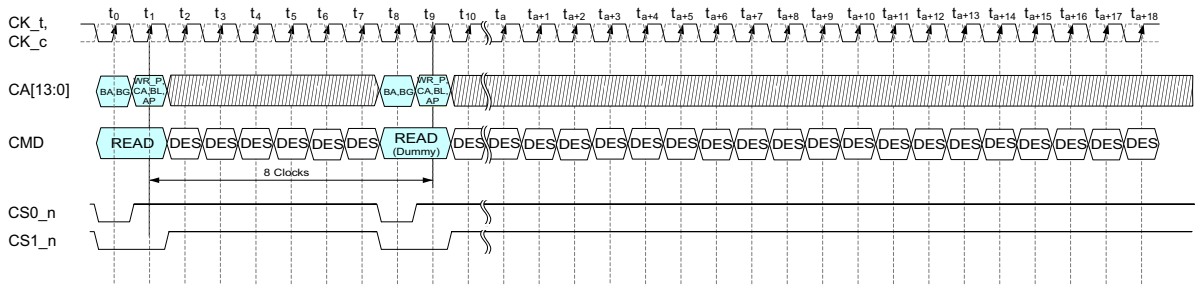
Figure 40 — TDQSCK Timing Definition

4.7.3 Read Burst Operation for Optional BL32 Mode

The following read timing diagrams cover read timings for fixed BL32 BL32 in BL32 OTF mode and BL16 in BL32 OTF mode for x4 devices only.

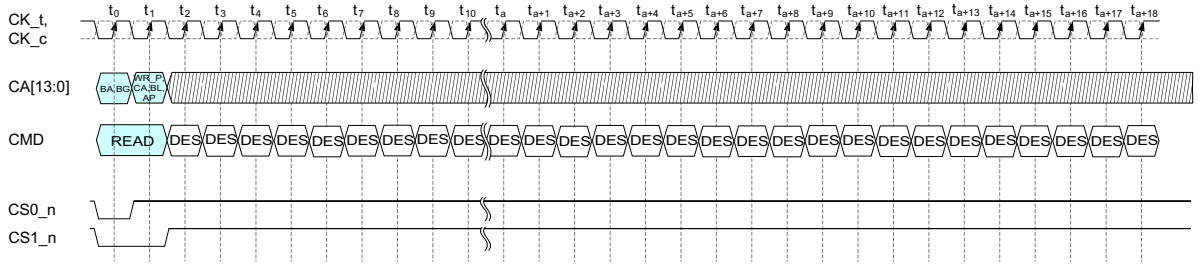
In these read timing diagrams, for clarity of illustration, CK and DQS are shown aligned. As well, DQS and DQ are shown edge-aligned. Offset between CK and DQS, and between DQS and DQ may be appropriate.

A dummy CAS command is required for second half of the transfer of BL32. If non-target ODT is needed in the system then a dummy ODT command must be issued to the non-target rank for second half of the transfer of BL32.



NOTES:
1. DES commands are shown for ease of illustration; other commands may be valid at these times.
2. A dummy RD command is required for the second half of the transfer with a delay of 8 clocks from the first RD command.
3. The figure also shows a dummy ODT command being issued to non-target rank 1 for the second half of the transfer.
4. C10 is used for burst ordering and can be LOW or HIGH for the first RD command. C10 for the dummy RD command must be the opposite value from the first RD command.
5. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.
6. CA bits other than C10 and AP in dummy CAS command are the same as the first CAS command.

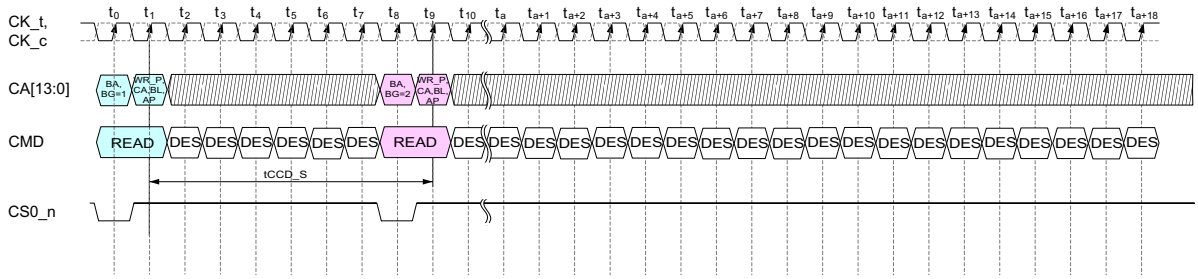
Figure 41 — Read Timing for fixed BL32 and BL32 in BL32 OTF Mode



NOTES:
1. Figure shows BL16 read operation when MR0 is programmed to use BL32 OTF mode. In this case, no dummy RD command is required as transfer size is BL16.
2. DES commands are shown for ease of illustration; other commands may be valid at these times including commands to allow data transfer from the same die after transfer of BL16.
3. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

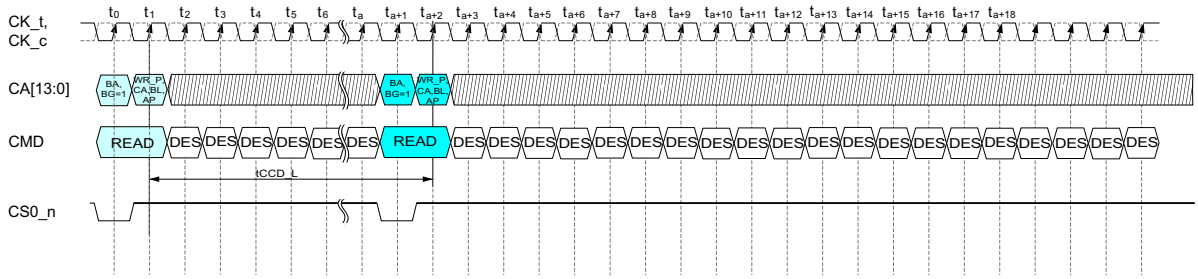
Figure 42 — Read Timings for BL16 in BL32 OTF Mode

4.7.3 Read Burst Operation for Optional BL32 Mode (cont'd)



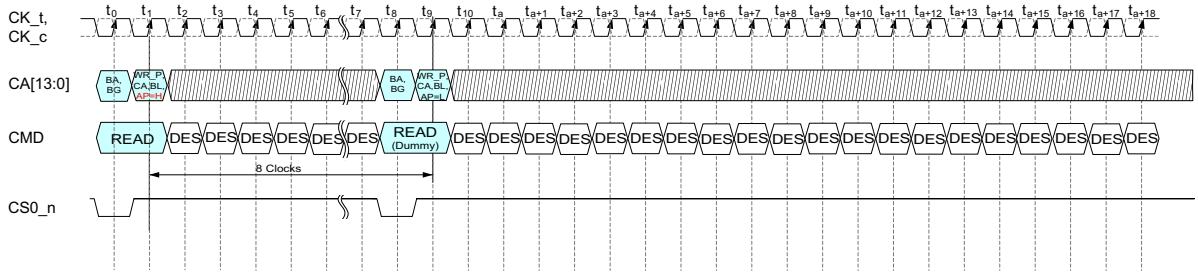
NOTES:
1. Figure shows back to back BL16 writes to different bank groups.
2. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

Figure 43 — Read to Read to Different Bank Group for BL16 in BL32 OTF



NOTES::
1. Figure shows back to back BL16 reads to same bank group using a timing of tCCD_L.
2. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

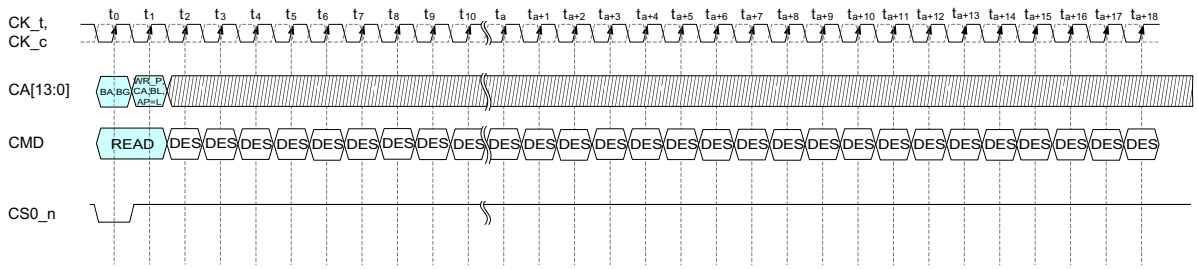
Figure 44 — Read to Read to Same Bank Group for BL16 in BL32 OTF



NOTES:
1. AP bit must be set HIGH for first CAS and LOW for dummy CAS command.
2. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.
3. CA bits other than C10 and AP in dummy CAS command are the same as the first CAS command.

Figure 45 — Read with Auto-Precharge for Fixed BL32 and BL32 in BL32 OTF Mode

4.7.3 Read Burst Operation for Optional BL32 Mode (cont'd)



NOTES:
1. AP bit must be set to LOW with the CAS command.
2. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

Figure 46 — Read with Auto-Precharge for BL16 in BL32 OTF Mode

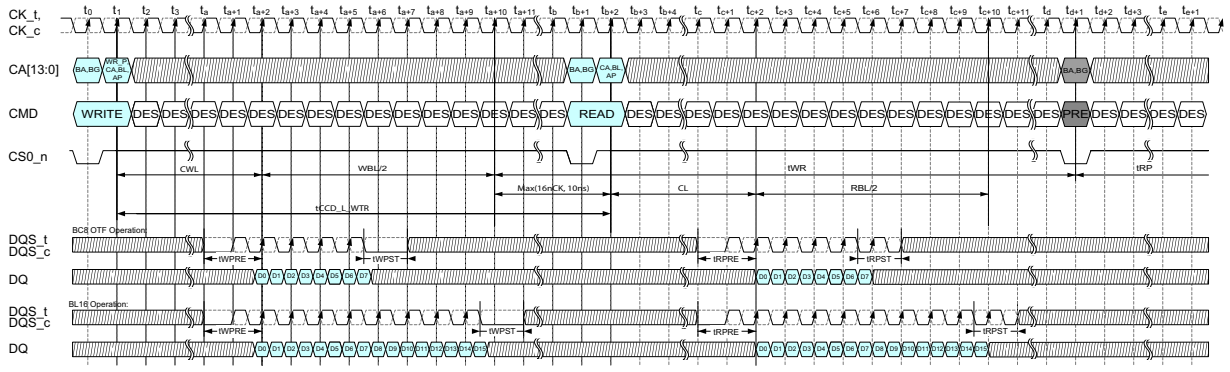
4.7.4 Read and Write Command Interval

Table 44 — Minimum Read and Write Command Timings

Bank Group	Timing Parameter	DDR5-3200 ~ 9200	Units	Notes
same	Minimum Read to Write	tCCD_L_RTW		1, 3, 4
	Minimum Write to Read	tCCD_L_WTR		2, 4
	Minimum Write to Read AP, same bank	tCCD_WTRA		2, 4
different	Minimum Read to Write	tCCD_S_RTW		1, 3, 4
	Minimum Write to Read	tCCD_S_WTR		2, 4

NOTE 1 RBL: Read burst length associated with Read command
RBL = 32 (36 w/ RCRC on) for fixed BL32 and BL32 in BL32 OTF mode
RBL = 16 (18 w/ RCRC on) for fixed BL16 and BL16 in BL32 OTF mode
RBL = 16 (18 w/ RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
NOTE 2 WBL: Write burst length associated with Write command
WBL = 32 (36 w/ WCRC on) for fixed BL32 and BL32 in BL32 OTF mode
WBL = 16 (18 w/ WCRC on) for fixed BL16 and BL16 in BL32 OTF mode
WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
NOTE 3 The following is considered for tRTW equation
1tCK needs to be added due to tDQS2CK
Read DQS offset timing can pull in the tRTW timing
1tCK needs to be added when 1.5tCK postamble
NOTE 4 CWL=CL-2

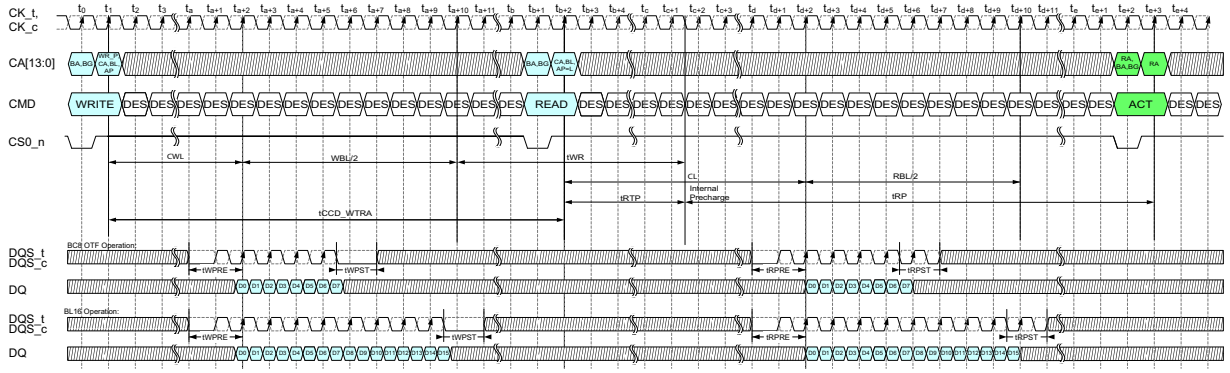
4.7.4 Read and Write Command Interval (cont'd)



NOTES:

1. BC OTF=8 or BL=16, Preamble = 2tCK - 0010 pattern, Postamble = 1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at Ta+10.
   tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.
4. The DQ signal is shown as "Don't Care" before the first Write data bit indicating DFE is disabled. When DFE is enabled, the DQ signal shall be high for a minimum of 4UI prior to the first Write data bit for proper DFE synchronization.

Figure 47 — Timing Diagram for Write to Read



NOTES:

1. BC OTF=8 or BL=16, Preamble = 2tCK - 0010 pattern, Postamble = 1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at Ta+10.
   The internal precharge after the Read AutoPrecharge command cannot begin before tWR is satisfied, which is equivalent to tWTRA + tRTP
4. The DQ signal is shown as "Don't Care" before the first Write data bit indicating DFE is disabled. When DFE is enabled, the DQ signal shall be high for a minimum of 4UI prior to the first Write data bit for proper DFE synchronization.

Figure 48 — Timing Diagram for Write to Read AutoPrecharge in Same Bank

4.7.5 Read and Write Command Interval for Optional BL32 Modes

Table 45 — Minimum Read to Read Timings - Same Bank Group

From	To		Units	Notes
	BL16 in BL32 OTF Mode	BL32 in BL32 OTF Mode		
BL16 in BL32 OTF Mode	tCCD_L	tCCD_L		1
BL32 in BL32 OTF Mode	Max(16nCK, 5ns)	Max(16nCK, 5ns)		1
NOTE 1 DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.				

Table 46 — Minimum Read to Read Timings - Different Bank Group

From	To		Units	Notes
	BL16 in BL32 OTF Mode	BL32 in BL32 OTF Mode		
BL16 in BL32 OTF Mode	tCCD_S	tCCD_S		1
BL32 in BL32 OTF Mode	2*tCCD_S	2*tCCD_S		1
NOTE 1 DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.				

Table 47 — Minimum Write to Write Timings - Same Bank Group

From	To		Units	Notes
	BL16 in BL32 OTF Mode	BL32 in BL32 OTF Mode		
BL16 in BL32 OTF Mode	tCCD_L_WR	tCCD_L_WR2		1
BL32 in BL32 OTF Mode	8nCK+tCCD_L_WR	9nCK+tCCD_L_WR2		1
NOTE 1 DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.				

DDR5 x8 and x16 devices will have different write to write same bank group timings, based on whether the second write requires a read-modify-write (RMW), the Burst Length mode of the device set by MR0: OP[1:0], and whether data masking is enabled by MR5:OP[5]. BL16 Partial Writes and BC8 Writes require a RMW on x8/x16 devices. BL16 non-partial writes do not require RMW. See Timing parameters per speed grade for details on parametric timings.

Table 48 — Minimum Write to Write Same Bank Group Timings, x8/x16 Devices

From	To			Units	Notes
	BC8	BL16 Partial Write	BL16 not Partial Write		
BC8 or BL16	tCCD_L_WR	tCCD_L_WR	tCCD_L_WR2		

Table 49 — Minimum Write to Write Timings - Different Bank Group

From	To		Units	Notes
	BL16 in BL32 OTF Mode	BL32 in BL32 OTF Mode		
BL16 in BL32 OTF Mode	tCCD_S_WR	tCCD_S_WR		1
BL32 in BL32 OTF Mode	2*tCCD_S_WR	2*tCCD_S_WR		1
NOTE 1 DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.				

4.7.6 Read and Write Command Interval for 3DS

Table 50 — Minimum Read and Write Command Timings for x4 3DS

Logical Rank	Bank Group	Parameter Name	Timing Parameter	3DS DDR5 3200 ~ 9200	Units	Note
same	same	tCCD_L_slr, tCCD_M_slr	Minimum Read to Read	See Chapter 13, Timing Parameters by Speed Grade for 3DS	nCK	
		tCCD_L_WR_slr, tCCD_M_WR_slr	Minimum Write to Write		nCK	
		tCCD_L_RTW_slr	Minimum Read to Write		nCK	
		tCCD_L_WTR_slr, tCCD_M_WTR_slr	Minimum Write to Read		nCK	
	different	tCCD_S_slr	Minimum Read to Read		nCK	
		tCCD_S_slr	Minimum Write to Write		nCK	
		tCCD_S_RTW_slr	Minimum Read to Write		nCK	
		tCCD_S_WTR_slr	Minimum Write to Read		nCK	
different	same or different	tCCD_S_dlr	Minimum Read to Read		nCK	
		tCCD_S_dlr	Minimum Write to Write		nCK	
		tCCD_S_RTW_dlr	Minimum Read to Write		nCK	
		tCCD_S_WTR_dlr	Minimum Write to Read		nCK	

4.8 Write Operation

The Write Operation stores data to the DRAM. It is initiated by the Write command during which the beginning column address and bank/group address for the data to be written to the array is provided. The data is provided to the DRAM on the DQ inputs CAS Write Latency (CWL) cycles after the Write command along with the proper waveform on the DQS inputs. CAS Write Latency is defined and measured from final cycle of the Write command to the first effective rising DQS (excluding write preamble).

4.8.1 Write Data Mask

One write data mask (DM_n) pin for each byte data group is supported on x8 and x16 DDR5 SDRAMs. The DM_n pin/function is enabled via mode register. For the x4 configuration SDRAM, the DM mode register setting must be disabled. The DM_n pin has identical timings and termination functionality on write operations as the DQ pins, as shown in Figure 43. The DM_n pin is not used for read cycles and the pin should behave like a DQ pin driving high or be terminated to RTT_PARK. When the DM function is disabled by MR, the DRAM disables the DM input and output receiver and does not expect nor drive any valid logic level.

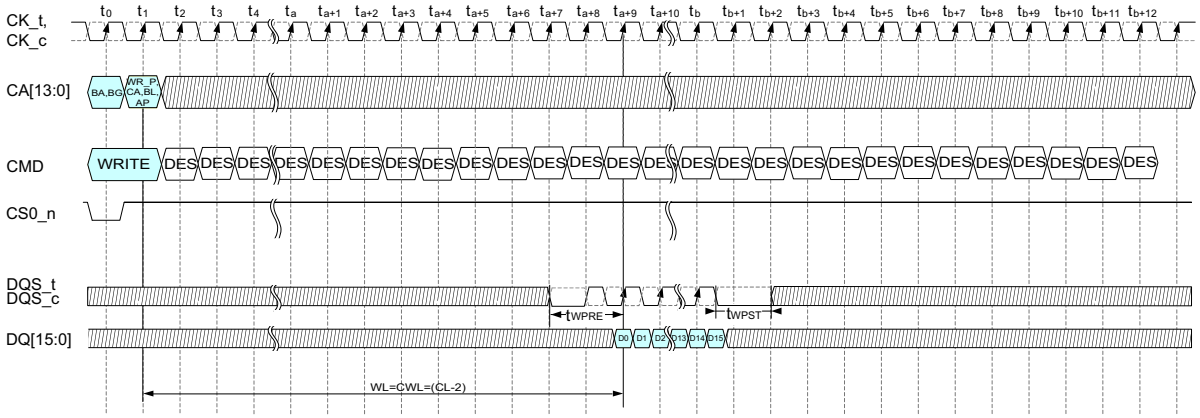
Each data mask burst bit position corresponds to the same bit position in the DQ data burst across the corresponding byte group.

The WR_Partial (WR_P) = Low as part of the write command must be used in conjunction with the DM_n data. The WR_Partial (WR_P) = Low is to help DRAM start an internal read for 'read modify write' during masked writes. If WR_Partial (WR_P) = High during write, then the mask data on DM_n must be high. If DM is disabled, MR5 OP[5] = 0, WR_Partial (WR_P) must be “H”. DM_n may be high or low.

4.8.2 Write Burst Operation

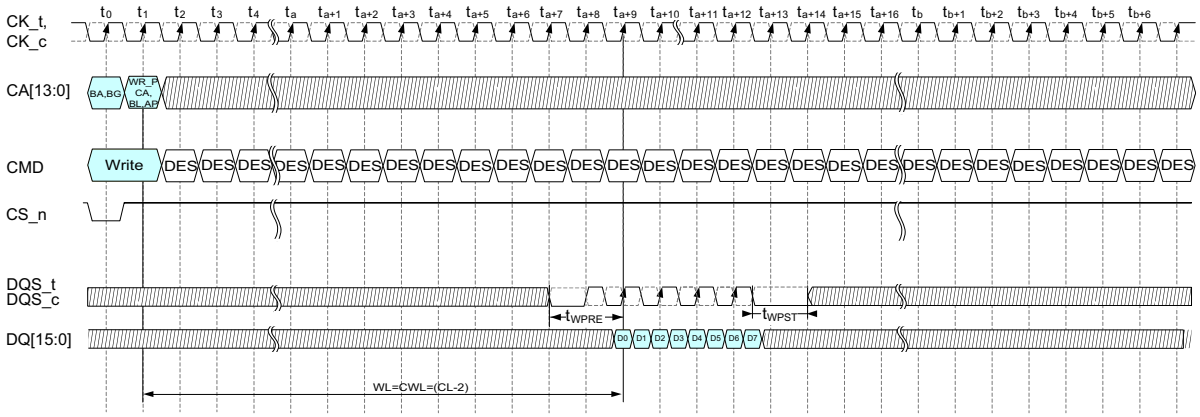
The following write timing diagrams are to help understand the meaning of each write parameter; the diagrams are just examples. The details of each parameter are defined separately.

In these write timing diagrams, for clarity of illustration, CK and DQS are shown aligned. As well, DQS and DQ are shown center-aligned. Offset between CK and DQS, and between DQS and DQ may be appropriate.



NOTES:
1. BL=16, 2tCK Preamble, 1.5tCK Postamble
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. The DQ signal is shown as “Don’t Care” before the first Write data bit indicating DFE is disabled. When DFE is enabled, the DQ signal shall be high for a minimum of 4UI prior to the first Write data bit for proper DFE synchronization.

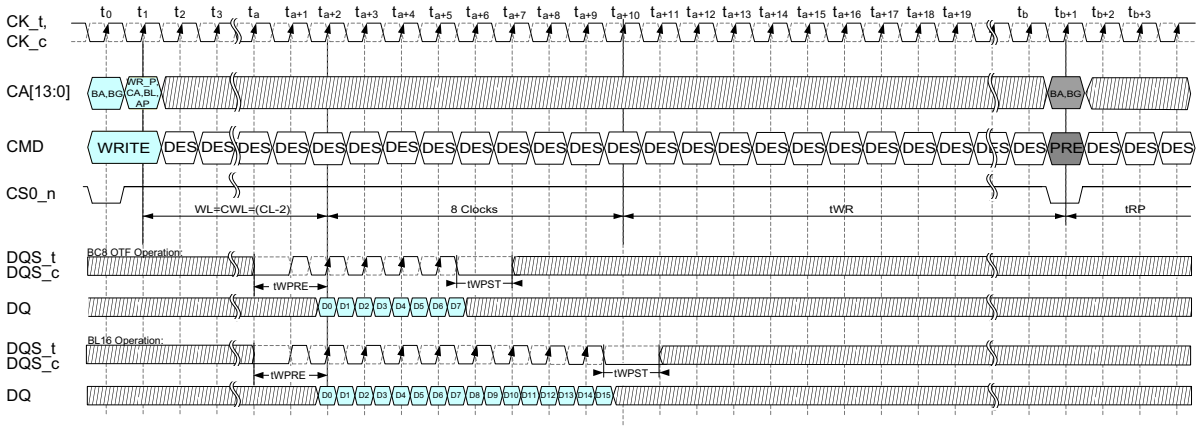
Figure 49 — WRITE Burst Operation (BL16)



NOTES:
1. BC=8, 2tCK Preamble, 1.5tCK Postamble
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. In non-CRC mode, DQS_t and DQS_c stop toggling at the completion of the BC8 data bursts, plus the postamble.
4. The DQ signal is shown as “Don’t Care” before the first Write data bit indicating DFE is disabled. When DFE is enabled, the DQ signal shall be high for a minimum of 4UI prior to the first Write data bit for proper DFE synchronization.

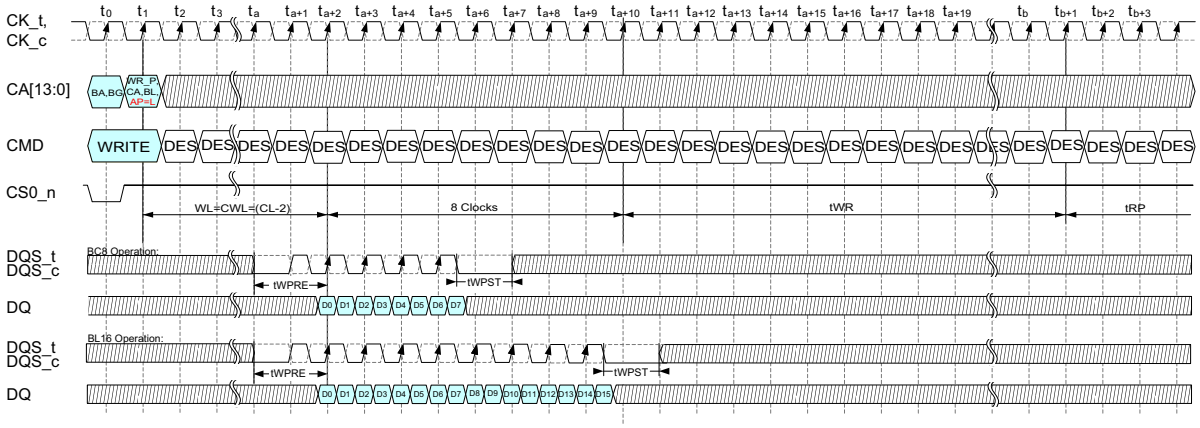
Figure 50 — Write Burst Operation (BC8)

4.8.2 Write Burst Operation (cont'd)



NOTES:
1. BC=8 or BL=16, Preamble = 2tCK - 0010 pattern, Postamble = 1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at Ta+10
   tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.
4. The DQ signal is shown as "Don't Care" before the first Write data bit indicating DFE is disabled. When DFE is enabled, the DQ signal shall be high for a minimum of 4UI prior to the first Write data bit for proper DFE synchronization.

Figure 51 — WRITE (BL16) to PRECHARGE Operation with 2tCK Preamble

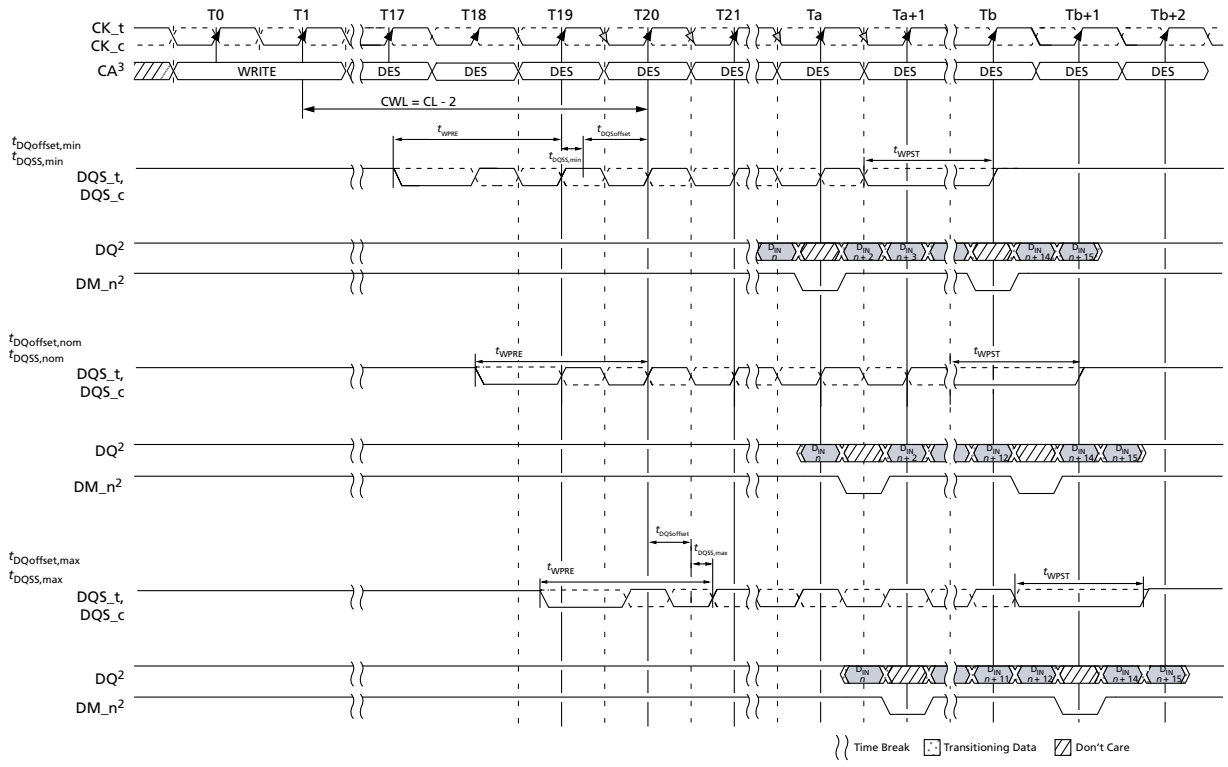


NOTES:
1. BC OTF=8 or BL=16, Preamble = 2tCK - 0010 pattern, Postamble = 1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. The write recovery time (WR) is referenced from the first rising clock edge after the last write data shown at Ta+10.
   WR specifies the last burst write cycle until the precharge command can be issued to the same bank.
4. The DQ signal is shown as "Don't Care" before the first Write data bit indicating DFE is disabled. When DFE is enabled, the DQ signal shall be high for a minimum of 4UI prior to the first Write data bit for proper DFE synchronization.

Figure 52 — WRITE (BL16) with Auto PRECHARGE Operation and 2tCK Preamble

4.8.3 Write Timing Parameters

Figure 53 is for example only to enumerate the strobe edges for a particular write burst. For a valid burst, all timing parameters for each edge of a burst must be satisfied.



NOTES:

1. BL=16, Preamble=2CK - 0010 pattern, Postamble=1.5CK,
2. DES commands are shown for ease of illustration, other commands may be valid at these times.
3. *t*DQSS must be met at each rising clock edge.
4. Figure assumes DRAM internal WL training complete.
5. DQ/DM_n pulse timing and DQS to DQ skew defined by Rx Strobe Jitter Sensitivity Specifications for the respective speed bin.

Figure 53 — DDR5 Write Timing Parameters

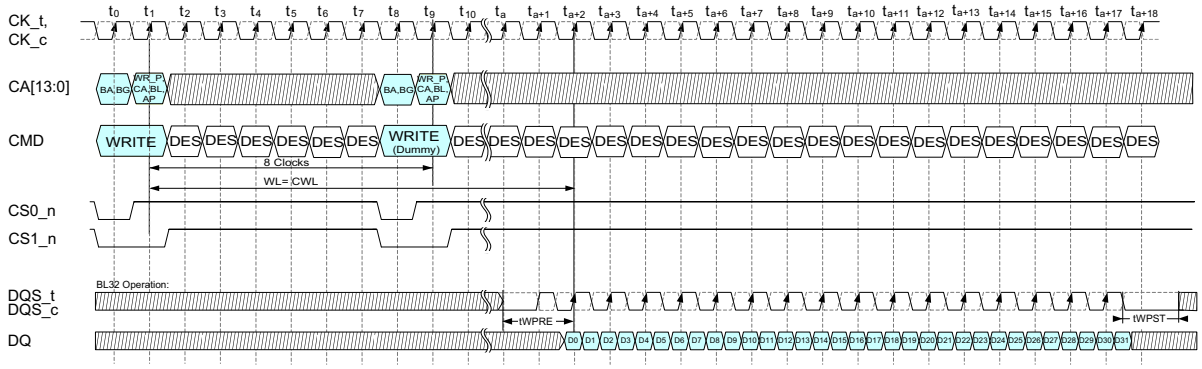
4.8.4 Write Burst Operation for Optional BL32 Mode

The following write timing diagrams cover write timings for fixed BL32, BL32 in BL32 OTF mode and BL16 in BL32 OTF mode for x4 devices only.

In these write timing diagrams, for clarity of illustration, CK and DQS are shown aligned. As well, DQS and DQ are shown center-aligned. Offset between CK and DQS, and between DQS and DQ may be appropriate.

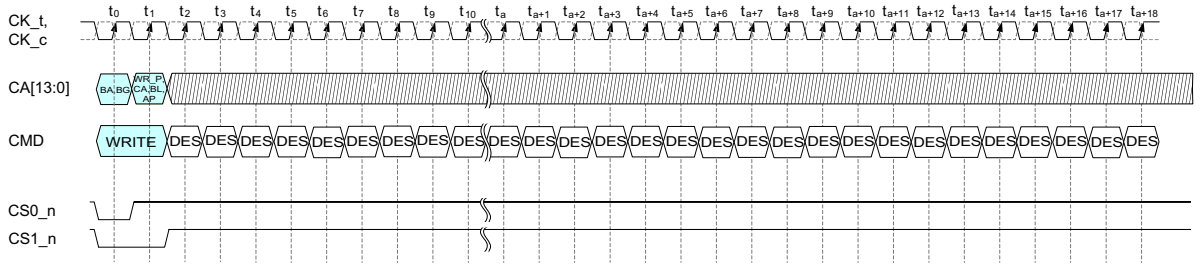
A dummy CAS command is required for second half of the transfer of BL32. If non-target ODT is needed in the system then a dummy ODT command must be issued to the non-target rank for second half of the transfer of BL32.

When the DFE is enabled, the DQs shall be high for a minimum of 4UI prior to the first Write data bit to ensure proper DFE synchronization.



NOTES:
1. BL=32, 2tCK Preamble, 1.5tCK Postamble
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. A dummy WR command is required for the second half of the transfer with a delay of 8 clocks from the first WR command.
4. The figure also shows a dummy ODT command being issued to non-target rank 1 for the second half of the transfer.
5. C10 is used for burst ordering and shall be LOW for the first WR command, and be HIGH for dummy WR command.
6. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.
7. CA bits other than C10 and AP in dummy CAS command are the same as the first CAS command.
8. The DQ signal is shown as “Don’t Care” before the first Write data bit indicating DFE is disabled. When DFE is enabled, the DQ signal shall be high for a minimum of 4UI prior to the first Write data bit for proper DFE synchronization.

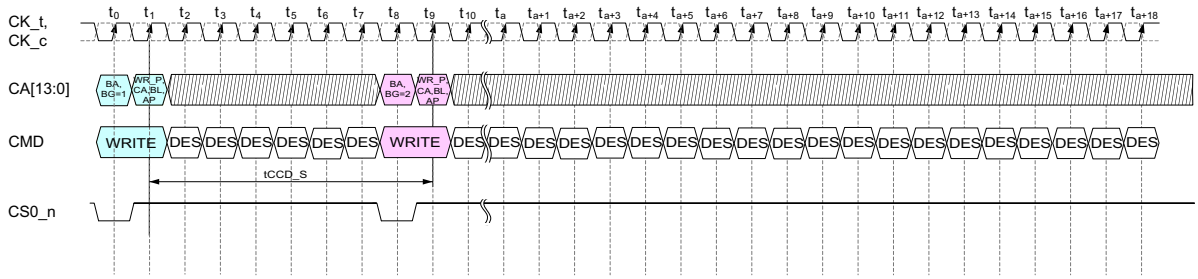
Figure 54 — Write Timing for Fixed BL32 and BL32 in BL32 OTF Mode



NOTES:
1. Figure shows BL16 write operation when MR0 is programmed to use BL32 OTF mode. In this case, no dummy WR command is required as transfer size is BL16.
2. DES commands are shown for ease of illustration; other commands may be valid at these times including commands to allow data transfer from the same die after transfer of BL16.
3. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

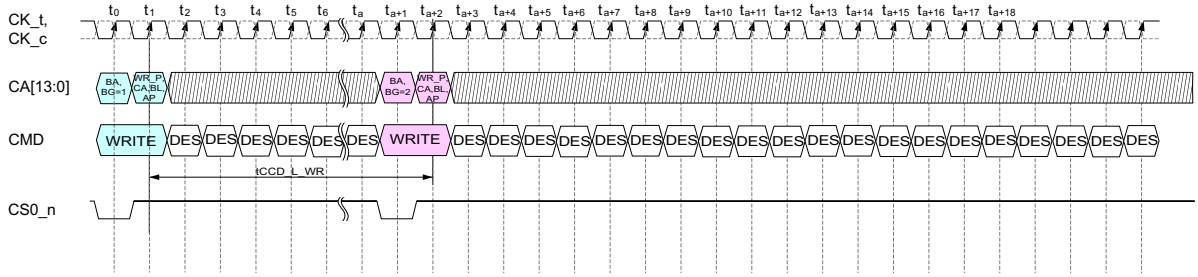
Figure 55 — Write Timings for BL16 in BL32 OTF Mode

4.8.4 Write Burst Operation for Optional BL32 Mode (cont'd)



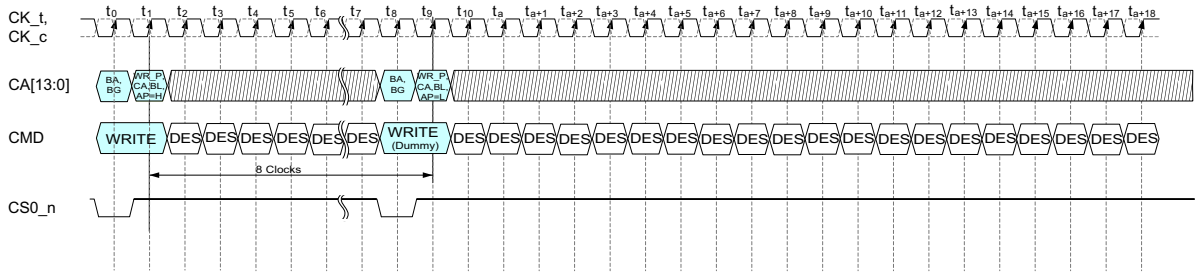
NOTES:
1. Figure shows back to back BL16 writes to different bank groups.
2. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

Figure 56 — Write to Write to Different Bank Group for BL16 in BL32 OTF



NOTES:
1. Figure shows back to back BL16 writes to same bank group using a timing of tCCD_L_WR.
2. Back to Back BL32 writes to same bank group shall have a minimum separation of 16 clocks.
3. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

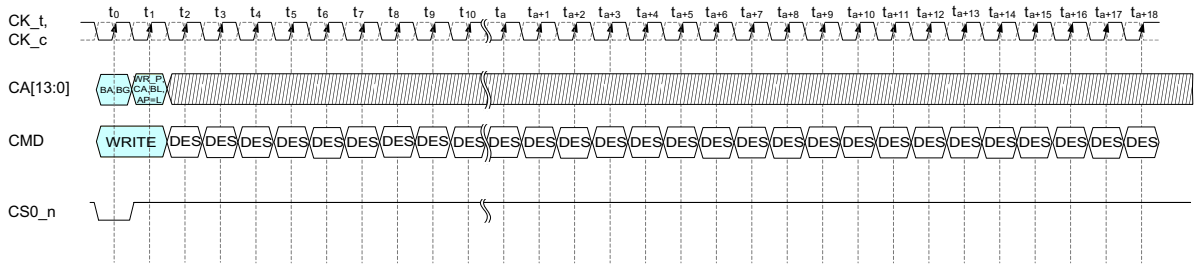
Figure 57 — Write to Write to Same Bank Group for BL16 in BL32 OTF



NOTES:
1. AP bit must be set HIGH for first CAS and LOW for dummy CAS command.
2. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.
3. CA bits other than C10 and AP in dummy CAS command are the same as the first CAS command.

Figure 58 — Write with Auto-Precharge for Fixed BL32 and BL32 in BL32 OTF Mode

4.8.4 Write Burst Operation for Optional BL32 Mode (cont'd)



NOTES:
1. AP bit must be set to LOW with the CAS command.
2. DDR5 DRAM supports an optional fixed BL32 mode and optional BL32 OTF (On the fly) mode for x4 devices only.

Figure 59 — Write with Auto-Precharge for BL16 in BL32 OTF Mode

4.8.5 Same Bank Group Write to Write Timings

DDR5 devices will have separate same bank group write timings, based on whether the second write requires an RMW (Read-Modify-Write) access or JW (Just-Write) access. In JW access, DDR5 updates all 128 bits of data on the addressed codeword, while in RMW access, a part of 128 bits is updated.

Table 51 — JW (Just-Write) Access and RMW (Read-Modify-Write) Access Definition

Configuration	BL16		BC8		Optional BL32	Notes
	Normal	Data Mask	Normal	Data Mask		
x4	RMW	—	RMW	—	JW	1, 2, 3
x8 / x16	JW	RMW			—	1, 2, 3

NOTE 1 BC8 refers to BC8 OTF mode enabled by MR0 OP[1:0]=01B, where Write command is issued with BL=L in CA5.
NOTE 2 Optional BL32 refers to BL32 OTF mode (enabled by MR0 OP[1:0]=11B), where Write command is issued with BL=L in CA5, or BL32 fixed mode (enabled by MR0 OP[1:0]=10B).
NOTE 3 Data Mask refers to Data Mask mode enabled by MR5 OP[5]=1B, where Write command is issued with WP=L in CA11.

Table 52 — Same Bank in Bank-Group Write Access to RMW Access Timings

From	To		Notes
	BL16	BC8	
BL16	tCCD_L_WR	tCCD_L_WR	1, 2, 3
BC8	tCCD_L_WR	tCCD_L_WR	1, 2, 3
Optional BL32	8nCK+tCCD_L_WR	—	1, 2, 3, 4, 5

NOTE 1 BC8 refers to BC8 OTF mode enabled by MR0 OP[1:0]=01B, where Write command is issued with BL=L in CA5.
NOTE 2 Optional BL32 refers to BL32 OTF mode (enabled by MR0 OP[1:0]=11B), where Write command is issued with BL=L in CA5, or BL32 fixed mode (enabled by MR0 OP[1:0]=10B).
NOTE 3 In Optional BL32 case, this timing table affects to the 1st Write command only, not the dummy Write command.
NOTE 4 There is no BL32 to BC8 case.
NOTE 5 When Write CRC is enabled, the timing increases by 1nCK, i.e., 9nCK+tCCD_L_WR

4.8.5 Same Bank Group Write to Write Timings (cont'd)

Table 53 — Different Bank in Bank-Group Write Access to RMW Access Timings

From	To		Notes
	BL16	BC8	
BL16	tCCD_M_WR	tCCD_M_WR	1, 2, 3
BC8	tCCD_M_WR	tCCD_M_WR	1, 2, 3
Optional BL32	8nCK+tCCD_M_WR	—	1, 2, 3, 4, 5

NOTE 1 BC8 refers to BC8 OTF mode enabled by MR0 OP[1:0]=01B, where Write command is issued with BL=L in CA5.
NOTE 2 Optional BL32 refers to BL32 OTF mode (enabled by MR0 OP[1:0]=11B), where Write command is issued with BL=L in CA5, or BL32 fixed mode (enabled by MR0 OP[1:0]=10B).
NOTE 3 In Optional BL32 case, this timing table affects to the 1st Write command only, not the dummy Write command.
NOTE 4 There is no BL32 to BC8 case.
NOTE 5 When Write CRC is enabled, the timing increases by 1nCK, i.e., 9nCK+tCCD_M_WR

Table 54 — Same or Different Bank in Bank-Group Write Access to JW Access Timings

From	To		Notes
	BL16	Optional BL32	
BL16	tCCD_L_WR2	tCCD_L_WR2	1, 2, 3
BC8	tCCD_L_WR2	—	1, 2, 3, 4
Optional BL32	—	8nCK+tCCD_L_WR2	1, 2, 3, 5

NOTE 1 BC8 refers to BC8 OTF mode enabled by MR0 OP[1:0]=01B, where Write command is issued with BL=L in CA5.
NOTE 2 Optional BL32 refers to BL32 OTF mode (enabled by MR0 OP[1:0]=11B), where Write command is issued with BL=L in CA5, or BL32 fixed mode (enabled by MR0 OP[1:0]=10B).
NOTE 3 In Optional BL32 case, this timing table affects to the 1st Write command only, not the dummy Write command.
NOTE 4 There is no BC8 to BL32 case.
NOTE 5 When Write CRC is enabled, the timing increases by 1nCK, i.e., 9nCK+tCCD_L_WR2

4.8.6 Different Bank-Group Write to Write Timings

Table 55 — Different Bank-Group Write to Write Timings

From	To			Notes
	BL16	BC8	Optional BL32	
BL16	8nCK	8nCK	8nCK	1, 2, 3
BC8	8nCK	8nCK	—	1, 2, 3, 4
Optional BL32	16nCK	—	16nCK	1, 2, 3, 4

NOTE 1 BC8 refers to BC8 OTF mode enabled by MR0 OP[1:0]=01B, where Write command is issued with BL=L in CA5.
NOTE 2 Optional BL32 refers to BL32 OTF mode (enabled by MR0 OP[1:0]=11B), where Write command is issued with BL=L in CA5, or BL32 fixed mode (enabled by MR0 OP[1:]=11B).
NOTE 3 In Optional BL32 case, this timing table affects to the 1st Write command only, not the dummy Write command.
NOTE 4 There is no BC8 to BL32 case.

4.8.7 Write Timing Violations

4.8.7.1 Motivation

Generally, if Write timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure that the DRAM works properly. However, it is desirable, for certain violations as specified below, the DRAM is guaranteed to not “hang up,” and that errors are limited to that particular operation.

For the following, it will be assumed that there are no timing violations with regards to the Write command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

4.8.7.2 Data to Strobe Eye Height or Width Violations

Should the required data to strobe timing or voltage parameters be violated (Such as: tRx_RDQ_tMargin, tRx_DQS2DQ_Skew, VRx_DQS, VRx_DQ, etc.), for any of the data/strobe timing edges or data/strobe voltage limits associated with a write burst data eye, then incorrect data might be written to the memory locations addressed with this WRITE command.

Subsequent reads from that location might results in unpredictable read data, however the DRAM will work properly otherwise.

4.8.7.3 Strobe and Strobe to Clock Timing Violations

Should the strobe timing requirements (tWPRE, tWPST) or the strobe to clock timing requirements (tDQSS, tDQSoffset) be violated for any of the strobe edges associated with a Write burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise with the following constraints:

(1) Both Write CRC and data burst OTF are disabled; timing specifications other than tWPRE, tWPST, tDQSS, tDQSoffset are not violated.

(2) The offending write strobe (and preamble) arrive no earlier or later than six DQS transition edges from the Write-Latency position.

(3) A Read command following an offending Write command from any open bank is allowed.

(4) One or more subsequent WR or a subsequent WRA {to same bank as offending WR} may be issued tCCD_L later but incorrect data could be written; subsequent WR and WRA can be either offending or non-offending Writes. Reads from these Writes may provide incorrect data.

(5) One or more subsequent WR or a subsequent WRA {to a different bank group} may be issued tCCD_S later but incorrect data could be written; subsequent WR and WRA can be either offending or non-offending Writes. Reads from these Writes may provide incorrect data.

(6) Once one or more precharge commands (PREpb, PREsb, or PREab) are issued to DDR5 after offending WRITE command and all banks become precharged state (idle state), a subsequent, non-offending WR or WRA to any open bank shall be able to write correct data.

(7) DQS strobes including preamble must align to each Write commands data burst length configuration. If the DRAM fails to capture or incorrectly de-serializes the incoming data stream because of misalignment or missing strobe edges, errors may occur. These errors will propagate indefinitely until the DRAM is put into an idle state, i.e., all banks are in the precharged state with tRP satisfied.

4.8.8 Write Enable Timings

4.8.8.1 Introduction

The following specifies the relationship between the write enable timing window tWPRE_EN_ntck and the DRAM related DQS to CK drift window tDQSD as well as the system related DQS to CK drift window tDQSS around the final DQS to CK offset trained pass/fail point tDQSoffset based on write leveling feedback in order to support n-tck pre-amble mode. Functional operation requires that the following condition is met:

- tWPRE_EN_ntck >= |tDQSSmin|+tDQSSmax+|tDQSDmin|+tDQSDmax

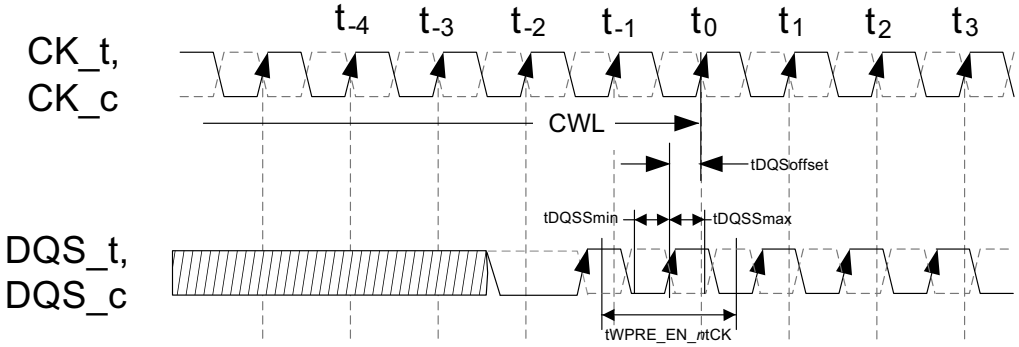


Figure 60 — tDQSS: DRAM External CLK-to-DQS Variation

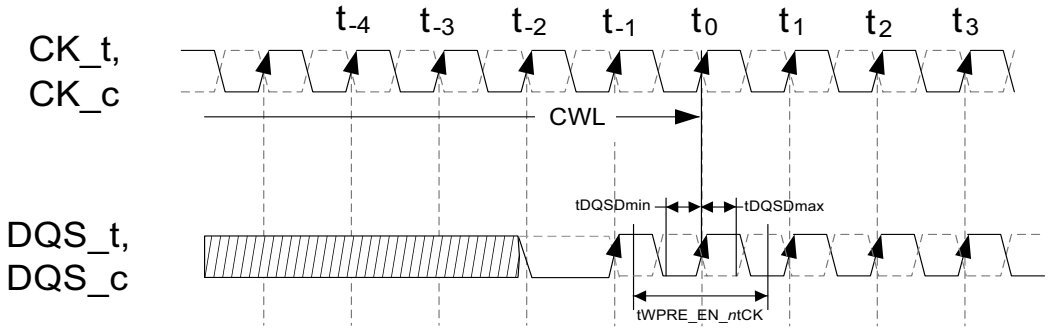


Figure 61 — tDQSD: DRAM Internal CLK-to-DQS Variation

4.8.8.1 Introduction (cont'd)

Table 56 — Write Enable Timing Parameters DDR5 3200 to 9200

Parameter	Symbol	Speed Bins DDR5 3200-9200		Unit	Notes
		Min	Max		
2-tck Write pre-amble enable window	tWPRE_EN_2tck	1.5	-	tCK	
3-tck Write pre-amble enable window	tWPRE_EN_3tck	2.5	-	tCK	
4-tck Write pre-amble enable window	tWPRE_EN_4tck	2.5	-	tCK	
Final trained value of host DQS_t-DQS_c timing relative to CWL CK_t-CK_c edge	tDQSoffset	-0.5	0.5	tCK	2
DRAM voltage/temperature drift window of first rising DQS_t pre-amble edge relative to CWL CK_t-CK_c edge	tDQSD	-0.25* tWPRE_EN_*n*tCK (min)	0.25* tWPRE_EN_*n*tCK (min)	tCK	1
Host and system voltage/temperature drift window of first rising DQS_t pre-amble edge relative to CWL CK_t-CK_c edge	tDQSS	-0.25* tWPRE_EN_*n*tCK (min)	0.25* tWPRE_EN_*n*tCK (min)	tCK	1, 3

NOTE 1 Measured relative to the write leveling feedback, after write leveling training has been completed.

NOTE 2 When measuring the tDQSoffset, tWLS/H are reflected in the tDQSoffset result.

NOTE 3 DDR5-3200 timings apply for data rates <2933 MT/s. For example, at 2000 MT/s, tDQSS(max) = (2000/2933)*0.25*tWPRE_EN_*n*tck(min) = 0.17*tWPRE_EN_*n*tck(min).

Symbol	Description	Min	Max	Unit
tWLS/H	Write Leveling Setup/Hold Time	-80	+80	ps

4.9 Self Refresh Operation

The Self-Refresh command can be used to retain data in the DDR5 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR5 SDRAM retains data without external clocking. The DDR5 SDRAM device has a built-in timer to accommodate Self-Refresh operation. While in Self Refresh, the DDR5 SDRAM adjusts and updates its internal average periodic refresh interval, as needed, based on its own temperature sensor. The internal average periodic refresh interval adjustment (increasing, decreasing or staying constant) does not require any external control.

Self Refresh entry is command based (SRE), while the Self-Refresh Exit Command is defined by the transition of CS_n LOW to HIGH with a defined pulse width tCSH_SRexit, followed by three or more NOP commands (tCSL_SRexit) to ensure DRAM stability in recognizing the exit. This is described below in more detail.

Before issuing the Self-Refresh-Entry command, the DDR5 SDRAM must be idle with all bank precharge state with tRP satisfied. 'Idle state' is defined as all banks are closed (tRP, etc. satisfied), no data bursts are in progress, and all timings from previous operations are satisfied (tMRD, tRFC, etc.). A Deselect command must be registered on the last positive clock edge before issuing Self Refresh Entry command. Once the Self Refresh Entry command is registered, Deselect commands must also be registered at the next positive clock edges until tCPDED is satisfied. After tCPDED has been satisfied, CS_n must transition low. After CS_n transitions low at the end of tCPDED, the CS_n shall stay low until exit. The DDR5 SDRAM may switch to a CMOS based receiver to save more power and that transition should coincide with CS_n going low.

When the CS_n is held low, the DRAM automatically disables ODT termination and sets Hi-Z as termination state regardless RTT configuration for the duration of Self-Refresh mode. Upon exiting Self-Refresh, DRAM automatically enables ODT termination and set RTT_PARK (for DQs) asynchronously during tXSDLL when RTT_PARK is enabled. CA/CS/CK ODT shall revert to its strapped or its MR ODT Setting state if previously applied. During normal operation (DLL on) the DLL is automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self-Refresh.

When the DDR5 SDRAM has entered Self-Refresh mode, all of the external control signals, except CS_n and RESET_n, are "don't care." For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSS, and VPP) must be at valid levels. DRAM internal VrefDQ and/or VrefCA generator circuitry may remain ON or turned OFF depending on DRAM design. If DRAM internal VrefDQ and/or VrefCA circuitry is turned OFF in self refresh, when DRAM exits from self refresh state, it ensures that VrefDQ and/or VrefCA and generator circuitry is powered up and stable within tXS period. First Write operation or first Write Leveling Activity may not occur earlier than tXS after exit from Self Refresh. The DRAM initiates a minimum of one Refresh command internally once it enters Self-Refresh mode.

The clocks must stay on until tCKLCS but can be DON'T CARE after tCKLCS expires but it should be noted that shortly after tCPDED, the termination for the clocks will be off. The clock is internally disabled (in the DRAM) during Self-Refresh Operation to save power. The minimum time that the DDR5 SDRAM must remain in Self-Refresh mode is tCSL. The user may change the external clock frequency or halt the external clock tCKLCS after Self-Refresh entry is registered, however, the clock must be restarted and stable tCKSRX before the device can exit Self-Refresh operation.

The procedure for exiting Self-Refresh requires a sequence of events. Since the DRAM will switch to a CMOS based driver to save power, the DRAM will trigger Self-Refresh exit upon seeing the CS_n transition from low to high and stay high for tCSH_SRExit. tCASRX prior to CS_n transitioning high, the CA bus must be driven high. Once tCSH_SRExit is satisfied, three NOP commands must be issued, otherwise the DRAM could be put into an unknown state. The clocks must be valid for tCKSRX prior to issuing the NOP commands that completes the Self Refresh exit sequence. Once a Self-Refresh Exit is registered, the following timing delay must be satisfied:

1. Commands that do not require locked DLL:
   tXS - ACT, MPC, MRW, PDE, PDX, PRE(ab,sb,pb), REF(ab,sb), RFM(ab,sb), SRE, VREFCA

2. Commands that require locked DLL:
   tXS_DLL - RD, MRR, WR, WRP

There are some Host system requirements and restrictions to use the optional SRX/NOP Clock-Sync feature. The Clock-Sync feature is intended to address issue in a system where Host Clock has Duty Cycle Distortion that is different from cycle to cycle in even/odd clock in repeating manner where Clock mis-alignment between Host Clock and DRAM internal 4-phase clock can results in worse performance than initially trained. If Host Clock can guarantee the consistent duty cycle on every even/odd clock as far as meeting CK input spec, the Clock-Sync feature is not needed. If Host CLK has the consistent duty cycle on every even/odd clocks but changes direction (i.e., from 46% to 54%) after SRX, the Clock-Sync feature won't be able to address such issue.

4.9 Self Refresh Operation (cont'd)

This Clock-Sync feature can be used only with Host system tracking clock from the first SRX Clock-Sync prior to DCA training and guarantee to issue subsequent SRX with exact same phase. Host system applications that cannot guarantee the consistent system clock phase between the first SRX Clock-Sync prior to DCA training and subsequent SRX at the first NOP (for example, like a system where system clock is stopped to put host system in low power mode or to do frequency change and put DRAM into self-refresh) cannot use the Clock Sync feature and therefore should not enable this feature.

The SRX/NOP Clock-Sync scheme helps the DRAMs that have 4-phase internal clock to determine whether ICLK or IBCLK will be the first one that is synchronized with Host Clock after Self-Refresh Exit (SRX). It also helps host to identify the right DCA MR setting that was pre-trained during the initialization process to the clock edge. DRAMs are responsible to align the first NOP after SRX (tc+1 in Figure 58 and Figure 59) to the internal clock edge that existed during the DCA training. For instance on the DRAM that aligns the first NOP with internal Odd clock, while in SREF, the DRAM detects whether the first NOP arrives via the Even or the Odd command-decode pipeline. Then if the first NOP arrives via the Odd pipeline, the DRAM does do nothing. If the first NOP arrives via the Even Pipeline, the DRAM does initiate the Clock-Sync scheme to sync the first NOP after SRX to the internal Odd clock. For all subsequent SRE/SRX sequences, the DRAM will sync its internal clocks with what existed during the DCA training. In order for DRAM to do this, host is required to send SRX first NOP on the exact same clock phase that was used during the DCA training. In this way, the SRX/NOP Clock-Sync feature enforces repeatability of clock phases to an Odd phase upon SRX. It also helps on minimizing repeatability of the additive/subtractive effect of the DCA training on Tx jitter. If host sends SRX first NOP on different clock phase than the phase used during DCA training while the Clock-Sync feature is enabled, DCA adjustment may be in the wrong direction and could result in worse performance than without DCA adjustment. The SRX/NOP Clock-Sync scheme is an optional feature on DDR5. MR13:OP[5] indicates host whether the SRX/NOP Clock-Sync feature is supported or not.

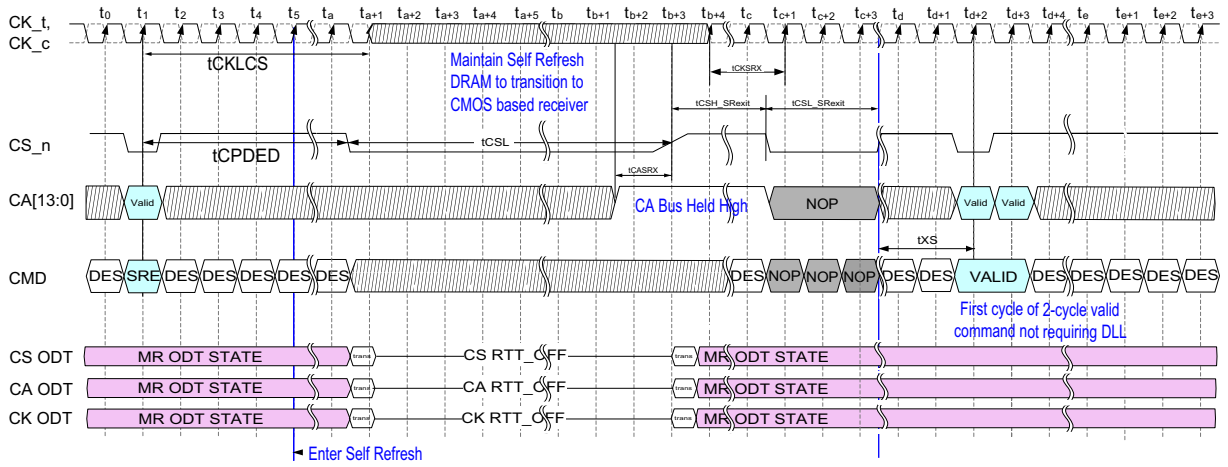
When SRX/NOP Clock-Sync feature is enabled by MRW to MR13:OP[5]=1, to make the Clock-Sync Scheme fully functional, (1) Host (including RCD, Clock Driver) is responsible to ensure the phases of the system clock before and after SRX. (2) Host shall issue an initial SRE/SRX pair after CSTM/CATM prior to DCA training to ensure that the Clock-Sync is in effect during DCA training, (3) the continuous system clock during Self-Refresh is not required to make the Clock-Sync feature fully functional, but every first NOP registered after each tCSH_SRexit shall be the same phase of system clock (for example, Odd) that existed at the first NOP at tc+1 cycle in the initial SRX sequence prior to DCA training so that DRAM can get the consistent phases of system clock when DRAM does do the clock sync, and (4) for DCA training at multiple frequencies, the first NOP after SRX for a given clock frequency shall be the same phase of system clock (for example, Odd) that existed at exit Self Refresh w/Frequency Change mode prior to DCA training for that frequency.

Depending on the system environment and the amount of time spent in Self-Refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in "ZQ Calibration Commands". To issue ZQ calibration commands, applicable timing requirements must be satisfied.

Upon exiting Self Refresh, tREFI begins when CS_n rises with tCSH_SRexit (tb+3 in Figure 62). One additional refresh shall be issued in addition to refreshes normally scheduled. This additional refresh is not counted toward the computation of the average refresh interval (tREFI). If this refresh isn't issued by tREFI after CS_n rises with tCSH_SRexit, then it counts toward the maximum number of refreshes which may be postponed. This additional refresh does not replace the regularly periodic refresh that's also scheduled at tREFI after CS_n rises with tCSH_SRexit (both of these refresh commands count toward the maximum number of refreshes which may be postponed). The additional refresh consists of a single REFab command or n * REFsb, where n is the number of banks in a bank group. If Self Refresh is to be re-entered and no regularly scheduled periodic refresh commands have been issued, the additional refresh shall be issued prior to Self Refresh re-entry. Plus, FGR mode may require extra Refresh command(s), in addition the aforementioned additional Refresh, depending on the condition of the Self Refresh entry (refer to Clause 4.13.7 for more information)

The exit timing from self-refresh exit to first valid command not requiring a locked DLL is tXS. The value of tXS is (tRFC). This delay is to allow for any refreshes started by the DRAM to complete. tRFC continues to grow with higher density devices so tXS will grow as well.

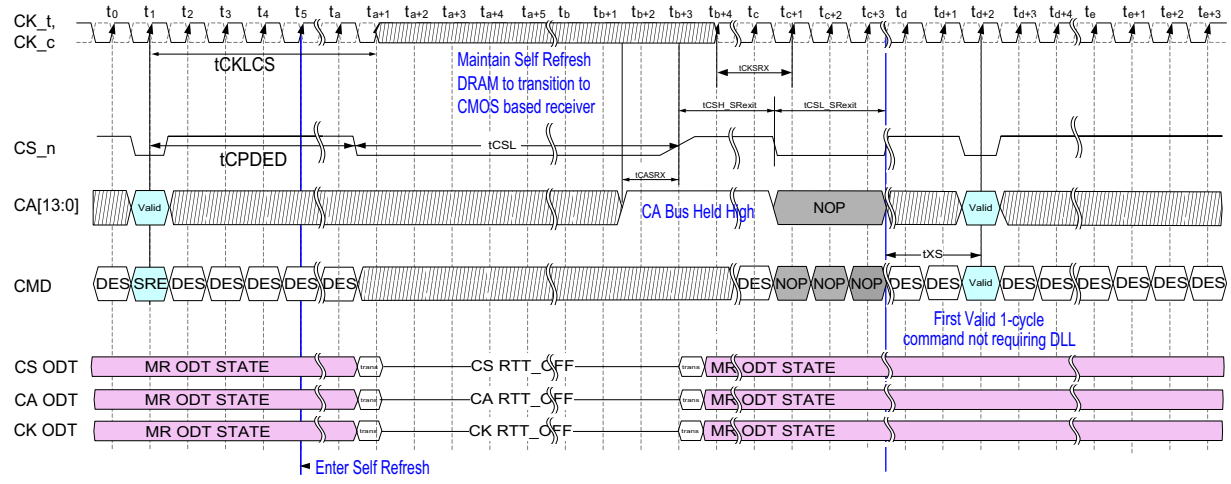
4.9 Self Refresh Operation (cont'd)



NOTES:

1. While in 2N mode, tCSL_SRexit will not be statically held low (as shown above), as it will pulse for each 2 cycle period. Refer to the 2N mode section for more details.
2 Both tCSH_SRexit and tCSL_SRexit timings must be satisfied to guarantee DRAM operation.
3. When tCSH_SRexit,min expires, the CA bus is allowed to transition from all bits High to any valid (V) level. Prior to CS_n being registered Low at tc+1, the CA bus must transition to NOP conforming to the CAI state of the DRAM and complying with applicable DRAM input timing parameters.

Figure 62 — Self-Refresh Entry/Exit Timing with 2-Cycle Exit Command



NOTES:

1. While in 2N mode, tCSL_SRexit will not be statically held low (as shown above), as it will pulse for each 2 cycle period. Refer to the 2N mode section for more details.
2. Both tCSH_SRexit and tCSL_SRexit timings must be satisfied to guarantee DRAM operation.
3. When tCSH_SRexit,min expires, the CA bus is allowed to transition from all bits High to any valid (V) level. Prior to CS_n being registered Low at tc+1, the CA bus must transition to NOP conforming to the CAI state of the DRAM and complying with applicable DRAM input timing parameters.

Figure 63 — Self-Refresh Entry/Exit Timing with 1-Cycle Exit Command

4.9 Self Refresh Operation (cont'd)

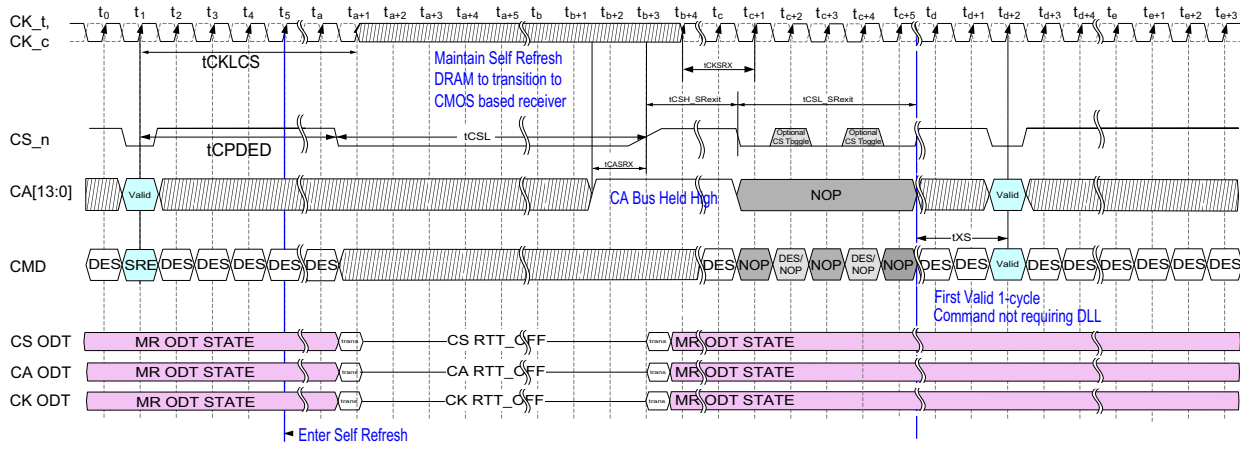
Table 57 — Self-Refresh Timing Parameters

Parameter	Symbol	Min	Max	Unit	Note
Command pass disable delay	tCPDED	max(5ns, 8nCK)	-	nCK, ns	
Self-Refresh CS_n low Pulse width	tCSL	10	-	ns	
Self-Refresh exit CS_n High Pulse width	tCSH_SRexit	13	200	ns	
Self-Refresh exit CS_n Low Pulse width	tCSL_SRexit	3nCK	30ns	nCK, ns	1
Valid Clock Requirement before SRX	tCKSRX	max(3.5ns, 8tCK)	-	nCK, ns	
Valid Clock Requirement after SRE	tCKLCS	tCPDED + 1nCK	-	nCK, ns	
Self-Refresh exit CS_n high	tCASRX	0		ns	
Exit Self-Refresh to next valid command NOT requiring a DLL	tXS	tRFC1	-	ns	
3DS exit Self-Refresh to next valid command NOT requiring a DLL	tXS_3DS	tRFC1_slr+10ns	-	ns	2, 3, 4
Exit Self-Refresh to next valid command requiring a DLL	tXS_DLL	tDLLK		ns	

NOTE 1 While in 2N mode, tCSL_SRexit will not be statically held low, as it will pulse for each 2-cycle period for a min of 6nCK. Refer to the 2N mode section for more details.
NOTE 2 Upon exit from Self-Refresh, the 3D Stacked DDR5 SDRAM requires a minimum of one extra refresh command to all logical ranksbefore it is put back into Self-Refresh Mode.
NOTE 3 This parameter utilizes a value that varies based on density. Refer to the 3DS Refresh section for more information.
NOTE 4 These timings are for x4 2H and 4H 3Ds devices.

4.9.1 Self Refresh in 2N Mode

The timing diagram in Figure 64 shows details for Self Refresh entry/exit in 2N Mode. Only SRX, with a pulsing CS_n (NOP-DES-NOP-DES-NOP) during tCSL_SRexit, to a 1-cycle command is shown, but behavior is similar for SRX to a 2-cycle command. Behavior is similar for Frequency Change during Self Refresh, with or without VREF and/or ODT changes. Pulsing CS_n during tCSL_SRexit is not required for Self Refresh exit (for example, CS_n may be held low for the full tCSL_SRexit duration).



NOTES:

1. Both tCSH_SRexit and tCSL_SRexit timings must be satisfied to guarantee DRAM operation.
2. When tCSH_SRexit,min expires, the CA bus is allowed to transition from all bits High to any valid (V) level. Prior to CS_n being registered Low at tc+1, the CA bus must transition to NOP conforming to the CAI state of the DRAM and complying with applicable DRAM input timing parameters.

Figure 64 — Self-Refresh Entry/Exit Timing in 2N Mode with 1-Cycle Exit Command

4.9.2 Partial Array Self Refresh (PASR)

PASR has been deprecated starting with spec working revision 1.90, JESD79-5C-v1.30. All MR60 bits will behave as RFU on devices that do not support PASR.

DDR5 DRAMs may contain an optional feature that disables refresh to selected segments in each bank when in self refresh. The feature allows for lower self refresh power if portions of the DRAMs are not required to retain data. Each bank is divided into six or eight segments based on the three highest row address bits supported by the DRAM device's density. Non-Binary density devices are divided into 6 segments as the 110 and 111 encodings of the PASR segment row bits are not used.
Binary densities are divided into 8 segments.

MR60 provides the segment mask for all banks, with one bit per segment. A 0 (default) in the bit position provides normal refresh operation for the segment while a 1 masks that segment. Masked segments are NOT refreshed during self refresh. Note that this affects Self Refresh only. All segments are refreshed by refresh command when out of self refresh.

Segments which are masked are not guaranteed to retain their data if self refresh is entered. ECS Transparency will not produce accurate results if any mask bit is set, but ECS scrubbing will still occur if enabled.

MR19 bit 7 is indicates whether the DRAM supports PASR. 0 = Not Supported, 1 = Supported

Table 58 — MR60 Definition

Segment (PASR Row Bits)	Type	Operand	Data	Notes
Segment 0 (000)	W	OP0	0=Normal, 1=Masked	
Segment 1 (001)	W	OP1	0=Normal, 1=Masked	
Segment 2 (010)	W	OP2	0=Normal, 1=Masked	
Segment 3 (011)	W	OP3	0=Normal, 1=Masked	
Segment 4 (100)	W	OP4	0=Normal, 1=Masked	
Segment 5 (101)	W	OP5	0=Normal, 1=Masked	
Segment 6 (110)	W	OP6	0=Normal, 1=Masked	Must be 0 for 24 Gbit and 48 Gbit devices.
Segment 7 (111)	W	OP7	0=Normal, 1=Masked	Must be 0 for 24 Gbit and 48 Gbit devices.

Table 59 — PASR Segment Row Address Bits

DRAM Density	PASR Row Bits	Segments
8 Gbit	R15:13	8
16 Gbit	R15:13	8
24 Gbit	R16:14	6
32 Gbit	R16:14	8
48 Gbit	R17:15	6
64 Gbit	R17:15	8

4.10 Power-Down Mode

DDR5's Power-Down (PD) mode is new to the DDR family, as it no longer has a CKE pin to control entry and exit. Instead, the Power-Down Entry (PDE)/Power-Down Exit (PDX) move to command based, triggered by the CS_n. Once in PD mode, the CS_n acts effectively like the historic CKE pin, waiting for it to transition from HIGH to LOW (with its command). In PD mode, CS_n should be sampled on every edge.

4.10.1 Power-Down Entry and Exit

Power-Down is entered when the PDE command is registered. Unlike Self Refresh Mode, CS_n will NOT be held low constantly while in Power-Down. Timing diagrams are shown in Figure 65 with details for entry and exit of Power-Down.

The DLL should be in a locked state when Power-Down is entered for fastest Power-Down exit timing. SDRAM design provides all AC and DC timing and voltage specifications, as well as proper DLL operation as long as DRAM controller complies with SDRAM standards.

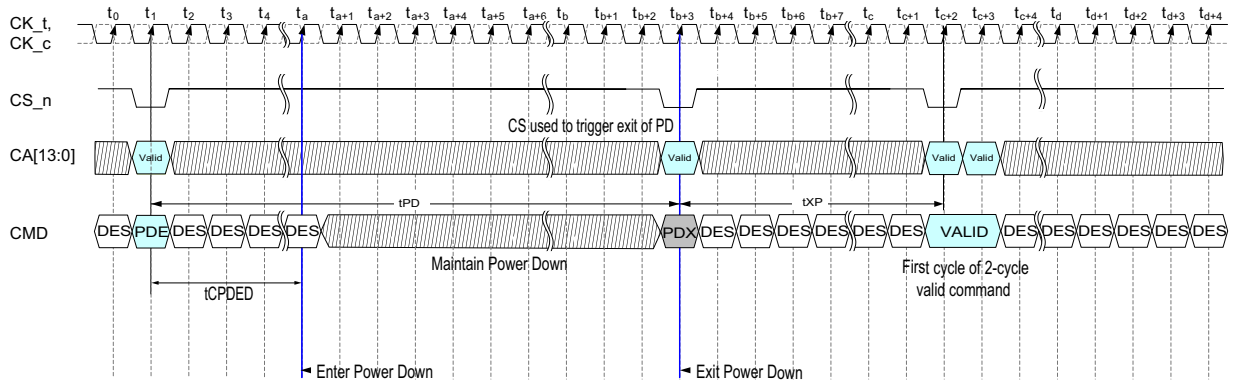
During Power-Down, if all banks are closed after any in-progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in-progress commands are completed, the device will be in active Power-Down mode.

Entering Power-Down deactivates the input and output buffers, excluding CK_t, CK_c, CS_n, RESET_n which remain enabled throughout the duration of Power-Down. If CA11=L during the PDE command, command input buffers CA1 and CA4 remain enabled, allowing the appropriate Non-Target (NT) On-Die Termination (ODT) command to be passed through and decoded by the non-target DRAM in Power-Down (i.e. the DRAM will monitor commands that utilize NT ODT and will not exit Power-Down as a result of a valid NT ODT command being registered). Optionally, command input buffers CA0, CA2, CA3 and CA5 may remain enabled if needed by the DRAM to properly decode the NT ODT commands during PDE and PDX.

If CA11=H during the PDE command, only the PDX command, qualified by CS_n, is legal during Power-Down. If CA11=L during the PDE command, only NT ODT commands and PDX commands, qualified by CS_n, are legal during Power-Down. Refer to the command truth table for more information.

Although MRR is BL16 regardless of the MR0 Burst Length setting, the host shall not issue MRR NT ODT commands during Power-Down when MR0:OP[1:0]=01.

When Power-Down is entered with NT ODT control enabled (CA11=L), the DRAM will continue to accept NT commands throughout the Power-Down process, including entry and exit. Upon Power-Down entry during the tCPDED period, the DRAM will be switching from decoding all CA bus command bits to only decoding CA1 and CA4. During this time all CA command bits must be valid when CS_n is asserted with the full Read or Write command, as the DRAM may still be decoding the full command. Following tCPDED, only CA1 and CA4 need be valid as the DRAM will be ignoring the others. Following the PDX command, all CA command bits must be valid for NT termination commands also, as the DRAM will be transitioning to decoding all bits. In the optional case where command input buffers CA0, CA2, CA3 and CA5 remain enabled, all CA command bits must be valid when CS_n is asserted between the PDE command and the completion of tXP upon PDX. It is only the time between tCPDED completion and tXP start that non-CA command bits (CA13:6) and CA command bits not being used for the NT ODT command decode need not be valid.



NOTES:
1. There is no specific PDX command. In the case of systems with register using CAI, the encoding out of the register may be inverted from a NOP type command.
2. Diagram above is shown with a valid 2-cycle command after tXP for simplicity. 1-cycle valid commands are also legal.
3. CS_n shall be held HIGH, not toggled, during Power-Down, except Non-Target ODT command when PDE with CA11=L is asserted.

Figure 65 — Power-Down Entry and Exit Mode

4.10.1 Power-Down Entry and Exit (cont'd)

Table 60 — Power-Down Entry Definitions

Status of DRAM	DLL	PD Exit	Relevant Parameters
Active (One or more banks open)	On	Fast	tXP
Precharge (All banks precharged)	On	Fast	tXP

The DLL is kept enabled during Precharge Power-Down or Active Power-Down. (If RESET_n goes low during Power-Down, the DRAM will be out of PD mode and into reset state). Power-down duration is limited by tPD(max) of the device.

Table 61 — Power Down Timing Parameters

Parameter	Symbol	Min	Max	Unit	Note
Command pass disable delay	tCPDED	max(5ns, 8nCK)	-	ns, nCK	
Power-Down duration	tPD	max(7.5ns, 8nCK)	5 * tREFI1 (Normal) 9 * tREFI2 (FGR)	ns, nCK	8
Power-Down Exit command to next valid command (excluding NT ODT commands when PDE with CA11=L)	tXP	max(7.5ns, 8nCK)		ns, nCK	
Activate command to Power Down Entry command	tACTPDEN	2		nCK	1
Precharge, Precharge All, or Precharge Same Bank command to Power-Down Entry command	tPRPDEN	2		nCK	1
Read or Read w/Auto Precharge command to Power-Down Entry command	tRDPDEN	CL+RBL/2+1		nCK	4, 6
Write command to Power-Down Entry command	tWRPDEN	CWL+WBL/2+WR+1		nCK	2, 4, 7
Write w/Auto Precharge command to Power-Down Entry command	tWRAPDEN	CWL+WBL/2+WR+1		nCK	2, 3, 4, 7
Refresh All or Refresh Same Bank command to Power-Down Entry command	tREFPDEN	2		nCK	
MRR command to Power-Down Entry command	tMRRPDEN	CL+8+1		nCK	4
MRW command to Power-Down Entry command	tMRWPDEN	tMRD(min)		nCK	
MPC command to Power-Down Entry command	tMPCPDEN	tMPC_delay		nCK	5

NOTE 1 Power-Down command can be sent while operations such as Activation, Precharge, Auto-Precharge or Refresh are in progress but IDD spec will not be applied until the operations are finished.

NOTE 2 Write Recovery (WR) is calculated from tWR by using the Rounding Algorithm. Refer to the Rounding Definitions and Algorithm section for more information.

NOTE 3 Write Recovery (WR) in clock cycles as programmed in MR6.

NOTE 4 Read/Write/MRR can refer to both Target command and Non-Target command when CA11=H during PDE command.

NOTE 5 tMPC_delay is a valid timing parameter for all MPC functions except:

a) Enter CS training Mode, Enter CA Training Mode, PDA Enumerate ID Program Mode because Power Down Entry is not supported for these MPC commands.

b) Apply VrefCA, VrefCS and RTT_CA/CS/CK because this MPC command requires waiting for VrefCA_time/VREFCS_time.

NOTE 6 RBL: Read burst length associated with Read command

a) RBL = 32 (36 with RCRC on) for fixed BL32 and BL32 in BL32 OTF mode

b) RBL = 16 (18 with RCRC on) for fixed BL16 and BL16 in BL32 OTF mode

c) RBL = 16 (18 with RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

NOTE 7 WBL: Write burst length associated with Write command

a) WBL = 32 (36 with WCRC on) for fixed BL32 and BL32 in BL32 OTF mode

b) WBL = 16 (18 with WCRC on) for fixed BL16 and BL16 in BL32 OTF mode

c) WBL = 16 (18 with WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

NOTE 8 tPD(max) shall always be less than or equal to 5*tREFI1(max) during Normal Refresh Mode and less than or equal to

NOTE 9 tREFI2(max) during Fine Granularity Refresh Mode, and when using the rounding algorithms, nPD(max) shall always be less than or equal to 5*nREFI1(max) during Normal Refresh Mode and less than or equal to 9*nREFI2(max) during Fine Granularity Refresh Mode.

4.10.1 Power-Down Entry and Exit (cont'd)

Table 62 — Valid Command During Power-Down with ODT Enabled

CA1	CA4	Command	Operation of DRAM in Power Down
L	L	Write	DRAM will enable ODT_WR_NOM
L	H	Read	DRAM will enable ODT_RD_NOM
H	L	Illegal	Illegal. CS_n will NOT be asserted to a powered down DRAM with this combination
H	H	PDX(NOP)	Exit Power Down
NOTE 1 MRR NT ODT commands during Power-Down are not allowed when MR0:OP[1:0]=01.			

4.11 Input Clock Frequency Change

Once the DDR5 SDRAM is initialized, the DDR5 SDRAM requires the clock to be "stable" during almost all states of normal operation. This means that, once the clock frequency has been set and is to be in the "stable state", the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under Self Refresh with Frequency Change mode. Outside Self-Refresh w/Frequency Change mode, it is illegal to change the clock frequency.

Prior to entering Self-Refresh with Frequency Change mode, the host must program tCCD_L/tCCD_L_WR/tCCD_L_WR2/tDLLK via MPC Command to update MR13 shadow register to the desired target frequency and configure VREFCA, VREFCS, RTT_CK, RTT_CS and RTT_CA (MR11, MR12, MR32, and MR33) shadow registers if needed.

Once the DDR5 SDRAM has been successfully placed into Self-Refresh w/Frequency Change mode and tCKLCS has been satisfied, the state of the clock becomes a don't care. Once a don't care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. During tCSL_FreqChg and prior to exiting Self-Refresh, the DRAM will automatically apply the changes to tCCD_L/tCCD_L_WR/tCCD_L_WR2/tDLLK, VREFCA, VREFCSRTT_CK, RTT_CS, and RTT_CA. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in Section 4.9 "Self-Refresh Operation". For the new clock frequency, Mode Registers may need to be configured (to program the appropriate CL, Preambles, Write Leveling Internal Cycle Alignment, DFE, DCA, etc.) prior to normal operation.

The DDR5 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade.

4.11.1 Frequency Change Steps

The following steps must be taken:

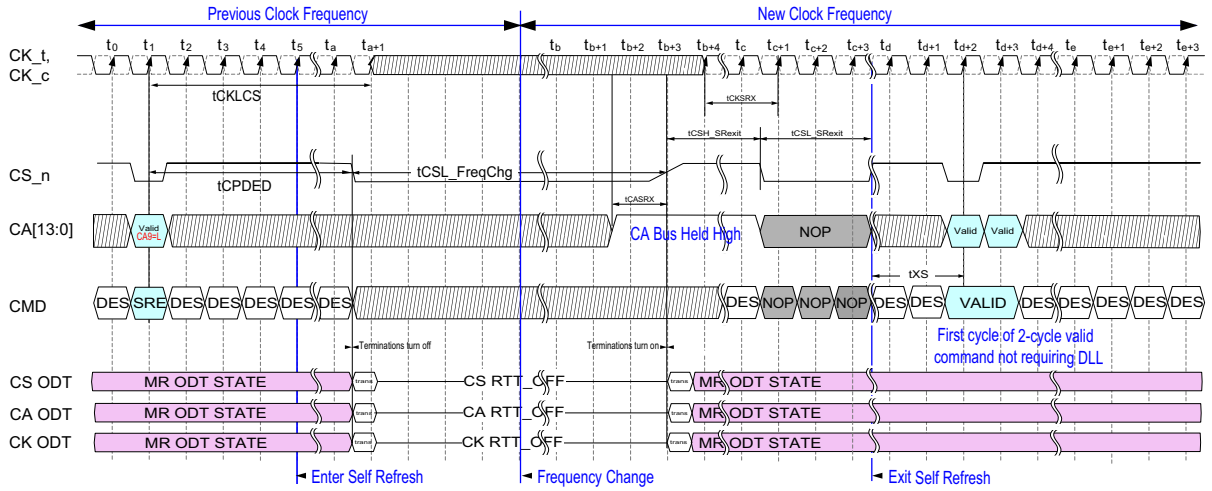
1. Prior to executing the SREF command, the shadow register of Mode Registers MR11/MR12/MR13/MR32/MR33 can be pre-loaded anytime if DRAM is in an IDLE state:
    - 1a. The host MUST program tCCD_L/tCCD_L_WR/tCCD_L_WR2/tDLLK via MR13:OP[3:0] to the desired target frequency. During this stage, the values are stored in the MR13 shadow register and shall be applied to MR13 automatically when running SREF w/ CA9="L" on the DRAM. This change occurs during tCSL_FreqChg when exiting Self-Refresh with Frequency Change.
    - 1b. The host can configure the appropriate CS/CA/CK ODT settings via Mode Register (MR32 and MR33) if new values are needed for the new target frequency. During this stage, the values are stored in the MR32 and MR33 shadow registers and shall be applied to MR32 and MR33 automatically when running SREF with CA9="L" on the DRAM. This change occurs during tCSL_FreqChg when exiting Self-Refresh w/Frequency Change.
    - 1c. The host can configure the VREFCA and VREF CS via the VREFCA or VREFCS command(s). During this stage, the values are stored in the MR11 and MR12 shadow registers and shall be applied to MR11 and MR12 automatically when running SREF with CA9="L" on the DRAM. This change occurs during tCSL_FreqChg when exiting Self-Refresh with Frequency Change.
    - 1d. Entering and exiting Self-Refresh with the SREF command shall replace the values of MR11, MR12, MR13, MR32, and MR33 with their shadow register values.
2. Enter Self Refresh with Frequency Change by sending the SREF command (SRE with CA9='L').

4.11.1 Frequency Change Steps (cont'd)

3. After tCPDED(min), the host will transition CS_n low, indicating to the DRAM that the terminations are safe to turn off.
4. After tCKLCS, the host can turn the clocks off.
5. Device enters Self Refresh.
6. At this time, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX
7. Exiting Self-Refresh w/Frequency Change follows the same process as normal Self-Refresh exit.
8. After tXS, any additional mode registers requiring the DLL that are needed for the new frequency can be configured or other commands not requiring a DLL may be issued. (ACT, MPC, MRW, PDE, PDX, PREab, PREsb, PREpb, REFab, REFsb, RFMab, RFMsb, SRE, VREFCA, VREFCS)
9. After tXS_DLL, normal operations resume and all commands are legal.

Table 63 — Self Refresh with Frequency Change (for Reference)

Function	Abbreviation	CS	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Self Refresh Entry with Frequency Change	SREF	L	H	H	H	L	H	V	V	V	V	L	L	V	V	V	1
NOTE 1 See Command Truth Table for details																	



NOTES:
1. While in 2N mode, tCSL_SRexit will not be statically held low (as shown above), as it will pulse for each 2 cycle period. Refer to the 2N mode section for more details.
2. Both tCSH_SRexit and tCSL_SRexit timings must be satisfied to guarantee DRAM operation.
3. Diagram above is shown with a valid 2-cycle command after tXS for simplicity. 1-cycle valid commands are also legal.
4. When tCSH_SRexit,min expires, the CA bus is allowed to transition from all bits High to any valid (V) level. Prior to CS_n being registered Low at tc+1, the CA bus must transition to NOP conforming to the CAI state of the DRAM and complying with applicable DRAM input timing parameters.

Figure 66 — Frequency Change during Self Refresh

Table 64 — Self-Refresh Frequency Change Timing Parameters

Parameter	Symbol	Min	Max	Unit	Note
Self-Refresh CS_n low Pulse width with Freq Change	tCSL_ FreqChg	VrefCA_time	-	ns	1
NOTE 1 Since frequency can require VREFCA, VREFCS and CA/CK/CS ODT Changes, the min time is longer than the traditional tCSL when the SRE command with CA9=L is used.					

4.12 Maximum Power Saving Mode (MPSM)

When Maximum Power Saving Mode is enabled by setting the MPSM enable (MR2:OP[3]) bit to '1' using MRW command, the device enters Maximum Power Saving Mode Idle (MPSM Idle) state. When Maximum Power Saving Mode for Device 15 is enabled by setting the Device 15 MPSM enable bit (MR2:OP[5]) to '1' using MRW command, and the device's PDA Enumerate ID (MR1 bits OP[3:0]) are equal to 15, the device enters Maximum Power Saving Mode Idle (MPSM Idle) state. Setting the Device 15 MSPM enable bit to '1' must be done after PDA device enumeration is complete. Once the DRAM is placed into the MPSM Idle state, it can stay in that state indefinitely, or it can further enter either Maximum Power Saving Mode Power Down (MPSM Power Down) state or Maximum Power Saving Mode Self Refresh (MPSM Self Refresh) state.

Data retention is not guaranteed when DRAM is in any of MPSM states. Mode register status and Soft PPR information is preserved.

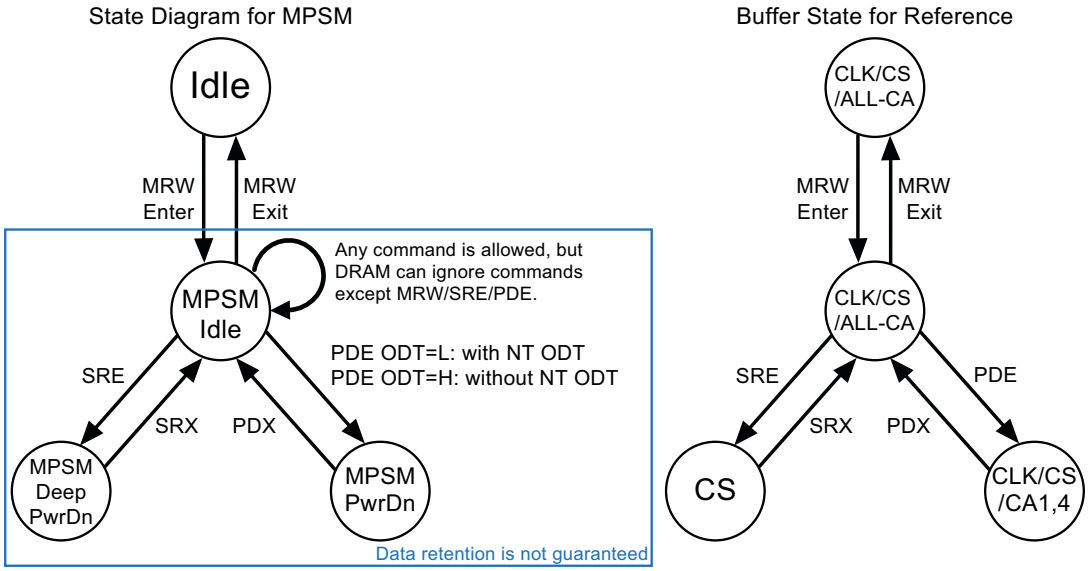


Figure 67 — State Diagram for Maximum Power Saving Mode

Table 65 — MPSM Configuration Options

MPSM MR2:OP[3]	Device 15 MPSM MR2:OP[5]	PDA Enumeration ID MR1:OP[3:0]	Action
1	X	X	Enter MPSM on MRW
X	1	1111	Enter MPSM on MRW
0	0	X	Exit MPSM on MRW
0	X	Not equal to 1111	Exit MPSM on MRW

4.12.1 MPSM Idle State

When DDR5 SDRAM is in this state, it ignores all types of commands except MRW, ODT, Power Down Entry (PDE) and Self Refresh Entry (SRE) commands. Only MRW commands to Exit MPST Idle, as described in Table 65, shall be issued. For any other MRW command the DRAM shall first be taken out of MPSM Idle, then the MRW command may be issued. ODT, PDE and SRE commands are executed normally. DRAM shall not respond to any other command except these four command types. DLL status is same as in normal idle state. DRAM continues to drive CA ODT as programmed.

Normal command timing parameters are applied in this state, except that tREFI doesn't need to be satisfied as Refresh command doesn't need to be issued in this state.

4.12.2 MPSM Power Down State

MPSM Power Down state is entered by Power Down Entry command from MPSM Idle state. When DDR5 SDRAM is in this state, it responds to ODT command normally as it does in precharged power down state. DLL status is same as in normal precharged power down state.

When the Power Down Exit command is issued, the DRAM goes back to the MPSM Idle state after tXP. Normal Power Down command timings are applied in this state, except the tREFI requirement.

4.12.3 MPSM Deep Power Down State

MPSM Deep Power Down (DPD) state is entered and exited by Self Refresh Entry and Exit commands from/to MPSM Idle state. Input signal requirements to the DRAM in this state are same to those in the Self Refresh mode. DRAM shall not execute any internal Refresh operation in this state.

When the Self Refresh Exit command is issued, the DRAM goes back to the MPSM Idle state after tXS. tXS_DLL must be met prior to issuing any commands that require a locked DLL. Normal Self Refresh command timings are applied in this state.

4.12.4 MPSM Command Timings

The device can exit from the MPSM Idle state by programming the MPSM enable (MR2:OP[1]) bit to '0' using the MRW command. MPSM exit to the first valid command delay is tMPSMX.

Table 66 — Maximum Power Saving Mode Timing Parameters

Symbol	Description	Min	Max	Unit
tMPSMX	MPSM exit to first valid command delay	tMRD	-	ns

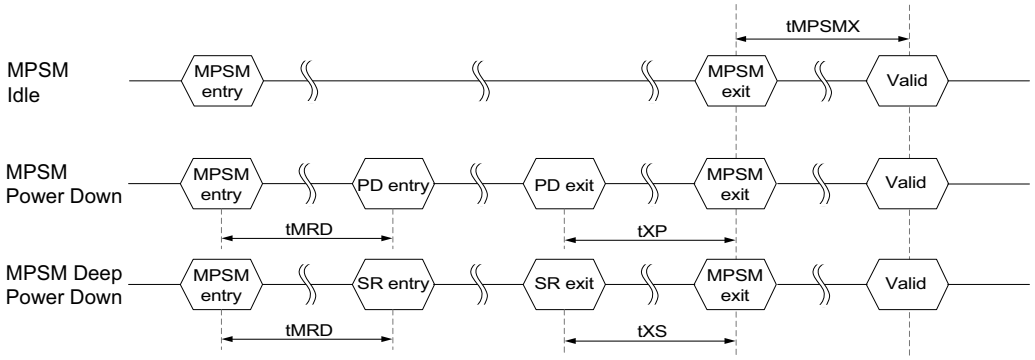


Figure 68 — Maximum Power Saving Mode Exit Timings

4.13 Refresh Operation

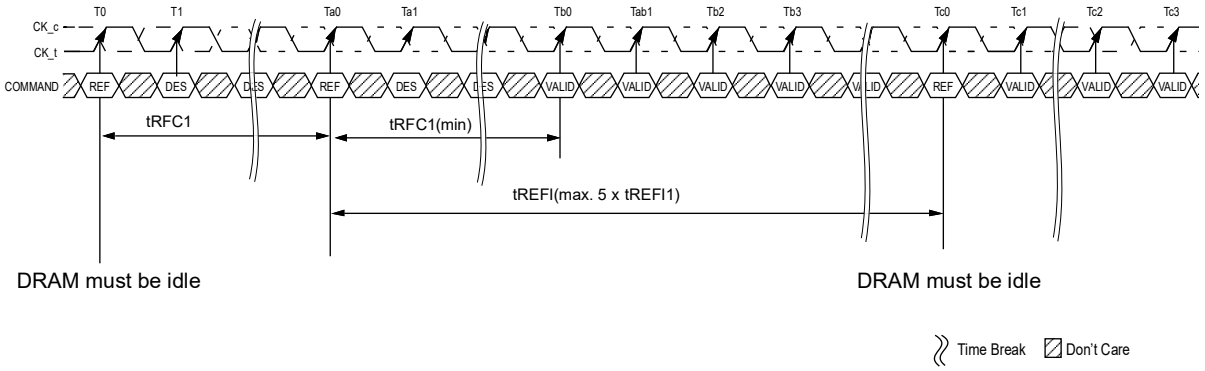
The Refresh command (REF) is used during normal operation of the DDR5 SDRAM. Since “data” is stored as 0s and 1s in capacitors in a DRAM, and the capacitors leak charge over time, the Refresh command is issued periodically to restore (refresh) the electrical charge in the capacitors. Each refresh command results in one or more Activate operations to a selected row or rows, followed by a self-timed Precharge to close the rows opened during the Activate. The Refresh command is non persistent, so it must be issued each time a refresh is required. The DDR5 SDRAM requires Refresh commands to be issued at an average periodic interval of tREFI.

There are three types of refresh operations supported by DDR5 SDRAMs.

- Normal Refresh: By issuing All Bank Refresh (REFab) command in Normal Refresh mode
- Fine Granularity Refresh: By issuing All Bank Refresh (REFab) command in Fine Granularity Refresh mode
- Same Bank Refresh: By issuing Same Bank Refresh (REFsb) command in Fine Granularity Refresh mode

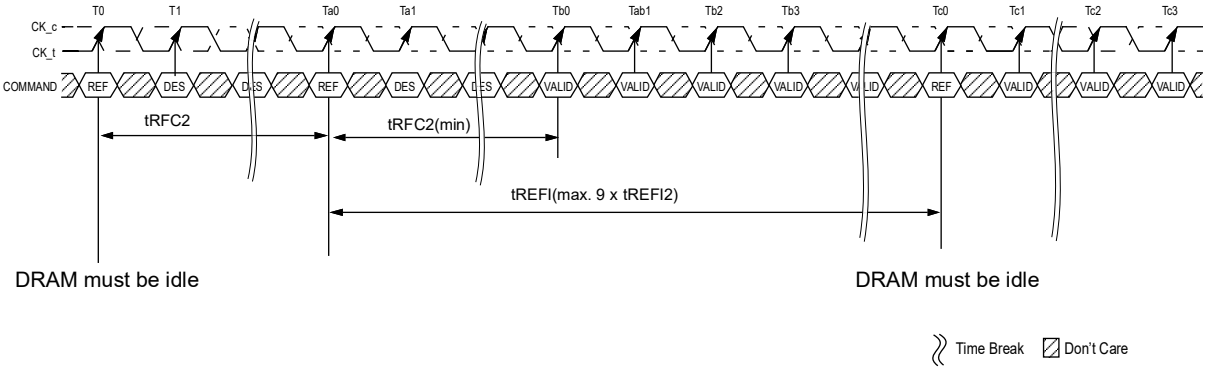
This clause describes the details of the refresh operations and requirements for each of the refresh operation types as well as the transitions between the refresh operation types.

For Normal Refresh and Fine Granularity Refresh operations, all banks of the SDRAM must be precharged and idle for a minimum of the precharge time tRP(min) before the All Bank Refresh command (REFab) can be issued. The refresh addressing is generated by the internal refresh controller during the refresh cycle. The external address bus is only required to be in a valid state once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Refresh command and the next valid command, except DES, PDE, NOP (PDX) and non-Target ODT commands, must be greater than or equal to the minimum Refresh cycle time tRFC(min) as shown in Figure 69 and Figure 70. Note that the tRFC timing parameter depends on memory density and the refresh mode setting, which can be set to Normal Refresh mode or Fine Granularity Refresh (FGR) mode.



NOTE: 1. Only DES, PDE, NOP (PDX) or non-Target ODT commands are allowed after Refresh command is issued until tRFC1(min) expires.
2. Time interval between two Refresh commands may be extended to a maximum of 5 x tREFI1.

Figure 69 — Refresh Command Timing (Example of Normal Refresh Mode)



NOTE: 1. Only DES, PDE, NOP (PDX) or non-Target ODT commands are allowed after Refresh command is issued until tRFC2(min) expires.
2. Time interval between two Refresh commands may be extended to a maximum of 9 x tREFI2.

Figure 70 — Refresh Command Timing (Example of Fine Granularity Refresh Mode)

4.13.1 Refresh Modes

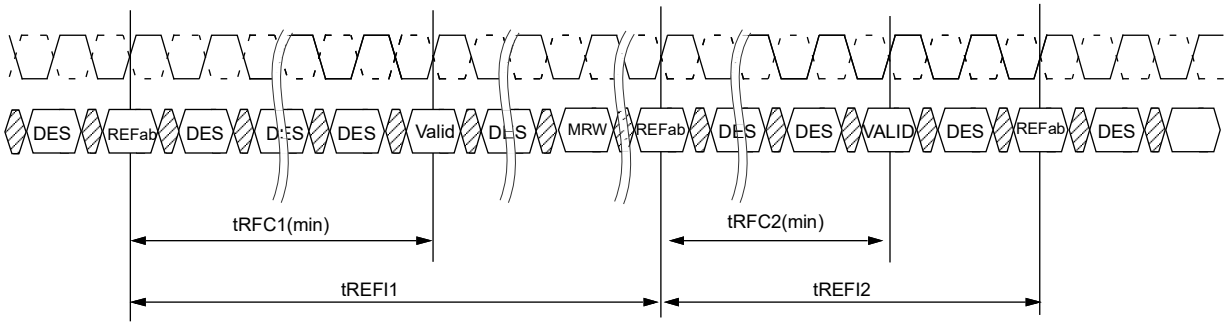
The DDR5 SDRAM has two different Refresh modes with two different refresh cycle time (tRFC) settings. There is a Normal Refresh mode setting and a Fine Granularity Refresh (FGR) mode setting. The FGR mode provides a shorter refresh cycle time (tRFC2) but also requires All Bank Refresh commands (REFab) to be provided twice as often (tREFI is divided by two, i.e. tREFI2 = tREFI1/2). The Refresh mode setting is programed by MRW command as shown in Table 67. The Refresh Modes are fixed until changed by MRW command to MR4 OP[4]. No on-the-fly Refresh mode change is supported.

Table 67 — Mode Register Definition for Refresh Mode

MR4 OP[4]	Refresh Mode (tRFC Setting)
0	Normal Refresh Mode (tRFC1)
1	Fine Granularity Refresh Mode (tRFC2)

4.13.2 Changing Refresh Mode

If Refresh Mode is changed by MRW, the new tREFI and tRFC parameters would be applied from the moment of the rate change. As shown in Figure 71, when an All Bank Refresh command is issued to the DRAM in Normal Refresh mode, then tRFC1 and tREFI1 are applied from the time that the command (REFab) was issued. And when an All Bank Refresh command is issued in Fine Granularity Refresh (FGR) mode, then tRFC2 and tREFI2 should be satisfied.



NOTE: 1. Refresh mode is Normal Refresh mode before the MRW and FGR mode after the MRW

Figure 71 — Refresh Mode Change Command Timing

The following conditions must be satisfied before the Refresh mode can be changed. Otherwise, data retention of DDR5 SDRAM cannot be guaranteed.

1. In the Normal Refresh mode, the REFab command must complete and tRFC1 must be satisfied before issuing the MRW command to change the Refresh Mode.
2. If performing REFab commands in the Fine Granularity Refresh mode, it is recommended that an even number of REFab commands are issued to the DDR5 SDRAM since the last change of the Refresh mode with an MRW command before the Refresh mode is changed again by another MRW command. If this condition is met, no additional Refresh commands are required upon the Refresh mode change. If this condition is not met, one extra REFab command is required to be issued to the DDR5 SDRAM upon Refresh mode change. This extra Refresh command is not counted toward the computation of the average refresh interval (tREFI1). This extra Refresh counts toward the maximum number of refreshes which may be postponed. See Figure 72.
3. If performing REFsb commands, it is recommended that all banks have received an even number of REFsb command since the last change of the Refresh mode with an MRW command before the Refresh mode is changed again by another MRW command, since a REFab command will reset the internal bank counter. If this condition is met, no additional refresh commands are required upon the Refresh mode change. If this condition is not met, one extra REFab command is required to be issued to the DDR5 SDRAM upon Refresh mode change. These extra Refresh commands are not counted toward the computation of the average refresh interval (tREFI1). These extra Refresh commands count toward the maximum number of refreshes which may be postponed. See Figure 73 for 16 Gb and higher density DRAM with 4 banks in a bank group example.

4.13.2 Changing Refresh Mode (cont'd)

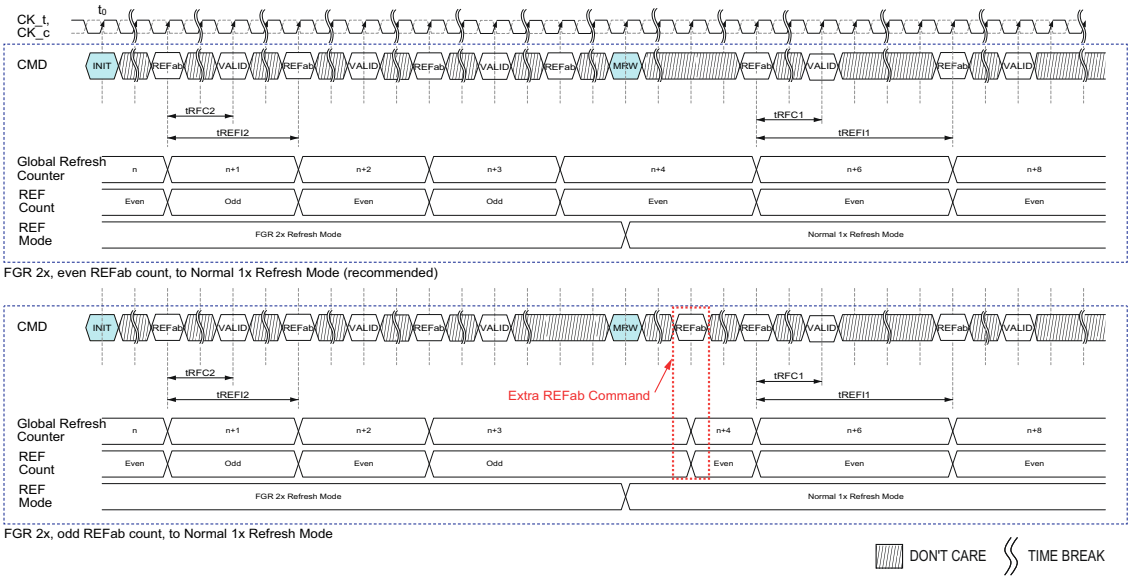
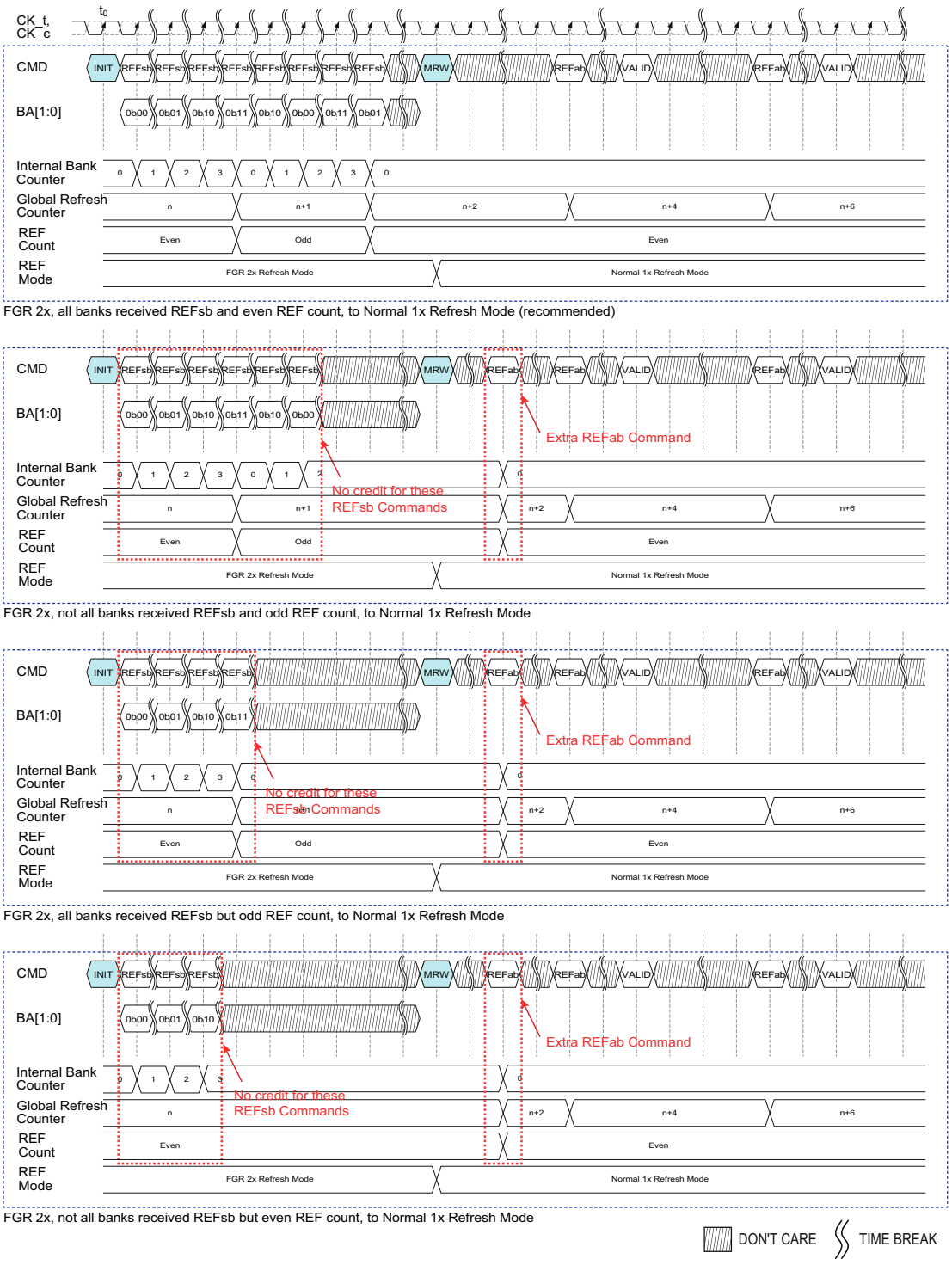


Figure 72 — Refresh Mode Change from FGR 2x to Normal 1x Command Timing

4.13.2 Changing Refresh Mode (cont'd)



FGR 2x, all banks received REFsb and even REF count, to Normal 1x Refresh Mode (recommended)

FGR 2x, not all banks received REFsb and odd REF count, to Normal 1x Refresh Mode

FGR 2x, all banks received REFsb but odd REF count, to Normal 1x Refresh Mode

FGR 2x, not all banks received REFsb but even REF count, to Normal 1x Refresh Mode

Figure 73 — 16 Gb and Higher Density DRAM Refresh Mode Change from FGR 2x REFsb to Normal 1x Command Timing

4.13.3 Same Bank Refresh

Same Bank Refresh command (REFsb) allows the DDR5 DRAM to apply the refresh process to a specific bank in each bank group unlike the All Bank Refresh command (REFab) which applies the refresh process to all banks in every bank group. The determination whether a Same Bank Refresh or an All Bank Refresh is executed by the DRAM depends on whether REFsb or REFab command is issued, as shown in the command truth table. The REFsb command is only allowed in FGR mode (MR4[OP4]=1).

The first Same Bank Refresh command (REFsb) to each bank increments an internal bank counter and once the bank counter equals the number of available banks in a bank group, it will reset and start over on the next subsequent REFsb. Each time the internal bank counter resets and starts over on the next subsequent REFsb, the global refresh counter will also increment. A REFsb command can be issued to any bank and in any bank order. A subsequent REFsb command issued to the same bank prior to every bank receiving a REFsb command will repeat refreshing the same row since the SDRAM's global refresh counter will not increment until all banks in a bank group receive a REFsb command. The first REFsb command issued is the "Synchronization" REFsb command and the "Synchronization" count resets the internal bank counter to zero when either:

(a) every bank has received one REFsb command,

(b) RESET is applied,

(c) entering/exiting self refresh mode, or

(d) REFab is issued

The DRAM's global refresh counter increments when either a REFab is issued or when all banks have received their one REFsb command and the "Synchronization" count reset to zero. If a REFab command is issued when the bank counter is not zero, i.e., in the middle of same-bank refreshing, the SDRAM's global refresh counter will not increment until the completion of REFab, effectively losing the credits for any REFsb commands issued prior to the REFab. See the 16 Gb and Higher Density DRAM Bank and Refresh counter increment behavior table for details.

Table 68 — 16 Gb and Higher Density DRAM Bank and Refresh Counter Increment Behavior

Count #	Command	BA1	BA0	Refresh Bank #	Internal Bank Counter #	Global Refresh Counter # (Row Address #)
0	RESET, REFab, or SRE/SRX command and FGR mode on (MR4[OP4]=1)				To 0	-
1	REFsb	0	0	0	0 to 1	n
2	REFsb	0	1	1	1 to 2	
3	REFsb	1	0	2	2 to 3	
4	REFsb	1	1	3	3 to 0	
5	REFsb	1	0	2	0 to 1	n+1
6	REFsb	0	0	0	1 to 2	
7	REFsb	1	1	3	2 to 3	
8	REFsb	0	1	1	3 to 0	
9	REFsb	0	0	0	0 to 1	n+2
10	REFsb	0	1	1	1 to 2	
11	***REFab***	***V***	***V***	***0-3***	***To 0***	
12	REFsb	1	1	3	0 to 1	n+3
13	REFsb	0	1	1	1 to 2	
14	REFsb	0	0	0	2 to 3	
15	REFsb	1	0	2	3 to 0	
16	***REFab***	***V***	***V***	***0-3***	***To 0***	n+4
17	***REFab***	***V***	***V***	***0-3***	***To 0***	n+5
18	***REFab***	***V***	***V***	***0-3***	***To 0***	n+6
19	REFsb	1	1	3	0 to 1	n+7
20	***REFab***	***V***	***V***	***0-3***	***To 0***	
21	REFsb	1	0	2	0 to 1	n+8
22	REFsb	0	1	1	1 to 2	
23	REFsb	0	0	0	2 to 3	
24	REFsb	1	1	3	3 to 0	

4.13.3 Same Bank Refresh (cont'd)

The REFsb command must not be issued to the device until the following conditions are met:

- tRFC1 or tRFC2 has been satisfied after the prior 1x or 2x REFab command(s), respectively
- tRFCsb has been satisfied after the prior REFsb command
- tRP has been satisfied after the prior PRECHARGE command to that bank
- tRRD_L has been satisfied after the prior ACTIVATE command (e.g. tRRD_L has to be met from ACTIVATE of a different bank in the same bank group to the REFsb targeted at the same bank group)

Additional restrictions for issuing the REFsb and RFMsb/RFMab commands:

- For mono devices, REFsb and RFMsb count as ACTIVATE commands for the four activate window timing restriction (tFAW).
- For 3DS devices, REFsb and RFMsb count as ACTIVATE commands for the four activate window timing restriction to the same logical rank (tFAW_slr).
- For 3DS devices, REFsb, REFab, RFMsb and RFMab count as ACTIVATE commands for the four activate window timing restriction to different logical ranks (tFAW_dlr).

Once a REFsb is issued, the target banks (one in each Bank Group) are inaccessible during the same-bank refresh cycle time (tRFCsb); however, the other banks in each bank group are accessible and can be addressed during this same-bank refresh cycle. When the same-bank refresh cycle has completed, the banks refreshed via the REFsb will be in idle state.

After issuing REFsb command, the following conditions must be met:

- tRFCsb must be satisfied before issuing a REFab command
- tRFCsb must be satisfied before issuing an ACTIVATE command to the same bank
- tREFSBRD must be satisfied before issuing an ACTIVATE command to a different bank.

Table 69 — Refresh Command Scheduling Separation Requirements

Symbol	Min Delay From	To	Notes
tRFC1	REFab	REFab	1
		ACTIVATE command to any bank	
tRFC2	REFab	REFab	2
		ACTIVATE command to any bank	
		REFsb	
tRFCsb	REFsb	REFab	2
		ACTIVATE command to same bank as REFsb	
		REFsb	
tREFSBRD	REFsb	ACTIVATE command to different bank from REFsb	2
tRRD_L	ACTIVATE	REFsb to different bank from ACTIVATE	2
tRRD_L_slr	ACTIVATE	REFsb to different bank in same logical rank in 3DS	2
tRRD_dlr	ACTIVATE	REFab/REFsb to different logical rank in 3DS	2

NOTE 1 MR4(OP[4]) set to Normal Refresh mode.
NOTE 2 MR4(OP[4]) set to FGR mode. REFsb command is valid only in FGR mode.

4.13.4 tREFI and tRFC Parameters

The maximum average refresh interval (tREFI) requirement for the DDR5 SDRAM depends on the refresh mode setting (Normal or FGR), and the device's case temperature (Tcase). When the refresh mode is set to Normal Refresh mode, REFab commands are issued (tRFC1), and Tcase<=85 °C, the maximum average refresh interval (tREFI1) is tREFI. When the refresh mode is set to FGR mode, REFab commands are issued (tRFC2) and Tcase<=85 °C, the maximum average refresh interval (tREFI2) is tREFI/2. This same tREFI/2 interval value is also appropriate if the refresh mode is set to Normal Refresh mode and REFab commands are issued (tRFC1) but 85 °C<Tcase<=95 °C. Finally, if the refresh mode is set to FGR mode, REFab commands are issued (tRFC2), and 85 °C<Tcase<=95 °C, the maximum average refresh interval (tREFI2) is tREFI/4.

The DDR5 SDRAM includes an optional method for the host to indicate when Refresh commands are being issued at the 2x (tREFI2) refresh interval rate. The 2x Refresh Interval Rate indicator (MR4:OP[3]) alerts the DRAM if the host supports the refresh interval rate indication as part of the REF command using CA8. If enabled (MR4:OP[3]=1), the host will issue 1x REF commands with CA8=H (Tcase<=85 °C), and the host will issue 2x REF commands with CA8=L (Tcase any allowable temperature). MR4:OP[3] is a Status Read/Write "SR/W" MR bit which shows DDR5 SDRAM support of this optional feature. Reading MR4:OP[3] will return a "1" if the 2x Refresh Interval Rate indicator is supported. A "0" will be returned if not supported. tREFI is based on the 8,192 refresh commands that need to be issued within the baseline tREF=32 ms refresh period on the DDR5 SDRAM.

4.13.5 tREFI and tRFC Parameters for 3DS Devices

Typical platforms are designed with the assumption that no more than one physical rank is refreshed at the same time. In order to limit the maximum refresh current (IDD5B1) for a 3D stacked SDRAM, it will be required to stagger the refresh commands to each logical rank in a stack.

The tRFC time for a single logical rank is defined as tRFC_slr and is specified as the same value as for a monolithic DDR5 SDRAM of equivalent density. The minimum amount of stagger between refresh commands sent to different logical ranks (tRFC_dlr) or physical ranks (tRFC_dpr) is specified to be approximately tRFC_slr/3 - seeTable 72.

Table 70 — tREFI Parameters for REFab and REFsb Commands (including 3DS)

Command	Refresh Mode	Symbol and Range		Expression	Value	Unit	Notes
REFab	Normal	tREFI1	0 °C <= TCASE <= 85 °C	tREFI	3.9	µs	1, 2
			85 °C < TCASE <= 95 °C	tREFI/2	1.95	µs	1, 2
REFab	Fine Granularity	tREFI2	0 °C <= TCASE <= 85 °C	tREFI/2	1.95	µs	1, 2
			85 °C < TCASE <= 95 °C	tREFI/4	0.975	µs	1, 2
REFsb	Fine Granularity	tREFIsb	0 °C <= TCASE <= 85 °C	tREFI/(2*n)	1.95/n	µs	1, 2, 3
			85 °C < TCASE <= 95 °C	tREFI/(4*n)	0.975/n	µs	1, 2, 3

NOTE 1 All 3D Stacked (3DS) devices follow the same requirements as the monolith die regardless of logical rank.
NOTE 2 3DS specification covers up to 16Gb density. Future densities such as 24 Gb or 32 Gb could require different tREFI requirements.
NOTE 3 *n* is the number of banks in a bank group (e.g. 8G: n=2; 16G: n=4).

Table 71 — tRFC Parameters by Device Density

Refresh Operation	Symbol	8 Gb	16 Gb	24 Gb	32 Gb	Units	Notes
Normal Refresh (REFab)	tRFC1(min)	195	295	410	410	ns	
Fine Granularity Refresh (REFab)	tRFC2(min)	130	160	220	220	ns	
Same Bank Refresh (REFsb)	tRFCsb(min)	115	130	190	190	ns	

4.13.5 tREFI and tRFC Parameters for 3DS Devices (cont'd)

Table 72 — 3DS and DDP tRFC Parameters by Logical Rank Density

Refresh Operation	Symbol	8 Gb	16 Gb	24 Gb	32 Gb	Units	Notes
Normal Refresh with 3DS same logical rank	tRFC1_slr(min)	tRFC1(min)				ns	1
Fine Granularity Refresh with 3DS same logical rank	tRFC2_slr(min)	tRFC2(min)				ns	1
Same Bank Refresh with 3DS same logical rank	tRFCsb_slr(min)	tRFCsb(min)				ns	1
Normal Refresh with 3DS different logical rank	tRFC1_dlr(min)	tRFC1(min)/3				ns	3, 6
Normal Refresh with 3DS or DDP different physical rank	tRFC1_dpr(min)	tRFC1min/3				ns	2, 3, 6
Fine Granularity Refresh with 3DS different logical rank	tRFC2_dlr(min)	tRFC2(min)/3				ns	3, 4
Fine Granularity Refresh with 3DS or DDP different physical rank	tRFC2_dpr(min)	tRFC2min/3				ns	2, 3, 4
Same Bank Refresh with 3DS different logical rank	tRFCsb_dlr(min)	tRFCsb(min)/3				ns	3, 5

NOTE 1 All 3D Stacked (3DS) devices follow the same requirements as the monolith die for same logical ranks

NOTE 2 Parameter applies to all DDP, or dual-physical-rank (36 and 40 placement) 3DS-based DIMMs built with JESD301-1 "PMIC 5000/PMIC5010 Power Management IC Standard", but may not apply to DIMMs built with higher current capacity PMICs.

NOTE 3 3DS and DDP tRFC parameters are to be rounded up to the nearest 1ns after the "tRFC*min"/3 calculation.

NOTE 4 Parameter applies, from REFab to REFab, from REFab to REFsb.

NOTE 5 Parameter applies, from REFsb to REFsb, from REFsb to REFab.

NOTE 6 Parameter applies, from REFab to REFab.

Table 73 — Same Bank Refresh Parameters

Refresh Mode	Symbol	8 Gb	16 Gb	24 Gb	32 Gb	Units
Same Bank Refresh to ACT delay	tREFSBRD(min)	30	30	30	30	ns

Table 74 — Refresh Parameters for 3DS 2H, 4H

Refresh Mode	Symbol	8 Gb	16 Gb	24 Gb	32 Gb	Units
Same Bank Refresh to ACT delay SLR	tREFSBRD_slr(min)	30	30	30	30	ns
Same Bank Refresh to ACT delay DLR	tREFSBRD_dlr(min)	15	15	15	15	ns
All Bank Refresh to ACT delay DLR	tREFABRD_dlr(min)	15	15	15	15	ns

4.13.6 Refresh Operation Scheduling Flexibility

In general, a Refresh command needs to be issued to the DDR5 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided.

In Normal Refresh mode, a maximum of 4 REFab commands can be postponed, meaning that at no point in time more than a total of 4 Refresh commands are allowed to be postponed. In case that 4 REFab commands are postponed in a row, the resulting maximum interval between the surrounding REFab commands is limited to 5 × tREFI1 (see Figure 74). At any given time, a maximum of 5 REFab commands can be issued within 1 x tREFI1 window. Self-refresh mode may be entered with a maximum of 4 REFab commands being postponed. After exiting Self-Refresh mode with one or more REFab commands postponed, additional REFab commands may be postponed to the extent that the total number of postponed REFab commands (before and after the Self-Refresh) will never exceed 4. During Self-Refresh Mode, the number of postponed REFab commands does not change. An additional REFab command is required after Self-Refresh exit (refer to Clause 4.9 for more information).

In FGR Mode, the maximum REFab commands that may be postponed is 8, with the resulting maximum interval between the surrounding REFab commands limited to 9 x tREFI2 (see Figure 75). At any given time, a maximum of 9 REFab commands can be issued within 1 x tREFI2 window. The same maximum count of 8 applies to postponed REFab commands around self-refresh entry and exit. An additioinal REFab command is required after Self-Refresh exit (refer to Clause 4.9 for more information). Where *n* is the number of banks in a bank group, a single REFab command can be replaced with *n* REFsb commands for the purpose of scheduling postponed refresh commands.

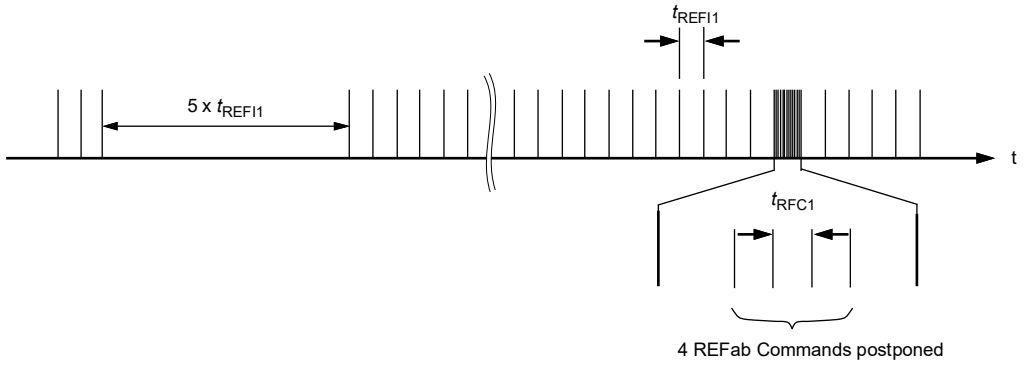


Figure 74 — Postponing Refresh Commands
(Example of Normal Refresh Mode - tREFI1, tRFC1)

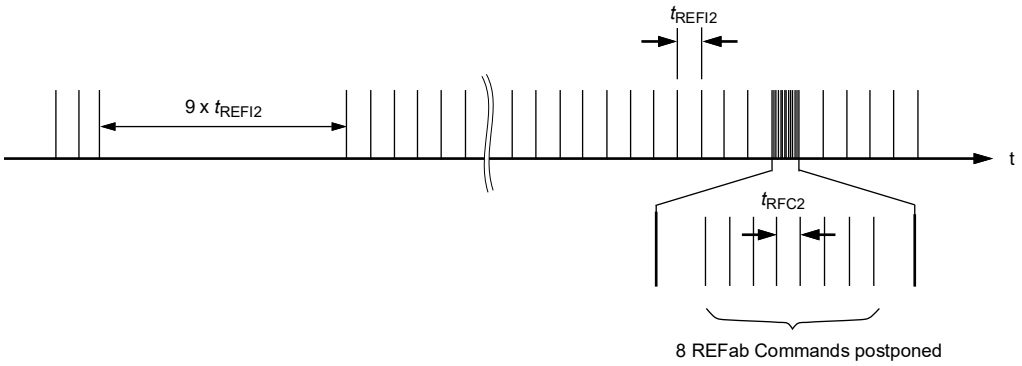


Figure 75 — Postponing Refresh Commands
(Example of Fine Granularity Refresh Mode - tREFI2, tRFC2)

4.13.7 Self Refresh Entry and Exit

DDR5 SDRAM can enter Self Refresh mode anytime in Normal Refresh and FGR mode without any restriction on the number of Refresh commands that have been issued during the mode before the Self Refresh entry. However, upon Self Refresh exit, one additional Refresh must be issued in addition to the normally scheduled Refresh commands (refer to Clause 4.9 for more information). Plus, extra Refresh command(s), in addition to the aforementioned additional Refresh, may also be required depending on the condition of the Self Refresh entry. The conditions and requirements for the extra Refresh command(s) are defined as follows:

1. There are no special restrictions for the Normal Refresh mode.

2. If performing REFab commands in FGR mode, it is recommended that there should be an even number of REFab commands before entry into Self Refresh since the last Self Refresh exit or MRW command that set the FGR mode. If this condition is met, no additional refresh commands are required upon Self Refresh exit. If this condition is not met, one extra REFab command is required to be issued to the DDR5 SDRAM upon Self Refresh exit. This extra Refresh command is not counted toward the computation of the average refresh interval (tREFI2). This extra Refresh counts toward the maximum number of refreshes which may be postponed. Refer to Clause 4.9 for more information. See Figure 76.

3. If performing REFsb commands, it is recommended that all banks have received a REFsb command prior to entering Self Refresh, since entering and exiting Self Refresh will reset the internal bank counter. If this condition is met, no additional refresh commands are required upon Self Refresh exit, and REFsb commands again can be issued to any bank in any bank order. If this condition is not met, one extra REFab command or an extra REFsb command to each bank is required to be issued to the DDR5 SDRAM upon Self Refresh exit. These extra Refresh commands are not counted toward the computation of the average refresh interval (16Gb and higher density DRAM with 4 banks per bank group example: tREFI2 - see Figure 77). These extra Refresh commands count toward the maximum number of refreshes which may be postponed. Refer to Clause 4.9 for more information.

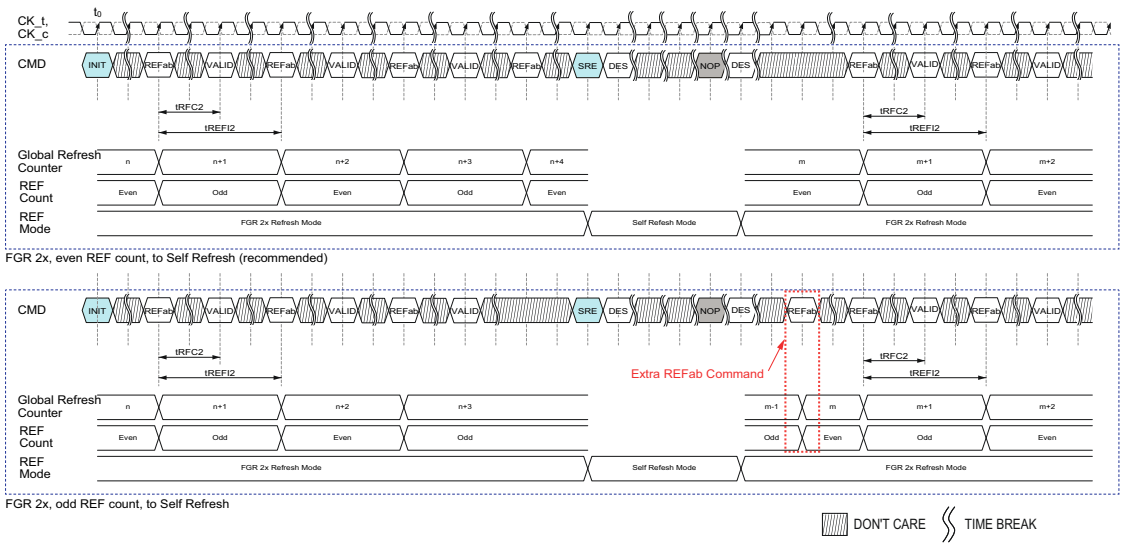
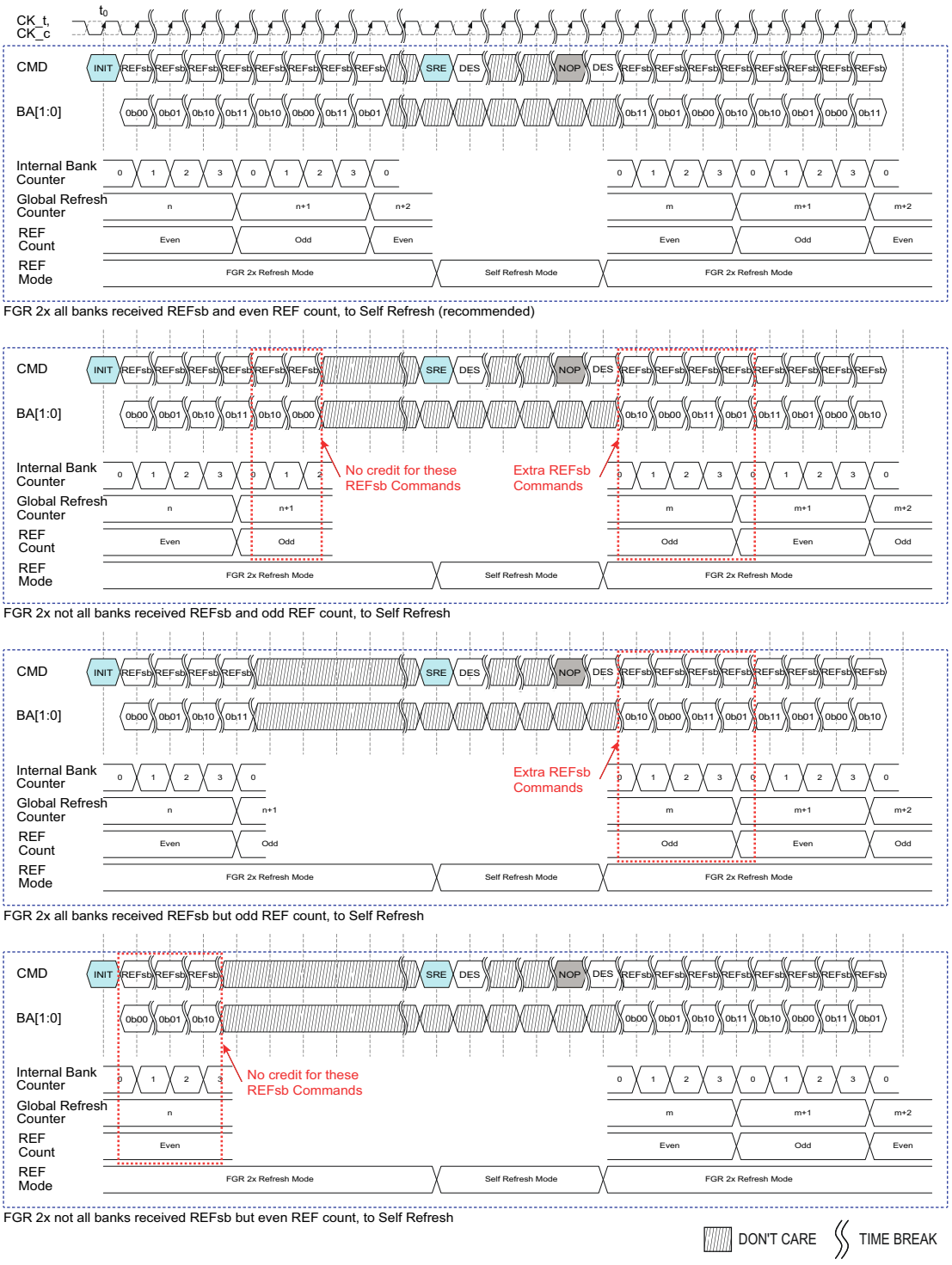


Figure 76 — FGR 2x to SREF Command Timing

4.13.7 Self Refresh Entry and Exit (cont'd)



FGR 2x all banks received REFsb and even REF count, to Self Refresh (recommended)

FGR 2x not all banks received REFsb and odd REF count, to Self Refresh

FGR 2x all banks received REFsb but odd REF count, to Self Refresh

FGR 2x not all banks received REFsb but even REF count, to Self Refresh

Figure 77 — 16 Gb and Higher Density DRAM FGR 2x REFsb to SREF Command Timing

4.14 Temperature Sensor

DDR5 devices feature a temperature sensor whose status (MR4:OP[2:0]) can be read to determine the minimum required refresh rate. Either the temperature sensor readout or the device TOPER may be used by the system to determine whether the refresh rate and operating temperature requirements are being met. Additionally, the device's temperature status (MR4:OP[2:0]) can be read by the system to determine the current approximate temperature range sensed by the device.

DDR5 devices shall monitor device temperature and update MR4 according to tTSI. Upon completion of device initialization, the device temperature status bits shall be no older than tTSI. MR4 will be updated even when device is in Self Refresh state.

When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification that applies for the standard or elevated temperature ranges. For example, TCASE may be above 85°C when MR4:OP[2:0]=010B. DDR5 devices shall allow for 2 °C temperature margin between the point at which the device updates the MR4 value and the point at which the controller reconfigures the system accordingly.

When MR4:OP[5]=0 (wide range temperature sensor not supported), the four thresholds of the temperature sensor will be nominally 80 °C, 85 °C, 90 °C, and 95 °C. The 2nd threshold (nominally 85 °C) is used by the system to switch to 2x refresh. The 4th threshold (nominally 95 °C) is used by the system to throttle activity to keep the DRAM at a safe operating temperature. The 1st threshold (nominally 80 °C) allows the system to take actions which delay reaching the 2nd threshold. The 3rd threshold (nominally 90 °C) allows the system to take actions which delay reaching the 4th threshold.

When MR4:OP[5]=1 (optional wide range temperature sensor range supported), the six thresholds of the temperature sensor will be nominally 75 °C, 80 °C, 85 °C, 90 °C, 95 °C, and 100 °C. The 3rd threshold (nominally 85 °C) is used by the system to switch to 2x refresh. The 5th threshold (nominally 95 °C) is used by the system to throttle activity to keep the DRAM at a safe operating temperature. The 6th threshold (nominally 100 °C) is used by the system to perform emergency actions such as forcing the system to power down. Support for temperature sensor readings above 95 °C does not imply the DDR5 DRAM device may operate properly above 95 °C - side effects may include loss of data integrity.

To ensure proper operation using the temperature sensor, applications should consider the following factors:

- TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2 °C, measured in the range of interest 80-100 °C.
- ReadInterval is the time period between MR4 reads from the system.
- TempSensorInterval (tTSI) is the maximum delay between internal updates of MR4.
- SysRespDelay is the maximum time between a read of MR4 and the response by the system.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$TempGradient \times (ReadInterval + tTSI + SysRespDelay) \leq TempMargin$$

Table 75 — Temperature Sensor Parameters

Parameter	Symbol	Min/Max	Value	Unit	Notes
System Temperature Gradient	TempGradient	Max	System Dependent	°C/s	
MR4 Read Interval	ReadInterval	Max	System Dependent	ms	
Temperature Sensor Interval	tTSI	Max	32	ms	
System Response Delay	SysRespDelay	Max	System Dependent	ms	
Device Temperature Margin	TempMargin	Max	2	°C	1
Temp Sensor Accuracy, 2nd threshold trip point	TempSensorAcc2	Min	78	°C	1, 2
Temp Sensor Accuracy, 4th threshold trip point	TempSensorAcc4	Min	88	°C	1, 2
Relative Trip Point, 2nd threshold minus 1st threshold	RelativeTrip2m1	Min/Max	Min 3 / Max 7	°C	1, 3
Relative Trip Point, 3rd threshold minus 2nd threshold	RelativeTrip3m2	Min/Max	Min 3 / Max 7	°C	1, 4
Relative Trip Point, 4th threshold minus 3rd threshold	RelativeTrip4m3	Min/Max	Min 3 / Max 7	°C	1, 4

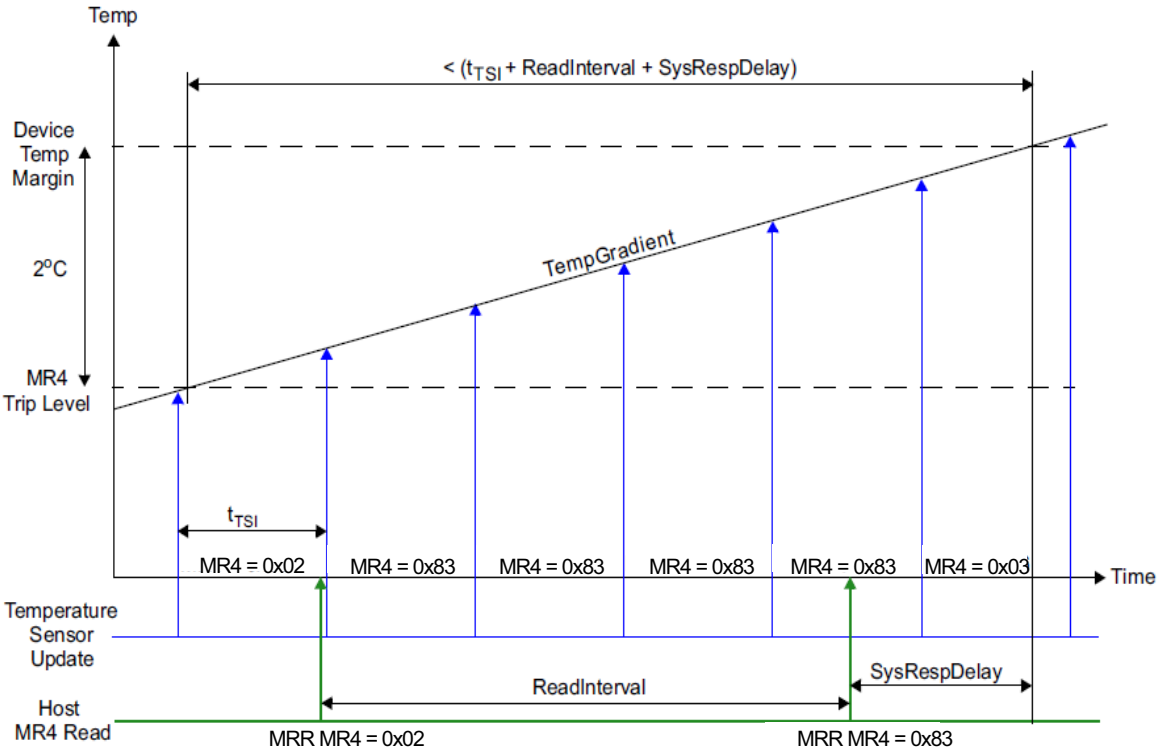
NOTE 1 Verified by design and characterization, and may not be subject to production test.
NOTE 2 Only the minimum (negative side) is specified for the second and fourth thresholds. The DRAM vendor is responsible for guaranteeing correct operation of 1x refresh for MR4 <= 010b, and correct operation of 2x refresh for MR4 <= 100b. This puts a vendor-specific constraint on the Temperature Sensor Accuracy on the positive side.
NOTE 3 The 1st threshold is defined relative to the 2nd threshold.
NOTE 4 The 3rd threshold is defined relative to the 2nd and 4th thresholds.

4.14 Temperature Sensor (cont'd)

For example, if TempGradient is 10 °C/s and the SysRespDelay is 100 ms:

(10 °C/s) x (ReadInterval + 32 ms + 100 ms) ≤ 2 °C

In this case, ReadInterval shall be no greater than 68 ms.



Note: MR4 encodings in the above figure are examples only and assume that MR4:OP[4]=0

Figure 78 — Temperature Sensor Timing Diagram

4.14.1 Temperature Sensor Usage for 3D Stacked (3DS) Devices

In the case of 3D Stacked devices, the Refresh Rate (MR4) is related to the hottest die in the stack only.

4.14.2 Temperature Encoding

The DDR5 DRAM provides temperature related information to the controller via an encoding on MR4:OP[2:0]. The encodings define the proper refresh rate expected by the DRAM to maintain data integrity.

4.14.3 MR4 Definition for Reference only - See Mode Register Section for Details

Table 76 — MR4 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TUF	RFU		Refresh tRFC Mode	Refresh Interval Rate Indicator	Refresh Rate		

Table 77 — MR4 Register Encoding

Function	Register Type	Operand	Data	Notes
Refresh Rate	R	OP[2:0]	000_B: RFU 001_B: tREFI x1 (1x Refresh Rate), <80°C nominal 010_B: tREFI x1 (1x Refresh Rate), 80-85°C nominal 011_B: tREFI /2 (2x Refresh Rate), 85-90°C nominal 100_B: tREFI /2 (2x Refresh Rate), 90-95°C nominal 101_B: tREFI /2 (2x Refresh Rate), >95°C nominal 110_B: RFU 111_B: RFU	1, 2, 3, 4, 5, 6, 7
Refresh Interval Rate Indicator	SR/W	OP[3]	DRAM Status Read (SR): 0_B: Not implemented (Default) 1_B: Implemented Host Write (W): 0_B: Disabled (Default) 1_B: Enabled	
Refresh tRFC Mode	R/W	OP[4]	0_B: Normal Refresh Mode (tRFC1) 1_B: Fine Granularity Refresh Mode (tRFC2)	
RFU	R/W	OP[6:5]	RFU	
TUF (Temperature Update Flag)	R	OP[7]	0_B: No change in OP[2:0] since last MR4 read (default) 1_B: Change in OP[2:0] since last MR4 read	

NOTE 1 The refresh rate for each OP[2:0] setting applies to tREFI1 and tREFI2. Each OP[2:0] setting specifies a nominal temperature range. The five ranges defined by OP[2:0] are determined by four temperature thresholds.

NOTE 2 The four temperature thresholds are nominally at 80 °C, 85 °C, 90 °C, and 95 °C. The 85 °C and 95 °C thresholds have a specified minimum temperature value, but the maximum temperature value is not specified.

NOTE 3 DRAM vendors must report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.

NOTE 4 The 2x Refresh Rate must be provided by the system before the DRAM Tj has gone up by more than 2 °C (Temperature Margin) since the first report out of OP[2:0]=011B. This condition is reset when OP[2:0] is equal to 010B.

NOTE 5 The device may not operate properly when OP[2:0]=101B, if the DRAM Tj has gone up by more than 2 °C (Temperature Margin) since the first report out of OP[2:0]=101B. This condition is reset when OP[2:0] is equal to 100B. OP[2:0]=101B must be a temporary condition of the DRAM, to be addressed by immediately reducing the Tj of the DRAM by throttling its power, and/or the power of nearby devices.

NOTE 6 OP[7] = 0 at power-up. OP[2:0] bits are valid after initialization sequence (Te).

NOTE 7 See the section on “Temperature Sensor” for information on the recommended frequency of reading MR4

4.15 Multi-Purpose Command (MPC)

4.15.1 Introduction

DDR5-SDRAMs use the Multi-Purpose Command (MPC) to issue commands associated with interface initialization, training, and periodic calibration. The MPC command is initiated with CS_n, and CA[4:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. The MPC command has eight operands (OP[7:0]) that are decoded to execute specific commands in the SDRAM.

The MPC command uses an encoding that includes the command encoding and the opcode payload in a single clock cycle. This enables the host to extend the setup and hold for the CA signals beyond the single cycle when the chip select asserts. In addition, the MPC command will support multiple cycles of CS_n assertion. The multiple cycles of CS_n assertion ensures the DRAM will capture the MPC command during at least one rising CK_t/CK_c edge.

Table 78 — MPC Function Definition

Function	Abbre-viation	CS_n	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
MPC	MPC	L	H	H	H	H	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V	1
NOTE 1 See Command Truth Table for details																	

4.15.2 MPC Opcodes

Table 79 specifies the opcode assignments for the MPC operations.

Table 79 — MPC Function Definition for OP[7:0]

Function	Operand	Data	Notes
Initialization and Training Modes	OP[7:0]	$0000\ 0000_B$: Exit CS Training Mode $0000\ 0001_B$: Enter CS Training Mode $0000\ 0010_B$: DLL RESET $0000\ 0011_B$: Enter CA Training Mode $0000\ 0100_B$: ZQCal Latch $0000\ 0101_B$: ZQCal Start $0000\ 0110_B$: Stop DQS Interval Oscillator $0000\ 0111_B$: Start DQS Interval Oscillator $0000\ 1000_B$: Set 2N Command Timing $0000\ 1001_B$: Set 1N Command Timing $0000\ 1010_B$: Exit PDA Enumerate Programming Mode $0000\ 1011_B$: Enter PDA Enumerate Programming Mode 0000 1100B: Manual ECS Operation 0000 1101B: RFU ...thru 0001 1110B: RFU 0001 1111B: Apply VrefCA, VrefCS and RTT_CA/CS/CK 0010 0xxxB: Group A RTT_CK = xxx (See MR32:OP[2:0] for encoding) 0010 1xxxB: Group B RTT_CK = xxx (See MR32:OP[2:0] for encoding) 0011 0xxxB: Group A RTT_CS = xxx (See MR32:OP[5:3] for encoding) 0011 1xxxB: Group B RTT_CS = xxx (See MR32:OP[5:3] for encoding) 0100 0xxxB: Group A RTT_CA = xxx (See MR33:OP[2:0] for encoding) 0100 1xxxB: Group B RTT_CA = xxx (See MR33:OP[2:0] for encoding) 0101 0xxxB: Set DQS _RTT_PARK = xxx (See MR33:OP[5:3] for encoding) 0101 1xxxB: Set RTT_PARK = xxx (See MR34:OP[2:0] for encoding) 0110 xxxxB: PDA Enumerate ID = xxxx (See encoding table below) 0111 xxxxB: PDA Select ID = xxxx (See encoding table below) 1000 xxxxB: Configure tDLLK/tCCD_L = xxxx (See MR13:OP[3:0] for encoding) 1001 0001B: CS Geardown Enable All Others: Reserved	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

NOTE 1 See command truth table for more information.

NOTE 2 Refer to the CS Training Mode section for more information regarding CS Training Mode Entry and Exit.

NOTE 3 Refer to the CA Training Mode section for more information regarding CA Training Mode Entry.

NOTE 4 Refer to the ZQ Calibration section for more information regarding ZQCal Start and ZQCal Latch.

NOTE 5 Refer to the DQS Interval Oscillator section for more information regarding Start DQS Interval Oscillator and Stop DQS Interval Oscillator

NOTE 6 Refer to the Per DRAM Addressability section for more information regarding Enter PDA Mode and Exit PDA Mode.

NOTE 7 Refer to the CA_ODT Strap Operation section for more information regarding Group A and Group B configurations for RTT_CA, RTT_CS, and RTT_CK.

NOTE 8 “Apply VrefCA, VrefCS and RTT_CA/CS/CK” applies the settings previously sent with the VrefCA or VrefCS command and “MPC Set RTT_CA/CS/CK”. Until this “MPC Apply VrefCA, VrefCS and RTT_CA/CS/CK” command is sent, the values are in a shadow register. Any MRR to the VrefCA, VrefCS and RTT_CA/CS/CK settings should return only the applied value. The shadow register shall retain the previously set value, so that any time the “MPC Apply VrefCA, VrefCS and RTT_CA/CS/CK” command is sent, there is no change in the applied value unless a new VrefCA , VrefCS or RTT_CA/CS/CK value was sent to the shadow register since the previous “MPC Apply VrefCA, VrefCS and RTT_CA/CS/CK” command.

NOTE 9 The PDA Enumerate ID and PDA Select ID opcodes include a 4-bit value, designated by xxxxB in the table. This is the value that is programmed into the MR for these fields. The PDA Enumerate ID can only be changed while in PDA Enumerate Programming Mode.

NOTE 10 For any MPC command that is associated with a Mode Register, the only way to program that Mode Register is via the MPC command. Those Mode Registers will be read only and will not support MRW.

NOTE 11 MPC command “tDLLK/tCCD_L” sets the settings to the MR13 shadow registers and applies the settings to MR13 when theDRAM encounters MPC command “DLL RESET” or SRE with CA9=”L”.

NOTE 12 The MPC function “DLL RESET” requires tMPC_delay to all commands that do not require a locked DLL. tDLLK_min shall be satisfied prior to issuing any commands that require a locked DLL. REFab/REFsb/RFMab/RFMsb shall not be issued during tRFC1 after issuing the MPC “DLL RESET” function. See Section on Self Refresh Operation for the full list of commands that require or do not require a locked DLL.

4.15.2 MPC Opcodes (cont'd)

Table 80 — PDA Enumerate and Select ID Encoding

MPC Function	OP[7:4]	OP[3:0]	Notes
PDA Enumerate ID	0110	0000_B: ID 0 0001_B: ID 1 0010_B: ID 2 0011_B: ID 3 0100_B: ID 4 0101_B: ID 5 0110_B: ID 6 0111_B: ID 7 1000_B: ID 8 1001_B: ID 9 1010_B: ID 10 1011_B: ID 11 1100_B: ID 12 1101_B: ID 13 1110_B: ID 14 1111_B: ID 15 - default	
PDA Select ID	0111	0000_B: ID 0 0001_B: ID 1 0010_B: ID 2 0011_B: ID 3 0100_B: ID 4 0101_B: ID 5 0110_B: ID 6 0111_B: ID 7 1000_B: ID 8 1001_B: ID 9 1010_B: ID 10 1011_B: ID 11 1100_B: ID 12 1101_B: ID 13 1110_B: ID 14 1111_B: ID 15 - This selects all devices regardless of their enumerate ID.	

4.15.3 MPC Function Timings

As shown in the following figures, the MPC CMD timings are extended when Multi-Cycle CS assertion mode (MR2:OP[4]) is set to zero. The CS_n is also asserted for multiple consecutive cycles, limited by tMPC_CS. All timings will be relative to the final rising CK_t/CK_c within the CS_n assertion window. The min delay from when the MPC command is captured to the next valid command is specified as tMPC_Delay. Prior to VrefCS, VrefCA, CS and CA Training completing successfully, the CA will be driven with additional setup and hold beyond the CS_n assertion. For the DRAM to latch the MPC command in cases where the alignment between CS_n, CA, and CK may be unknown, the CA inputs shall reach the proper command state and provide at least three cycles of setup prior to CS_n transitioning from high to low, CS_n shall remain low for tMPC_CS, and CA shall remain in the proper command state for and provide at least three cycles of hold after CS_n transitions from low to high. This additional setup and hold is only needed when MR2:OP[4] is set to 0 (Multi-Cycle CS assertion duration mode).

4.15.3 MPC Function Timings (cont'd)

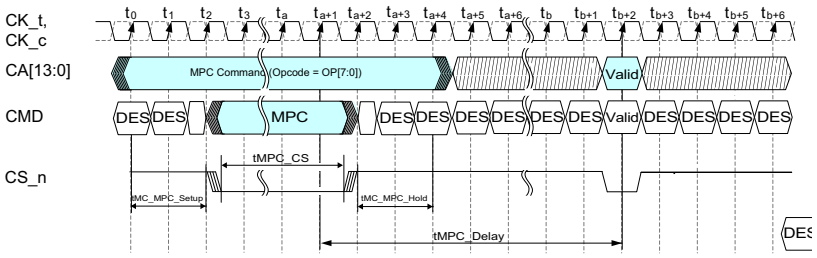


Figure 79 — MPC Function Timing to 1-Cycle Command

The DDR5 DRAM will support a MR setting to indicate when a Multi-Cycle CS_n assertion may be used for the MPC, VrefCA and VrefCS commands. MR2:OP[4] defaults to "0" upon a reset. Once MR2:OP[4] =1 (single-cycle CS_n assertion) has been set, the host is required to change MR2:OP[4]=0 if any multi-cyle CS_n timings are used.

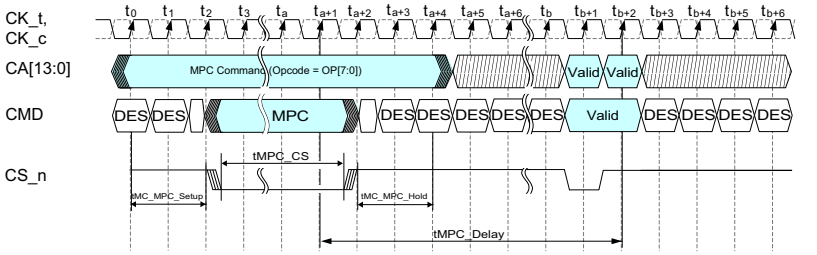


Figure 80 — MPC Function Timing to 2-Cycle Command

Table 81 — MPC, VrefCA, and VrefCS CS Assertion Duration

MR Address	Operating Mode	Description
MR2:OP[4]	CS Assertion Duration	0_B: **Only** Multiple cycles of CS assertion supported for MPC, VrefCA and VrefCS commands 1_B: Only a single cycle of CS assertion supported for MPC, VrefCA and VrefCS commands

Default value for the CS Assertion Duration is 0, which allows for Multi-Cycle CS assertions during training.

Table 82 — AC Parameters for MPC Function

Symbol	Description	Min	Max	Unit	Note
tMPC_Delay	MPC to any other valid command delay	tMRD	-	nCK	
tMC_MPC_Setup	Min time between stable MPC command and first falling CS edge (SETUP)	3	-	nCK	2
tMC_MPC_Hold	Min time between first rising CS edge and stable MPC command (HOLD)	3	-	nCK	2
tMPC_CS	Time CS_n is held low to register MPC command	3.5	8	nCK	1

NOTE 1 The minimum tMPC_CS constraint only applies when the CS Assertion Duration setting is 0. The CS Assertion Duration MR setting shall be set (MR2:OP[4]=1_B) to enable single cycle MPC commands. The earliest time to set the CS Assertion Duration MR (MR2:OP[4]=1_B) is after VrefCS, VrefCA, CS and CA training are complete, when MRW commands can be sent to the DRAM.

NOTE 2 This applies only to Multi-Cycle MPC commands when MR2:OP[4]=0_B

4.15.3 MPC Function Timings (cont'd)

Some MPC functions require all banks to be in an Idle state, while other MPC functions can occur regardless if all banks are Idle or if some or all banks are Active. Regardless of the initial bank state requirement for an MPC function, the MPC function itself will not change the bank state between active or idle.

MPC functions that require all banks to be Idle when the MPC is issued will complete in an all banks Idle state.

MPC functions that can occur regardless of the bank state will not change the state of the bank, but other commands simultaneously executing within the duration of the MPC function may result in a change of states. For example, a Precharge command to an Active bank can change the state from Active to Idle while the MPC function is executing.

Table 83 — MPC Functions Requiring All Banks Idle State [1]

MPC Functions
CSTM (Enter/Exit)
DLL Reset
CATM (Enter)
PDA Enumeration Programming (Enter/Exit)
Manual ECS Operation
Apply VrefCA, VrefCS and RTT_CA/CS/CK
Set DQS_RTT_PARK
SET RTT_PARK
PDA Enumerate/Select ID
CS Geardown Enable
NOTE 1 For 3DS, MPC commands for All Banks Idle cases require all banks to be idle on all logical ranks.

Table 84 — MPC Functions Independent of Bank State

MPC Function
ZQCAL (Latch/Start)
DQS Interval Oscillator (Start/Stop)
Set 1N/2N Command
Configure Group A/B RTT_CA/CS/CK
Configure tDLLK/tCCD_L

Table 85 — PRE Timing Constraints Related to ZQCal Start

From Command	To Command	Minimum Delay between "From Command" and "To Command"	Unit	Note
PREab/sb/pb	ZQCal Start	1	tCK	

Table 86 — RD/WR Timing Constraints Related to MPC, VrefCS and VrefCA for All Banks Idle Cases

From Command	To Command	Minimum Delay between "From Command" and "To Command"	Unit	Note
RDA	MPC	tRTP + tRP	tCK	1, 2, 3
	VrefCA/VrefCS	tRTP + tRP	tCK	1, 2, 3
WRA	MPC	CWL + BL/2 + tWR + tRP	tCK	1, 2, 3
	VrefCA/VrefCS	CWL+BL/2 + tWR + tRP	tCK	1, 2, 3
NOTE 1 RD/WR can refer to both target ODT RD/WR and non-target ODT RD/WR NOTE 2 Selected MPC functions require all banks to be idle. This includes all banks within 3DS logical ranks. NOTE 3 Non-target rank commands are required to meet the minimum ODT requirements for DQ/DQS				

4.16 Per DRAM Addressability (PDA)

DDR5 allows programmability of a given device on a rank. As an example, this feature can be used to program different ODT or Vref values on DRAM devices on a given rank. The Per DRAM Addressability (PDA) applies to MRW, MPC, VrefCA, and VrefCS commands. Some per DRAM settings will be required prior to any training of the CA and CS timings and the DQ write timings. The MPC, VrefCA, and VrefCS command timings with extended setup/hold and Multi-Cycle CS assertion may be used for PDA commands if the CA and CS timings have not yet been trained.

DDR5 introduces a CA interface-only method for Per DRAM Addressability, by having a unique PDA Enumerate ID in each DRAM, and the ability to Group A PDA Select ID in all DRAMs. The unique PDA Enumerate ID requires the use of the DQ signals and a PDA Enumerate Programming Mode in the DRAM to program. Once the PDA Enumerate ID has been programmed, subsequent commands must not use the DQ signals (Legacy PDA mode) to designate which DRAM is selected for the command. The PDA Enumerate ID is a 4-bit field, and the PDA Select ID is also a 4-bit field. When the PDA Select ID is the same as the PDA Enumerate ID or when the PDA Select ID is set to the "All DRAM" code of 1111_B, the DRAM will apply the MPC, MRW, VrefCA, or VrefCS command. There are a few MPC commands that do not use the PDA Select ID to determine if the command will be applied. Among these MPC commands that do not use the PDA Select ID are the MPC opcodes to set the PDA Enumerate ID and the opcode to set the PDA Select ID. During RESET procedure, the receive FIFO must be initialized with all ones in order to ensure that the PDA enumerate flow does not program an enumerate ID when the strobes are not toggling. Table 87 summarizes which MPC commands are dependent on the PDA Select ID values.

Table 87 — Commands that Support or Do Not Support PDA Select ID Usage

Command	Opcode	Uses PDA Select ID to Determine When to Execute Command	NOTE
MRW	All	Yes	
VrefCA	All	Yes	
VrefCS	All	Yes	
MPC	(Group A and B) RTT_CA	Yes	
MPC	(Group A and B) RTT_CS	Yes	
MPC	(Group A and B) RTT_CK	Yes	
MPC	Set RTT_PARK	Yes	
MPC	Set DQS_RTT_PARK	Yes	
MPC	Apply VrefCA/CS and RTT_CA/CS/CK	No	
MPC	Enter PDA Enumerate Programming Mode	No	
MPC	Exit PDA Enumerate Programming Mode	No	
MPC	PDA Enumerate ID	No	1
MPC	PDA Select ID	No	
MPC	All other MPC opcodes	No	

NOTE 1 The PDA Enumerate ID is the only command that utilizes the PDA Enumerate ID Programming mode.

4.16 Per DRAM Addressability (PDA) (cont'd)

The following mode register fields are associated with Per DRAM Addressable operation:

Table 88 — PDA Mode Register Fields

MR Address	Operating Mode	Description
MR1:OP[3:0]	PDA Enumerate ID[3:0]	This is a **Read Only** MR field, which is only programmed through an MPC command with the PDA Enumerate ID opcode. $xxxx_B$ Encoding is set with MPC command with the PDA Enumerate ID opcode. This can only be set when PDA Enumerate Programming Mode is enabled and the associated DRAM's DQ0 is asserted LOW. The PDA Enumerate ID opcode includes 4 bits for this encoding. Default setting is 1111_B
MR1:OP[7:4]	PDA Select ID[3:0]	This is a **Read Only** MR field, which is only programmed through an MPC command with the PDA Select ID opcode. $xxxx_B$ Encoding is set with MPC command with the PDA Select ID opcode. The PDA Select ID opcode includes 4 bits for this encoding. 1111B = all DRAMs execute MRW, MPC, VrefCA, and VrefCS commands For all other encodings, DRAMs execute MRW, MPC, VrefCA, and VrefCS comands only if PDA Select ID[3:0] = PDA Enumerate ID[3:0], with some exceptions for specific MPC commands that execute regardless of PDA Select ID. Default setting is 1111_B

4.16.1 PDA Enumerate ID Programming

1. PDA Enumerate Programming Mode is enabled by sending one or more MPC command cycles with OP[7:0]=0000 1011B. Data Mask and PDA Enumerate are not supported for use at the same time. Either data mask shall be disabled or DM_n driven high, while PDA Enumerate Programming Mode is enabled.
2. In the PDA Enumerate Programming Mode, only the MPC command with PDA Enumerate ID opcode is qualified with DQ0 for x4/x8 and DQL0 for x16. The DRAM captures DQ0 for x4/x8 and DQL0 for x16 by using DQS_c and DQS_t for x4/x8 DQSL_c and DQSL_t for x16 signals as shown in Figure 81, where DQ is driven low after the SET PDA Enumerate ID command, and DQS starts toggling at tPDA_DQS_DELAY, and DQ is held until after DQS stops toggling. An alternate method is shown in Figure where DQ is driven low and DQS toggles continuously starting prior to the SET PDA Enumerate ID command, and remains toggling until the Exit PDA Enumerate Programming Mode command has finished. If the value on DQ0 for x4/x8 or DQL0 for x16 is 0 then the DRAM executes the MPC command to set the PDA Enumerate ID. The controller may choose to drive all the DQ bits. Only the MPC command with PDA Enumerate ID opcodes will be supported in PDA Enumerate Programming Mode, and the MPC command to exit PDA Enumerate Programming Mode does not require a DQ qualification.
3. For the "don't enumerate" case where the SDRAM ignores the PDA Enumerate ID MPC command in the PDA Enumerate Programming Mode, the DQS_t/DQS_c and DQ signals (DQSL_t/DQSL_c and DQL/DQU for x16) may be high (driven or due to RTT_PARK termination) prior to sending the MPC command to enter PDA Enumerate Programming Mode. After entering PDA Enumerate Programming Mode, the DQS and DQ signals must remain high (driven or due to RTT_PARK termination) until exiting PDA Enumerate Programming Mode. Holding the signals high will ensure that this DRAM is never set to a PDA Enumerate ID other than the default setting of 0xFH (15). Timing diagram example shown in Clause 4.16.1.2.

4.16.1 PDA Enumerate ID Programming (cont'd)

Table 89 — PDA Enumerate Results

DQS_t/DQS_c for x4/x8 DQSL_t/DQSL_c for x16	DQ0 for x4/x8 DQL0 for x16	PDA Enumerate Result	Notes
Toggling	Low - "0"	Enumerate	
Toggling	High - "1"	Don't Enumerate	
High - "1"	Low - "0"	Unknown	1, 2
High - "1"	High - "1"	Don't Enumerate	2
Differentially Low	Valid	Don't Enumerate	3

NOTE 1 DQS_t/DQS_c are differential signals and small amounts of noise could appear as "toggling", resulting in "Unknown" PDA Enumerate Results".
NOTE 2 When the DQS signals are high, the DQs shall be held high as well.
NOTE 3 "Differentially Low" is defined as DQS_t low and DQS_c high (DQSL_t low and DQSL_c high for x16)

4. A minimum of one complete BL16 set of consecutive strobe edges (8 rising edges and 8 falling edges, plus 1 rising edge and 1 falling edge for the 2 tCK and 3 tCK preambles or 2 rising edges and 2 falling edges for the 4 tCK preamble) must be sent by the host beginning at tPDA_DQS_DELAY after the associated MPC command. The DQ value is captured during any strobe edge during the valid low duration of the target DQ. Valid low time is defined as the time between tPDA_S and tPDA_H. If the DRAM captures a 0 on DQ0 (or DQL0 for x16 devices) at any strobe edge in the strobe sequence, the PDA Enumerate ID command shall be executed by the DRAM. Since the write timings for the DQ bus have not been trained, the host must ensure a minimum of one complete BL16 set of consecutive strobe edges(8 rising edges and 8 falling edges, plus 1 rising edge and 1 falling edge for 2 tCK and 3 tCK preambles or 2 rising edges and 2 falling edges for 4 tCK preamble) occurs after a period of tPDA_DQS_Delay(min) after the associated MPC command. The BC8 mode register setting in the DRAM is ignored while in PDA Enumerate Programming mode. The DQS assumes preamble/postamble requirements (including the preamble and postamble DQS_t/DQS_c toggles).

5. Prior to when the MPC command for PDA Enumerate Programming Mode entry is sent by the host, the host must drive DQS_t and DQS_c differentially low, other than when the burst of 16 strobe edges (including the preamble and postamble DQS_t/DQS_c toggles)is sent in association with the PDA Enumerate ID MPC command. The host must send preamble and postamble DQS_t/DQS_c toggles during the qualification of the PDA command. Once PDA Enumerate Programming Mode is enabled in the DRAM, the host memory controller shall wait tMPC_Delay to the time the first PDA Enumerate ID MPC command is issued.

6. In the PDA Enumerate Programming Mode, only PDA Enumerate ID MPC commands and Exit PDA Enumerate Programming Mode MPC command are allowed.

7. In the PDA Enumerate Programming Mode, the default (or previously programmed) RTT_PARK value will be applied to the DQ signals.

8. The MPC PDA Enumerate ID command cycle time is defined as tPDA_DELAY. This time is longer than the normal MPC_Delay and must be met in order to provide the DRAM time to latch the asserted DQ and complete the write operation to the PDA Enumerate ID mode register (MR1:OP[3:0], prior to the next MPC PDA Enumerate ID command shown in Figure 81.

9. To remove the DRAM from PDA Enumerate Programming Mode, send an Exit PDA Enumerate Programming MPC command, OP[7:0]=0000 1010_B. The Exit PDA Enumerate Programming Mode MPC command is never qualified by the DQ settings and is applied to all DRAMs in the rank.

10. During the PDA Enumerate ID Programming mode, only one enumerate command is allowed to a device. Once the PDA Enumerate ID is programmed, any change for the PDA Enumerate ID requires DRAM to enter into PDA Enumerate ID Programming mode.

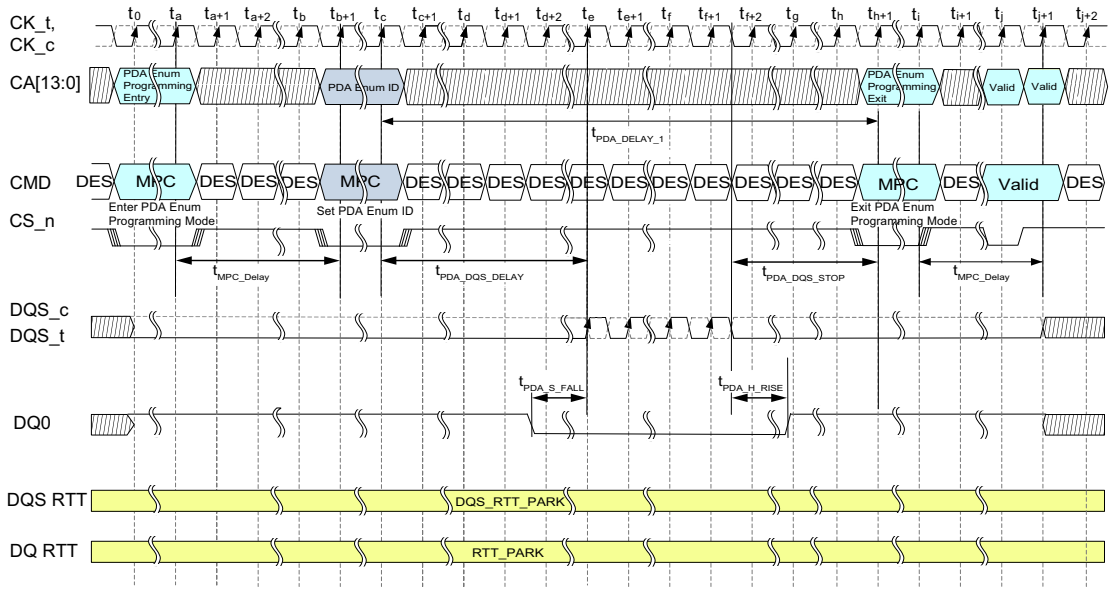
As an example, the following sequence to program the PDA Enumerate ID per device is as follows:

1. Send MPC with 'Enter PDA Enumerate Programming Mode' opcode
2. For (i = 0, i < MAX_DRAMS, i++)
   a. Send PDA Enumerate ID with i in the opcode (4-bit value), with device i's DQ signals low
3. Send MPC with 'Exit PDA Enumerate Programming Mode' opcode

Figure 81 shows a timing diagram for setting the PDA Enumerate ID value for one device. In this case only one device is programmed prior to exiting PDA Enumerate Programming Mode, but many devices may be programmed prior to exiting PDA Enumerate Programming Mode.

For a multi-device PDA Enumerate ID operation, host may choose either reiterate single device enumeration as plotted in Figure 81 and Figure 82, or follow suggested multi-device enumeration sequences as plotted in Figure 83 through Figure 85.

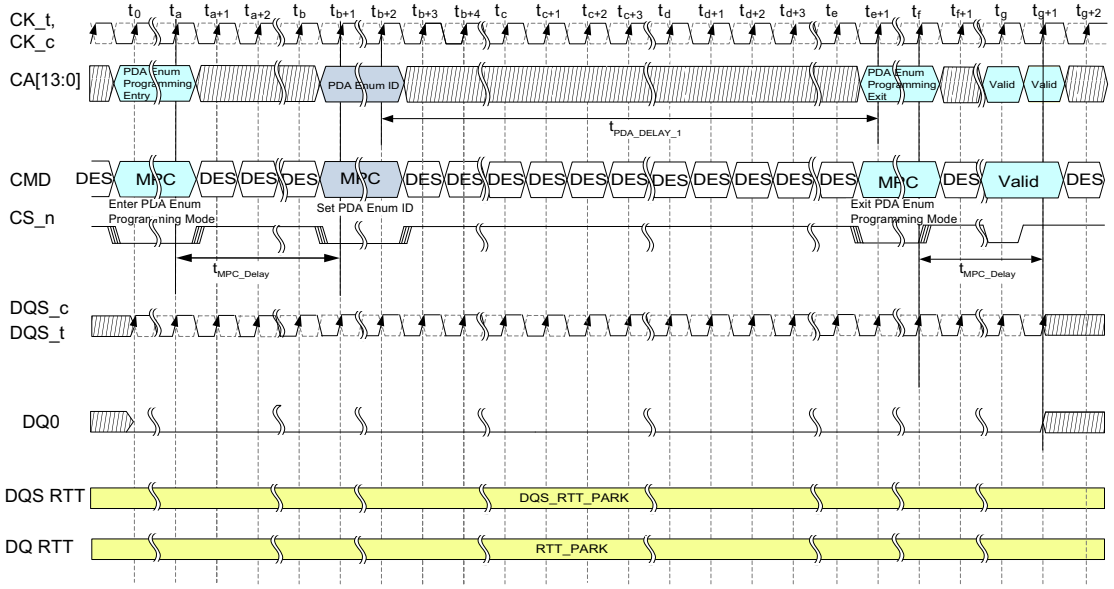
4.16.1.1 Timing Diagram of PDA Enumerate Programming with Resulting "Enumerate"



NOTES:

1. The figure assumes Multi-Cycle MPC commands, so the timings are adjusted to visually show separation betweentimings such as tMPC_DELAY (which start at the end of a command cycle and end at the beginning of the next) and other timings such as tPDA_DELAY_1.
2. The diagram above assumes preamble/postamble requirements for DQS (including 1 rising edge and 1 falling edge for the 2 tCK and 3 tCK preambles or 2 rising edges and 2 falling edges for the 4 tCK preamble).
3. tPDA_S_FALL and tPDA_H_RISE are minimum timing parameters, so DQ0 low from t_0 to t_{j+1} is valid.
4. No more than one DQ0 transition shall occur from t_0 to tPDA_S_FALL, and no more than one DQ0 transition shall occur from tPDA_H_RISE to t_{j+1}.

Figure 81 — Single Device PDA Enumerate Programming in Legacy Mode

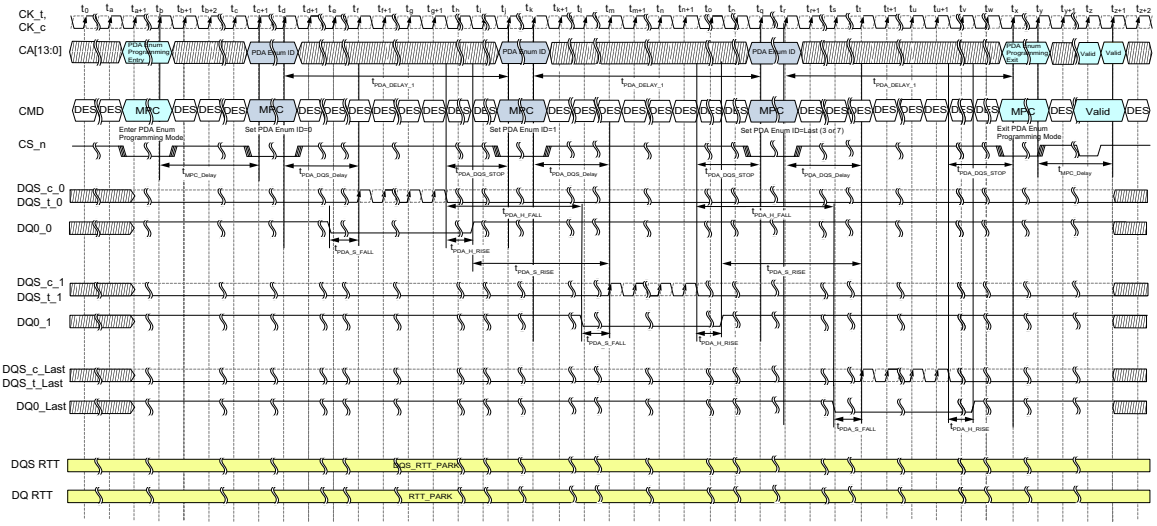


NOTES:

1. The figure assumes Multi-Cycle MPC commands, so the timings are adjusted to visually show separation between timings such as tMPC_DELAY (which start at the end of a command cycle and end at the beginning of the next) and other timings such as tPDA_DELAY_1.

Figure 82 — Single Device PDA Enumerate Programming in Continuous DQS Toggle Mode

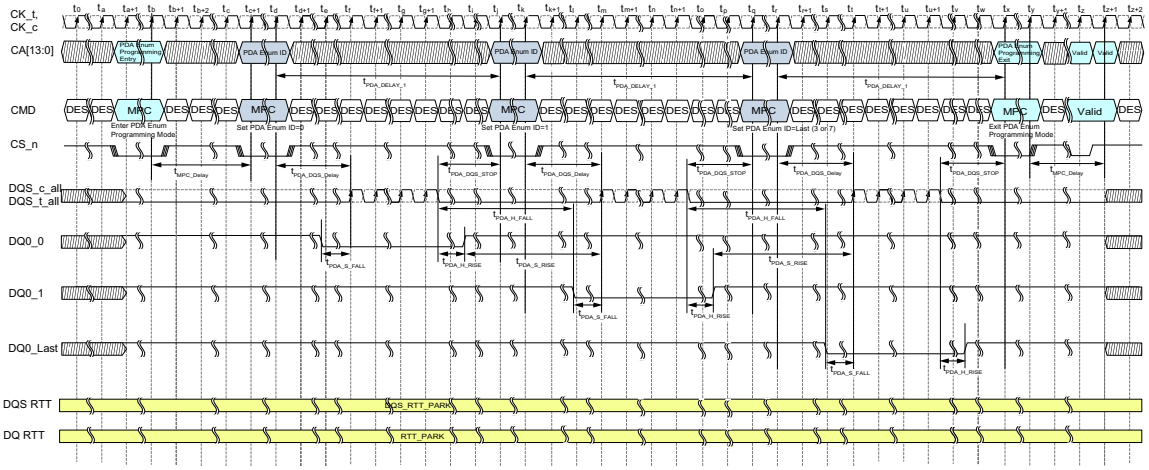
4.16.1.1 Timing Diagram of PDA Enumerate Programming with Resulting “Enumerate” (cont’d)



NOTES:

1. The figure assumes Multi-Cycle MPC commands, so the timings are adjusted to visually show separation between timings such as tMP-C_Delay (which start at the end of a command cycle and end at the beginning of the next) and other timings such as tPDA_DELAY.
2. The diagram above assumes preamble/postamble requirements for DQS (including 1 rising edge and 1 falling edge for the 2 tCK and 3 tCK preambles or 2 rising edges and 2 falling edges for the 4 tCK preamble).
3. tPDA_S_FALL and tPDA_H_RISE are minimum timing parameters, so DQ0_0 low from t_{a+1} is valid, and DQ0_Last low to t_{z+1} is valid.
4. No more than one DQ0 transition shall occur from t_{a+1} to tPDA_S_FALL, and no more than one DQ0 transition shall occur from tPDA_H_RISE to t_{z+1}.
5. tPDA_DQS_DELAY and tPDA_DQS_STOP apply to all DQ states.

Figure 83 — Multi-Device PDA Enumerate Programming in Legacy Mode with Dedicated DQS

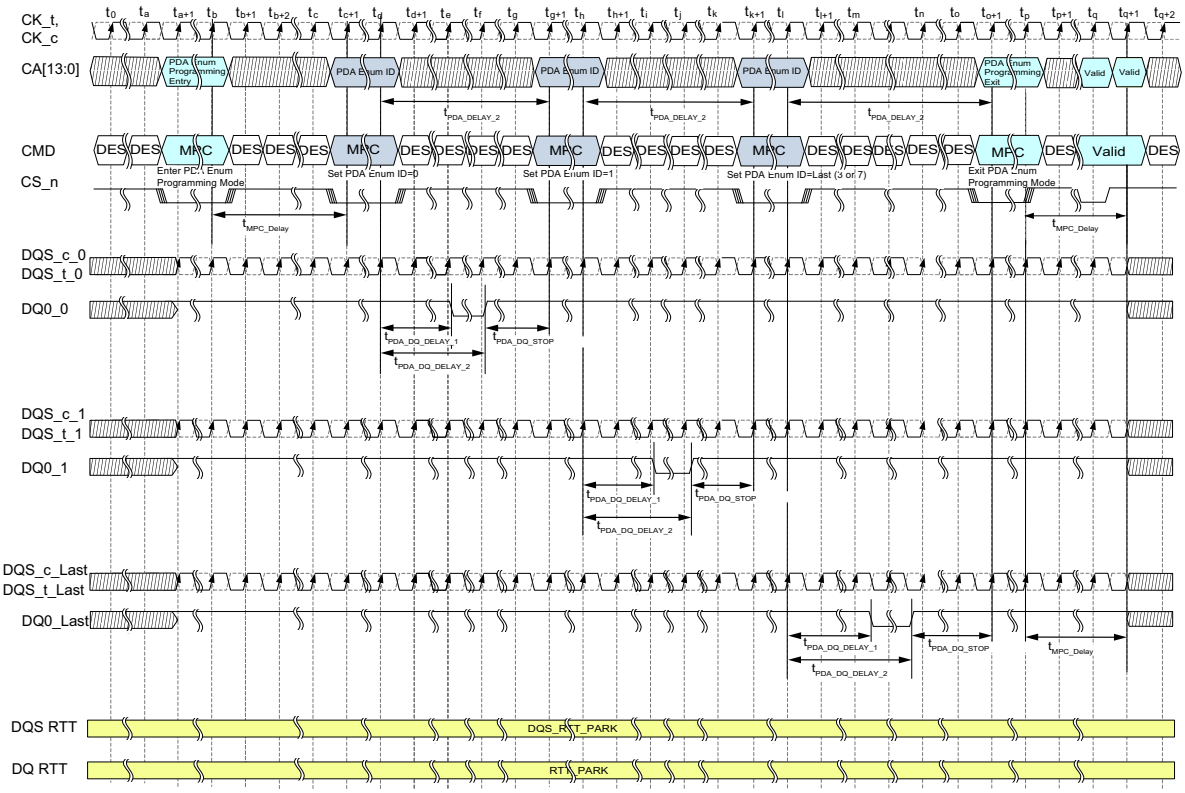


NOTES:

1. The figure assumes Multi-Cycle MPC commands, so the timings are adjusted to visually show separation between timings such as tMP-C_DELAY (which start at the end of a command cycle and end at the beginning of the next) and other timings such as tPDA_DELAY_1.
2. The diagram above assumes preamble/postamble requirements for DQS (including 1 rising edge and 1 falling edge for the 2 tCK and 3 tCK preambles or 2 rising edges and 2 falling edges for the 4 tCK preamble).
3. tPDA_S_FALL and tPDA_H_RISE are minimum timing parameters, so DQ0_0 low from t_{a+1} is valid, and DQ0_Last low to t_{z+1} is valid.
4. No more than one DQ0 transition shall occur from t_{a+1} to tPDA_S_FALL, and no more than one DQ0 transition shall occur from tPDA_H_RISE to t_{z+1}.
5. tPDA_DQS_DELAY and tPDA_DQS_STOP apply to all DQ states.

Figure 84 — Multi-Device PDA Enumerate Programming in Legacy Mode with all DQSs

4.16.1.1 Timing Diagram of PDA Enumerate Programming with Resulting “Enumerate” (cont’d)

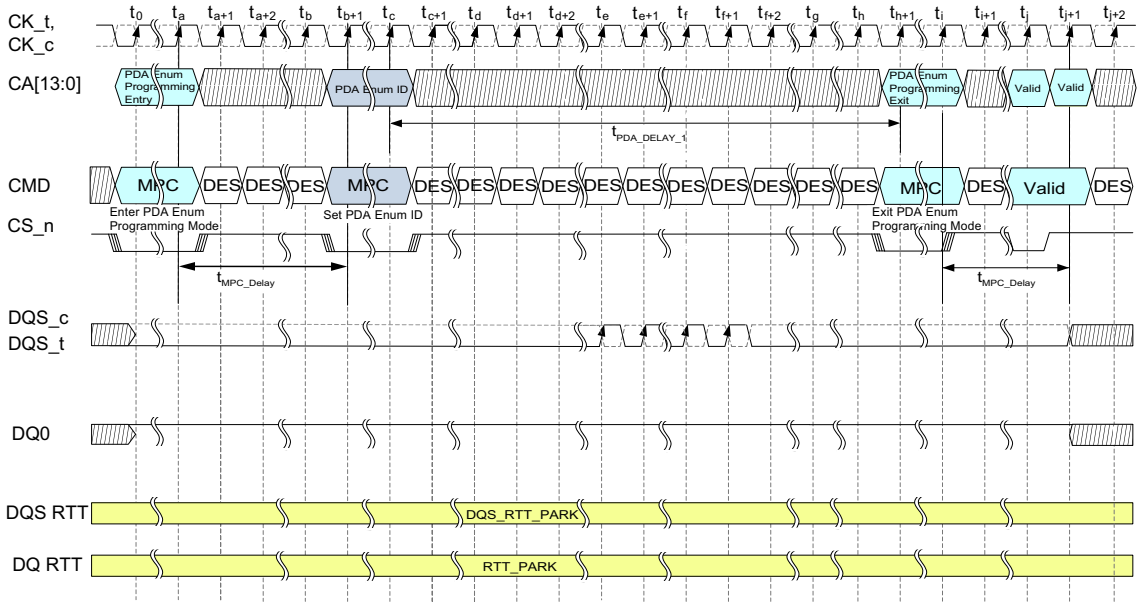


NOTES:

1. The figure assumes Multi-Cycle MPC commands, so the timings are adjusted to visually show separation between timings such as tMPC_DELAY (which start at the end of a command cycle and end at the beginning of the next) and other timings such as tPDA_DELAY_2.

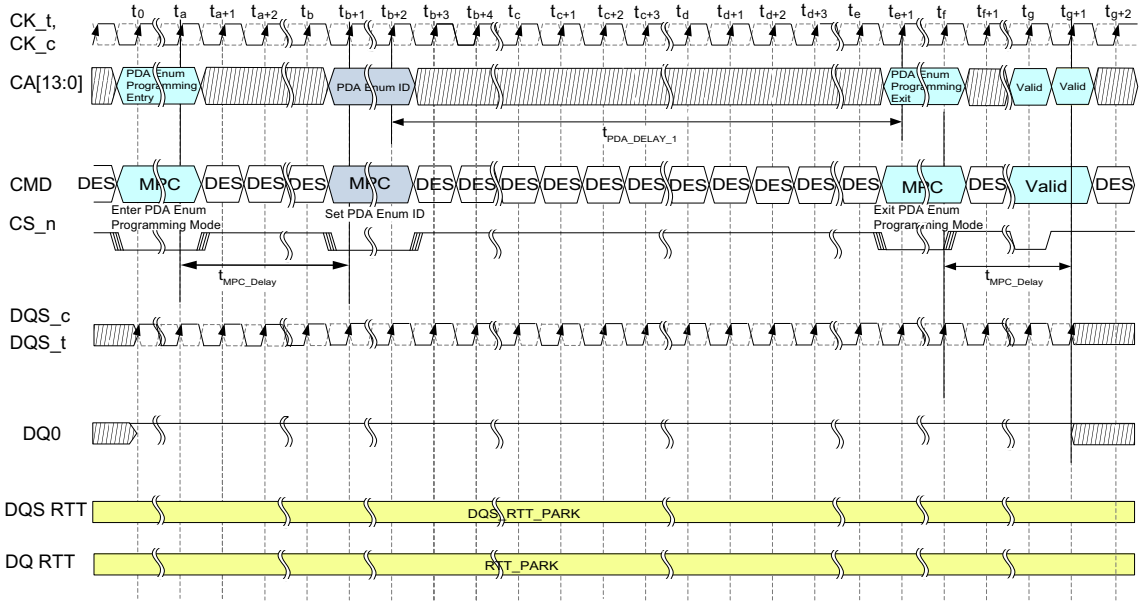
Figure 85 — Multi-Device PDA Enumerate Programming in Continuous DQS Toggle Mode

4.16.1.2 Timing Diagram of PDA Enumerate Programming with Resulting "Don't Enumerate"



NOTES:
1. The figure assumes Multi-Cycle MPC commands, so the timings are adjusted to visually show separation between timings such as tMPC_DELAY (which start at the end of a command cycle and end at the beginning of the next) and other timings such as tPDA_DELAY_1.
2. The diagram above assumes preamble/postamble requirements for DQS (including 1 rising edge and 1 falling edge for the 2 tCK and 3 tCK preambles or 2 rising edges and 2 falling edges for the 4 tCK preamble).

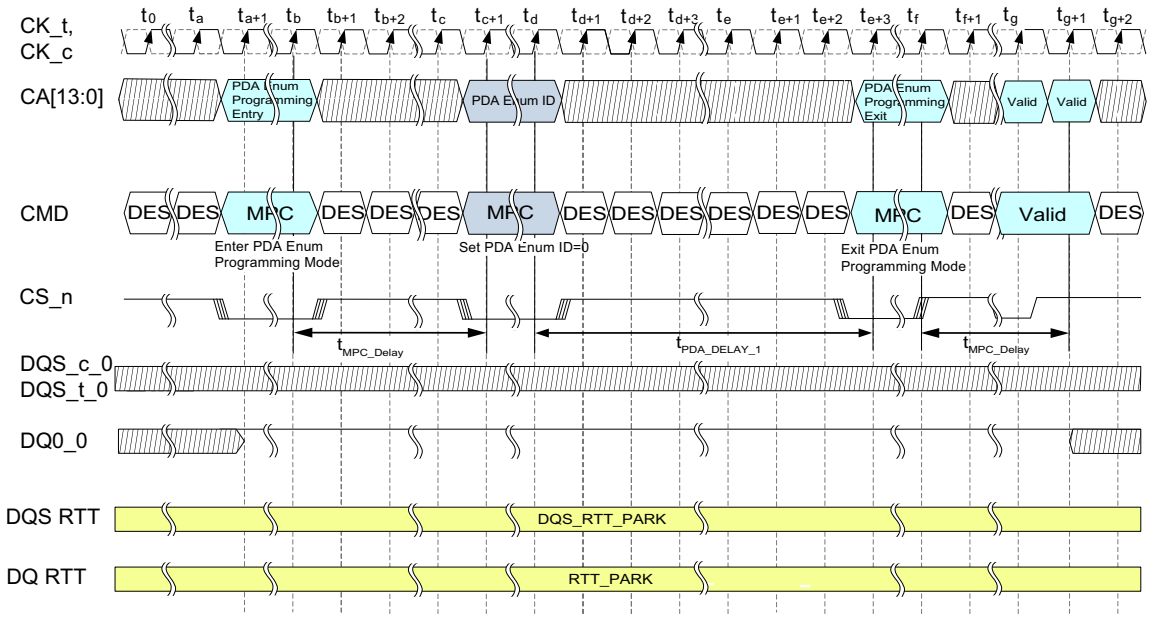
Figure 86 — Single Device PDA Enumerate Programming "Don't enumerate" Case in Legacy Mode



NOTES:
1. The figure assumes Multi-Cycle MPC commands, so the timings are adjusted to visually show separation between timings such as tMPC_DELAY (which start at the end of a command cycle and end at the beginning of the next) and other timings such as tPDA_DELAY_1.

Figure 87 — Single Device PDA Enumerate Programming "Don't Enumerate" Case in Continuous DQS Toggle Mode

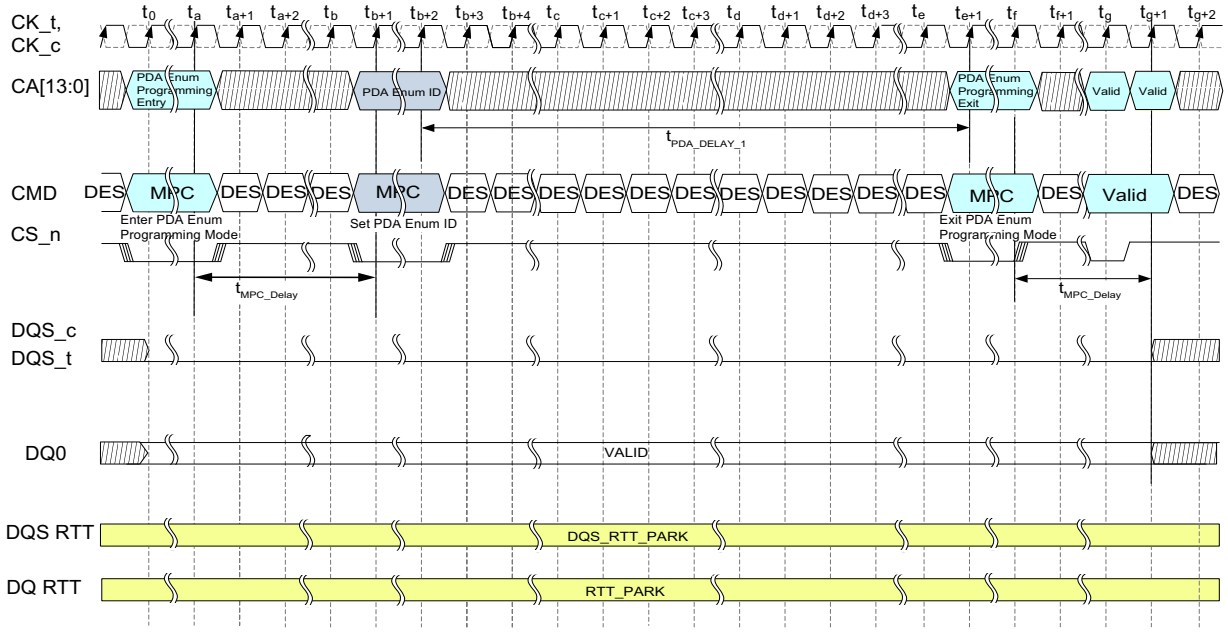
4.16.1.2 Timing Diagram of PDA Enumerate Programming with Resulting “Don’t Enumerate” (cont’d)



NOTES:

1. The figure assumes Multi-Cycle MPC commands, so the timings are adjusted to visually show separation between timings such as tMPC_DELAY (which start at the end of a command cycle and end at the beginning of the next) and other timings such as tPDA_DELAY_1.

Figure 88 — Single Device PDA Enumerate Programming “Don’t Enumerate” Case for DQ Held HIGH with any DQS State

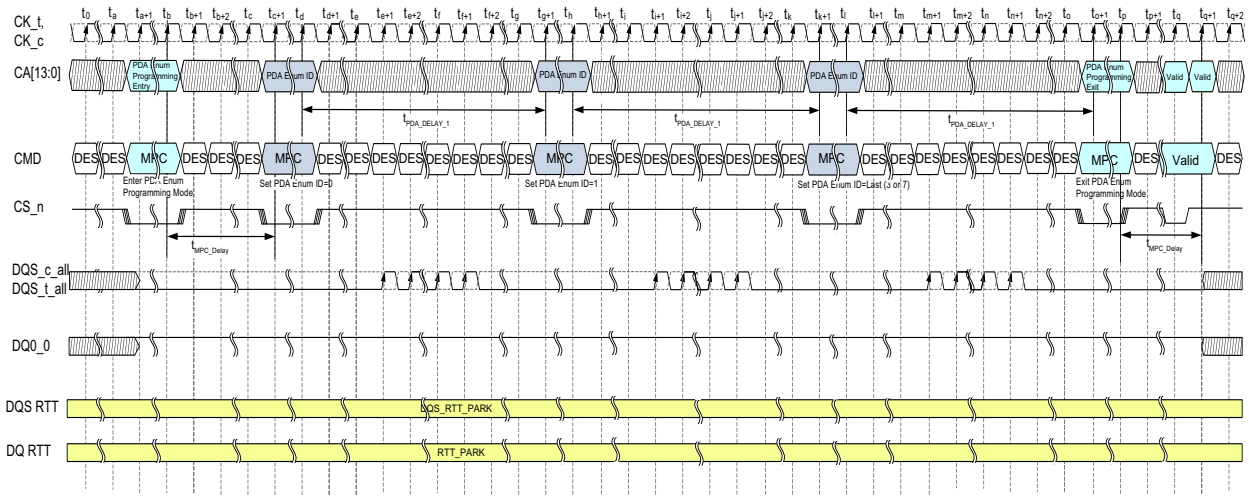


NOTES:

1. The figure assumes Multi-Cycle MPC commands, so the timings are adjusted to visually show separation between timings such as tMPC_DELAY (which start at the end of a command cycle and end at the beginning of the next) and other timings such as tPDA_DELAY_1.
2. DQ0 shall not transition during VALID state.

Figure 89 — Single Device PDA Enumerate Programming “Don’t Enumerate” Case for DQ is VALID and DQS is Differentially LOW

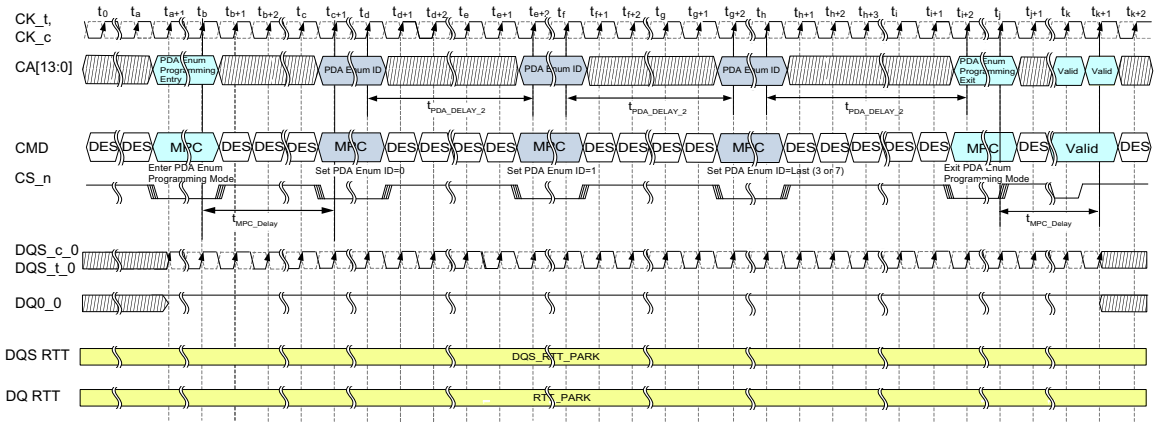
4.16.1.2 Timing Diagram of PDA Enumerate Programming with Resulting “Don’t Enumerate” (cont’d)



NOTES:

1. The figure assumes Multi-Cycle MPC commands, so the timings are adjusted to visually show separation between timings such as tMPC_DELAY (which start at the end of a command cycle and end at the beginning of the next) and other timings such as tPDA_DELAY_1.
2. The diagram above assumes preamble/postamble requirements for DQS (including 1 rising edge and 1 falling edge for the 2 tCK and 3 tCK preambles or 2 rising edges and 2 falling edges for the 4 tCK preamble).

Figure 90 — Multi Device PDA Enumerate Programming “Don’t Enumerate” Case in Legacy Mode

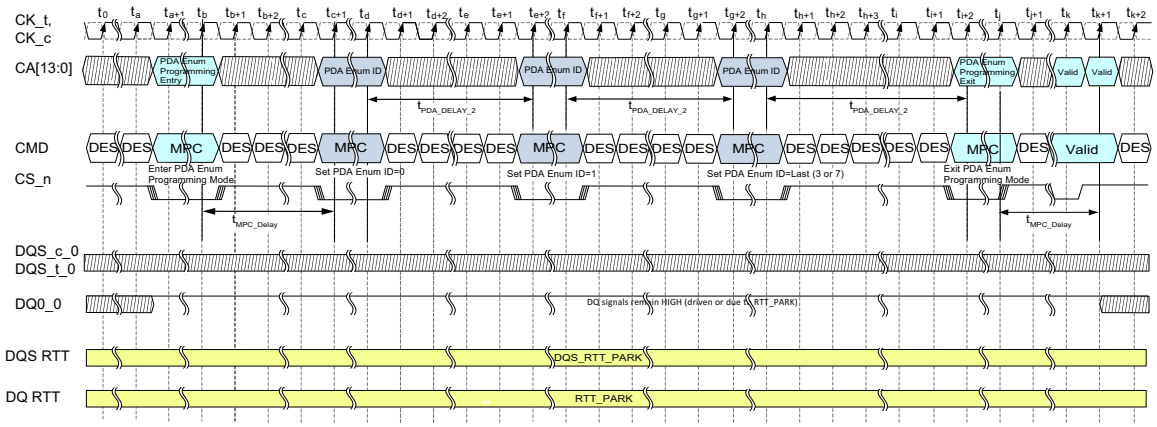


NOTES:

1. The figure assumes Multi-Cycle MPC commands, so the timings are adjusted to visually show separation between timings such as tMPC_DELAY (which start at the end of a command cycle and end at the beginning of the next) and other timings such as tPDA_DELAY_2.

Figure 91 — Multi Device PDA Enumerate Programming “Don’t Enumerate” Case in Continuous DQS Toggle Mode

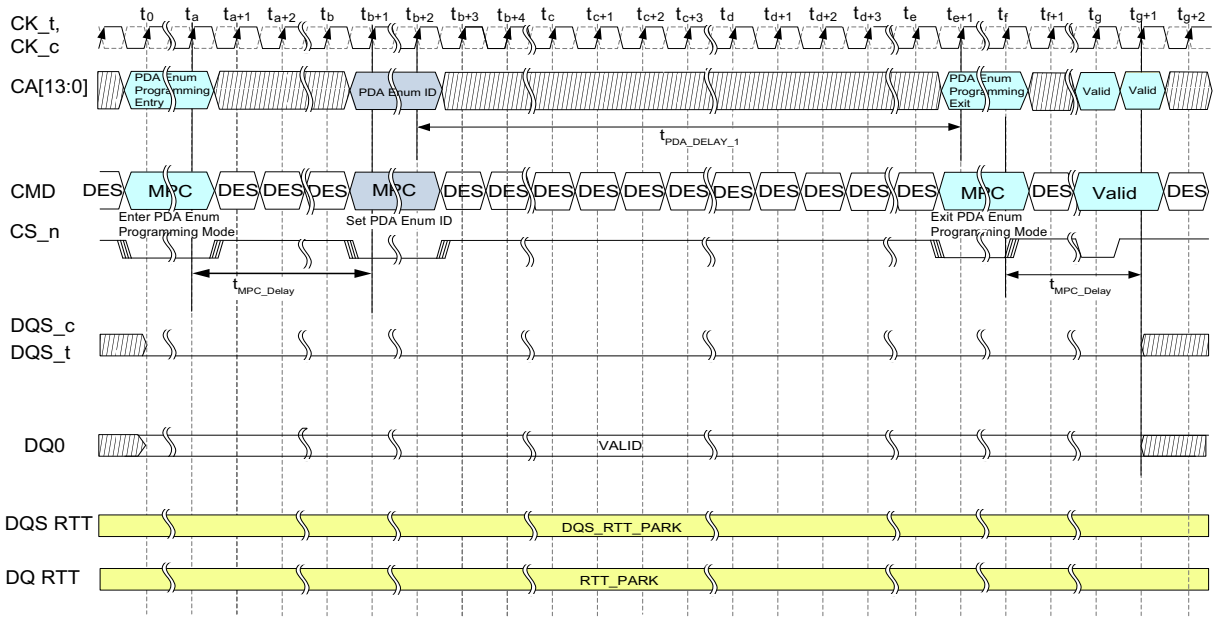
4.16.1.2 Timing Diagram of PDA Enumerate Programming with Resulting “Don’t Enumerate” (cont’d)



NOTES:

1. The figure assumes Multi-Cycle MPC commands, so the timings are adjusted to visually show separation between timings such as tMPC_DELAY (which start at the end of a command cycle and end at the beginning of the next) and other timings such as tPDA_DELAY_2.

Figure 92 — Multi Device PDA Enumerate Programming “Don’t Enumerate” Case for DQ Held HIGH and any DQS State



NOTES:

1. The figure assumes Multi-Cycle MPC commands, so the timings are adjusted to visually show separation between timings such as tMPC_DELAY (which start at the end of a command cycle and end at the beginning of the next) and other timings such as tPDA_DELAY_1.
2. DQ0 shall not transition during VALID state.

Figure 93 — Multi Device PDA Enumerate Programming “Don’t Enumerate” Case for VALID DQ and Differentially Low DQS

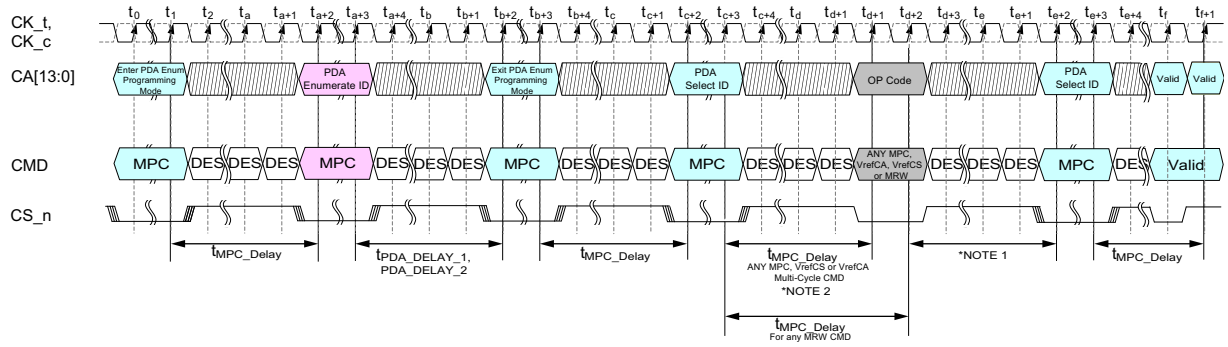
4.16.2 PDA Select ID Operation

Once the PDA Enumerate ID's have been programmed in all the DRAMs, the execution of future MPC/MRW/VrefCA/VrefCS commands depend on the value of the PDA Select ID and the type of MPC command. If the PDA Select ID is set to 1111_B, all DRAMs will execute the command. For all MRW, VrefCA, and VrefCS commands, and some of the MPC commands (RTT_CA/CS/CK and RTT_PARK opcodes), the PDA Select ID will be compared to the PDA Enumerate ID to determine if the DRAM will execute the commands. For all other MPC commands (i.e. not the RTT_CA/CS/CK and RTT_PARK opcodes), the DRAM will execute the command regardless of the PDA Select ID value.

As an example, the following sequence could be used to program unique MR fields per device:

1. Send MPC with 'PDA Select ID' opcode, with encoding 0000 included in the opcode
2. Send MRW's for field settings specific to Device 0000. this can be any number of MRW's
3. Send MPC with 'PDA Select ID' opcode, with encoding 0001 included in the opcode
4. Send MRW's for field settings specific to Device 0001. this can be any number of MRW's
5. Repeat for any number of devices
6. Send MPC with 'PDA Select ID' opcode, with encoding 1111 included in the opcode to enable all DRAMs to execute all MRW, VrefCA, VrefCS, and MPC commands.

The timing diagram in Figure 94 shows an example sequencing of the programming of the PDA Select ID and MPC, VrefCA, VrefCS, or MRW commands.



NOTES:

1. Commands used such as MPC, VREFCA, VREFCS, or MRW have different command spacing requirements. Please refer to those specific sections in the document for details.
2. ANY Multi-Cycle MPC, VREFCA, or VREFCS command spacing is measured from the last valid command cycle to the first following valid command cycle, while standard command spacing goes from last valid command cycle to last valid command cycle. See MRW command period diagrams for details.

Figure 94 — Timing Diagram Showing Multi-Cycle MPC Command Sequencing with PDA Enumerate and PDA Select ID

4.16.2 PDA Select ID Operation (cont'd)

Table 90 summarizes the electrical parameters associated with PDA Enumerate Programming Mode:

Table 90 — PDA Parametric Timings DDR5-3200 to DDR5-3600

Parameter	Symbol	DDR5-3200		DDR5-3600		Units	Note
		Min	Max	Min	Max		
PDA Enumerate ID Command to any other command cycle time	tPDA_DELAY_1	tPDA_DQS_DELAY (max)+ BL/2+19ns	-	tPDA_DQS_DELAY (max)+BL/2+19ns	-	nCK,ns	
PDA Enumerate ID Command to any other command cycle time for Multi-Device Continuous DQS Toggle Mode	tPDA_DELAY_2	tPDA_DELAY_1+t MPC_ Delay(min)	-	tPDA_DELAY_1+ tMPC_Delay(min)	-	nCK,ns	
Delay to rising strobe edge used for sampling DQ during PDA operation	tPDA_DQS_DELAY	5	18	5	18	ns	1
Delay to falling DQ edge during PDA operation	tPDA_DQ_DELAY_1	tPDA_DQS_DELAY (min)- tPDA_S_FALL(min)	tPDA_DQS_DELAY (max)- tPDA_S_FALL(min)	tPDA_DQS_DELAY (min)- tPDA_S_FALL(min)	tPDA_DQS_DELAY (max)- tPDA_S_FALL(min)	ns	
Delay to rising DQ edge during PDA operation	tPDA_DQ_DELAY_2	tPDA_DELAY_1(mi n)	-	tPDA_DELAY_1(mi n)	-	nCK, ns	
Delay after last DQS toggle used for sampling DQ during PDA	tPDA_DQS_STOP	tMPC_DELAY(min) + tPDA_H_RISE(min)	-	tMPC_DELAY(min) + tPDA_H_RISE(min)	-	nCK,ns	
Delay after last DQ toggle used for sampling DQ during PDA	tPDA_DQ_STOP	tMPC_DELAY(min)	-	tMPC_DELAY(min)	-	nCK,ns	
Falling DQ Edge Setup Time during PDA operation	tPDA_S_FALL	max(3nCK, 1.875ns)	-	max(3nCK, 1.666ns)	-	nCK,ns	
Rising DQ Edge Hold Time during PDA operation	tPDA_H_RISE	max(3nCK, 1.875ns)	-	max(3nCK, 1.666ns)	-	nCK,ns	
Rising DQ Edge Setup Time during PDA operation	tPDA_S_RISE	tMPC_DELAY(min)	-	tMPC_DELAY(min)	-	nCK,ns	
Falling DQ Edge Hold Time during PDA operation	tPDA_H_FALL	tMPC_DELAY(min)	-	tMPC_DELAY(min)	-	nCK,ns	

4.16.2 PDA Select ID Operation (cont'd)

Table 91 — PDA Parametric Timings DDR5-4000 to DDR5-4400

Parameter	Symbol	DDR5-4000		DDR5-4400		Units	Note
		Min	Max	Min	Max		
PDA Enumerate ID Command to any other command cycle time	tPDA_DELAY_1	tPDA_DQS_DELAY(max)+BL/2+19ns	-	tPDA_DQS_DELAY (max)+BL/2+19ns	-	nCK,ns	
PDA Enumerate ID Command to any other command cycle time for Multi-Device Continuous DQS Toggle Mode	tPDA_DELAY_2	tPDA_DELAY_1+ tMPC_Delay(min)	-	tPDA_DELAY_1+ tMPC_Delay(min)	-	nCK,ns	
Delay to rising strobe edge used for sampling DQ during PDA operation	tPDA_DQS_DELAY	5	18	5	18	ns	1
Delay to falling DQ edge during PDA operation	tPDA_DQ_DELAY_1	tPDA_DQS_DELAY (min)- tPDA_S_FALL(min)	tPDA_DQS_DELAY (max)- tPDA_S_FALL(min)	tPDA_DQS_DELAY (min)- tPDA_S_FALL(min)	tPDA_DQS_DELAY (max)- tPDA_S_FALL(min)	ns	
Delay to rising DQ edge during PDA operation	tPDA_DQ_DELAY_2	tPDA_DELAY_1(min)	-	tPDA_DELAY_1(min)	-	nCK, ns	
Delay after last DQS toggle used for sampling DQ during PDA	tPDA_DQS_STOP	tMPC_DELAY(min)+ tPDA_H_RISE(min)	-	tMPC_DELAY(min) + tPDA_H_RISE(min)	-	nCK,ns	
Delay after last DQ toggle used for sampling DQ during PDA	tPDA_DQ_STOP	tMPC_DELAY(min)	-	tMPC_DELAY(min)	-	nCK,ns	
Falling DQ Edge Setup Time during PDA operation	tPDA_S_FALL	max(3nCK, 1.500ns)	-	max(3nCK, 1.363ns)	-	nCK,ns	
Rising DQ Edge Hold Time during PDA operation	tPDA_H_RISE	max(3nCK, 1.500ns)	-	max(3nCK, 1.363ns)	-	nCK,ns	
Rising DQ Edge Setup Time during PDA operation	tPDA_S_RISE	tMPC_DELAY(min)	-	tMPC_DELAY(min)	-	nCK,ns	
Falling DQ Edge Hold Time during PDA operation	tPDA_H_FALL	tMPC_DELAY(min)	-	tMPC_DELAY(min)	-	nCK,ns	

4.16.2 PDA Select ID Operation (cont'd)

Table 92 — PDA Parametric Timings DDR5-4800 to DDR5-9200

Parameter	Symbol	DDR5-4800 to 9200		Units	Notes
		Min	Max		
PDA Enumerate ID Command to any other command cycle time	tPDA_DELAY_1	tPDA_DQS_DELAY(max)+BL/2+19ns	-	nCK,ns	
PDA Enumerate ID Command to any other command cycle time for Multi-Device Continuous DQS Toggle Mode	tPDA_DELAY_2	tPDA_DELAY_1+ tMPC_Delay(min)	-	nCK,ns	
Delay to rising strobe edge used for sampling DQ during PDA operation	tPDA_DQS_DELAY	5	18	ns	1
Delay to falling DQ edge during PDA operation	tPDA_DQ_DELAY_1	tPDA_DQS_DELAY (min)-tPDA_S_FALL(min)	tPDA_DQS_DELAY (max)-tPDA_S_FALL(min)	ns	
Delay to rising DQ edge during PDA operation	tPDA_DQ_DELAY_2	tPDA_DELAY_1(min)	-	nCK, ns	
Delay after last DQS toggle used for sampling DQ during PDA	tPDA_DQS_STOP	tMPC_DELAY(min)+ tPDA_H_RISE(min)	-	nCK,ns	
Delay after last DQ toggle used for sampling DQ during PDA	tPDA_DQ_STOP	tMPC_DELAY(min)	-	nCK,ns	
Falling DQ Edge Setup Time during PDA operation	tPDA_S_FALL	max(3nCK, 1.250ns)	-	nCK,ns	
Rising DQ Edge Hold Time during PDA operation	tPDA_H_RISE	max(3nCK, 1.250ns)	-	nCK,ns	
Rising DQ Edge Setup Time during PDA operation	tPDA_S_RISE	tMPC_DELAY(min)	-	nCK,ns	
Falling DQ Edge Hold Time during PDA operation	tPDA_H_FALL	tMPC_DELAY(min)	-	nCK,ns	

NOTE 1 tPDA DQS_DELAY specifies when the beginning of a minimum of one complete BL16 set of consecutive strobe edges (8 rising edges and 8 falling edges, plus 1 rising edge and 1 falling edge for the 2tCK and 3tCK preambles or 2 rising edges and 2 falling edges for the 4tCK preamble) shall be sent by the host controller after the associated MPC.

4.17 Read Training Pattern

4.17.1 Introduction

Training of the Memory Interface requires the ability to read a known pattern from the DRAM, prior to enabling writes into the DRAM. Due to the increased frequencies supported by DDR5, a simple repeating pattern will not be sufficient for read training. A Linear-Feedback Shift Register (LFSR) for a pattern generator will also be required. The Read Training Pattern is accessed when the host issues an MRR command to the MR31 address, and CRC must be disabled prior to issue this command. In this case, the returned data will be a pattern instead of the contents of a mode register. The timing of the read data return is the same as for an MRR or Read command, including the operation of the strobes (DQSL_t, DQSL_c, DQSU_t, DQSU_c). The Read Training Pattern is a full BL16 pattern for each MRR command issued to the Read Training Pattern address, regardless of the MR0 Burst Length setting. No ACT command shall be issued prior to the completion of the BL16 data output. The DRAM shall also support non-target ODT.

An alternate continuous burst mode is available and is configured with MRW to MR25:OP[3]=1. Once this mode is configured, an MRR to MR31 on the target DRAM will start the pattern output and will automatically continue to output the appropriate pattern until it is stopped by either a system reset or issuing an MRW to MR25:OP[3]=0 command that reverts it to the “MRR command based (Default)” mode as shown in Figure 98. An MRR to MR31 and an MRW to set MR25:OP[3}=0 are the only commands allowed after entering Read Training Continuous Burst Mode. Issuing any MRR other than to MR31 is invalid and may result in unexpected DQ behavior, requiring the host to issue a Reset to exit Continuous Burst mode and restart the training with an MRR to MR31. Data output is a repeated BL16 pattern, regardless of the MR0 Burst Length setting. Once the MR25:OP[3]=0 “MRR command based (Default)” is registered by the DRAM, it will stop all pattern traffic by tCont_Exit. Since there is no min time for tCont_Exit, the DRAM may stop the pattern prior to tCont_Exit, potentially truncating any current burst pattern. To ensure that the DRAM’s state-machine doesn’t get into some meta-stability while turning off the output pattern, the host shall issue a second MRW with MR25:OP[3]=0 after waiting a minimum of ttMRW but less than a maximum of tCBME after the first MRW command with MR25:OP[3]=0, which will then start tCont_Exit_delay. After tCont_Exit_delay has expired, any other valid command is then legal. No ACT commands shall be issued prior to the completion Read Training Continuous Burst Mode. All Read Training Patterns (modes) are supported in continuous burst mode. The host shall disable Read CRC, if enabled, prior to using continuous burst mode.

While in Read Training Pattern Continuous Burst Mode, the DRAM will set the ODT to DQS_RTT_OFF and RTT_OFF for DQS and DQ, respectively, for the duration of the continuous burst mode output. However, if a non-target rank is intended to provide termination for the duration of the continuous burst mode output on the target rank, the nontarget rank will only terminate the DQ ODT to RTT_NOM_RD (MR35:OP[5:3]) during the BL16 associated with the MRR NT command. Therefore, the host is responsible to ensure that RTT_PARK (MR34:OP[2:0] is programmed to align with RTT_NOM_RD (MR35:OP[5:3]), if so desired.

Upon exiting of Read Training Pattern Continuous Burst Mode, all RTT_PARK settings of the non-target rank needs programmed for normal operation if previously changed to align with RTT_NOM_RD.

Prior to utilizing either read training pattern mode (Continuous Burst Output mode or MRR Command Based mode), the initial seed value will need to be programmed in MR26-MR30 else the power on default values will be used.

The default value for the **Read Pattern Data0/LFSR0** (MR26) register setting is: 0x5A and the default value for the **Read Pattern Data1/LFSR1 (MR27)** register setting is: 0x3C. The **Read Pattern Invert** (MR28, MR29) register settings default to 0. The **Read LFSR Assignments** (MR30) register setting default is 0xFE.

The DRAM will not store the current LFSR state when exiting the Continuous Burst Output Mode and may clear the pattern values stored in MR26-MR30, therefore any subsequent pattern reads will require the host to reprogram the seed, pattern, inversion and LFSR assignments in MR26-MR30.

The Read Training Pattern has 2 primary supported modes of operation. One of the modes is referred to as the serial format. The second mode is LFSR mode. The LFSR mode is required due to the higher frequency bus operation for DDR5. There is a secondary mode associated with the LFSR mode, which enables the generation of a simple high frequency clock pattern instead of the LFSR pattern.

Table 93 — Read Training Pattern Address

MR Address	Operating Mode	Description
MR31	Read Training Pattern	This MR address is reserved. There are no specific register fields associated with this address. In response to the MRR to this address the DRAM will send the BL16 read training pattern. All 8 bits associated with this MR address are reserved.

4.17.1 Introduction (cont'd)

Table 94 shows the MR field and encodings for the Read Training Pattern format settings.

Table 94 — Read Training Mode Settings

MR Address	Operating Mode	Description
MR25 OP[0]	Read Training Pattern Format	0B: Serial 1B: LFSR
MR25 OP[1]	LFSR0 Pattern Option	0B: LFSR 1B: Clock
MR25 OP[2]	LFSR1 Pattern Option	0B: LFSR 1B: Clock
MR25 OP[3]	Continuous Burst Mode	0B: MRR command based (Default) 1B: Continuous Burst Output

The default value for the **Read Training Pattern Format** register setting is: 0x0.

For Serial Read Training Pattern Format mode, the following Mode Registers are programmed with the data pattern. There are two 8-bit registers to provide a 16 UI pattern length and two 8-bit registers to provide up to x16 data width for per-DQ-lane inversion.

The LFSR mode requires an 8-bit Mode Register to program the seed for the 8-bit LFSR. The details of the LFSR polynomial and outputs are explained in the following section. The **Read Pattern Data0/LFSR0** and **Read Pattern Data1/LFSR1** registers are repurposed to program the LFSR seed when the **Read Training Pattern Format** is set to LFSR.

Table 95 — Read Pattern Data0 / LFSR0

MR Address	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR26	D7	D6	D5	D4	D3	D2	D1	D0

The default value for the **Read Pattern Data0/LFSR0** register setting is: 0x5A.

Table 96 — Read Pattern Data1 / LFSR1

MR Address	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR27	D15	D14	D13	D12	D11	D10	D9	D8

The default value for the **Read Pattern Data1/LFSR1** register setting is: 0x3C.

The values for the **Read Pattern Data0/LFSR0** and **Read Pattern Data1/LFSR1** registers may be restored to the default values under the following conditions:

- Self Refresh
- Power-down entry
- Exiting Continuous Burst Output Mode

If any of the above conditions occur, the Host will need to reprogram the contents of MR26 and MR27, prior to utilizing either read training pattern mode (Continuous Burst Output mode or MRR Command Based mode).

In both cases, when the **Read Training Pattern Format** is set to Serial mode or LFSR mode, the **Read Pattern Invert - Lower DQ Bits** and **Read Pattern Invert - Upper DQ Bits** settings will additionally invert the pattern, per DQ bit. The **Read Pattern Invert - Lower DQ Bits** register will apply to x4, x8, and x16 devices. The **Read Pattern Invert - Upper DQ Bits** register only applies to x16 devices, for the upper byte.

Table 97 — Read Pattern Invert - Lower DQ Bits

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR28	DQ Invert	DQL7	DQL6	DQL5	DQL4	DQL3	DQL2	DQL1	DQL0

The default value for the **Read Pattern Invert - Lower DQ Bits** register setting is: 0x00.

Table 98 — Read Pattern Invert - Upper DQ Bits

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR29	DQ Invert	DQU7	DQU6	DQU5	DQU4	DQU3	DQU2	DQU1	DQU0

The default value for the **Read Pattern Invert - Upper DQ Bits** register setting is: 0x00.

4.17.1 Introduction (cont'd)

The values for both **Read Pattern Invert - Lower and Upper DQ Bit** registers may be restored to the default values under the following conditions:

- Self Refresh
- Power-down entry
- Exiting Continuous Burst Output Mode

If any of the above conditions occur, the Host will need to reprogram the contents of MR28 and MR29 if non-default values are desired, prior to utilizing either read training pattern mode (Continuous Burst Output mode or MRR Command Based mode).

A value of 0 in any bit location of the **Read Pattern Invert - Lower DQ Bits** or **Read Pattern Invert - Upper DQ Bits** registers will leave the pattern un-inverted for the associated DQ. A value of 1 in any bit location of the **Read Pattern Invert - Lower DQ Bits** or **Read Pattern Invert - Upper DQ Bits** registers will invert the pattern for the associated DQ.

4.17.2 LFSR Pattern Generation

The LFSR is an 8-bit Galois LFSR. The polynomial for the Galois LFSR is $x^8+x^6+x^5+x^4+1$. Figure 95 shows the logic to implement the LFSR. The numbered locations within the shift register show the mapping of the seed/state positions within the register. There are two instances of the same LFSR polynomial. These two instances will have unique seeds/states and supply patterns to any of the DQ outputs.

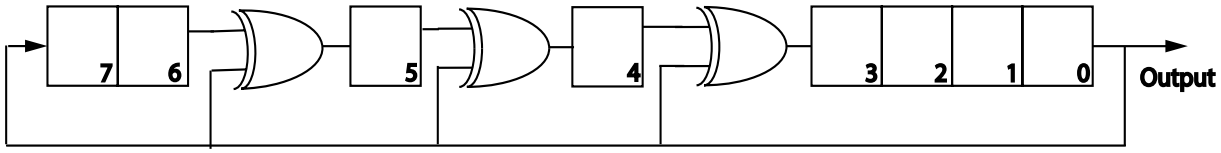


Figure 95 — Read Training Pattern LFSR

The seed location in the figure clarifies the mapping for the **Read Pattern Data0/LFRS0** and **Read Pattern Data1/LFSR1** mode registers relative to the LFSR logic. The LFSR output is directed to any number of the DQ outputs, depending on the LFSR assignment programming. These assignments between LFSR0 and LFSR1 to each DQ output will create a unique pattern sequence for better coverage of DQ to DQ crosstalk interactions. The LFSR assignments are programmed according to Table 99:

Table 99 — Read LFSR Assignments

MR Address	MRW OP	LFSR Assignment	MR Setting
MR30	OP0	DQL0/DQU0	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**
	OP1	DQL1/DQU1	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**
	OP2	DQL2/DQU2	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**
	OP3	DQL3/DQU3	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**
	OP4	DQL4/DQU4	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**
	OP5	DQL5/DQU5	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**
	OP6	DQL6/DQU6	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**
	OP7	DQL7/DQU7	**0B:** Read Pattern Data0/**LFSR0** **1B:** Read Pattern Data1/**LFSR1**

The default value for the **Read LFSR Assignments** register setting is: 0xFE.

4.17.2 LFSR Pattern Generation (cont'd)

The values for the **Read LFSR Assignments** register may be restored to the default values under the following conditions:

- Self Refresh
- Power-down entry
- Exiting Continuous Burst Output Mode

If any of the above conditions occur, the Host will need to reprogram the contents of MR30 if non-default values are desired, prior to utilizing either read training pattern mode (Continuous Burst Output mode or MRR Command Based mode).

The LFSR output will change at the UI frequency, producing a new output value on every UI. The LFSR will only change state to support the read data after the MRR to the specific (MR31) Read Training Pattern address. When there are no MRR accesses to the (MR31) Read Training Pattern address, the LFSR will retain its previous state (from the end of the previous Read Training Pattern MRR access completion). Therefore, the full state space of the LFSR may be traversed through a series of 16 MRR commands, each of which accesses 16 UI's of LFSR output. The BL for the LFSR data will always be BL16. The state of the LFSR can also be changed by sending a new MRW command to reset the LFSR0 and LFSR1 seed mode registers (MR26 and MR27) or through the reset conditions listed for those registers. A setting of 0x00 in either of the LFSR seed registers (MR26 and MR27) will not produce a pattern with any transitions to 1. When set to this value the LFSR will produce a constant 0 pattern.

When the **LFSR0 Pattern Option** MR25:OP[1] is set to 1, the pattern that is supplied by the DRAM is a high frequency clock pattern, instead of the LFSR. This clock pattern is sent only to the DQ signals that have a setting of 0 in the corresponding DQ Opcode location in the **Read LFSR Assignments register**. The first UI of the pattern will have a value of 0. The second UI will have a value of 1, and this will continue to toggle for each subsequent UI.

When the **LFSR1 Pattern Option** MR25:OP[2] is set to 1, the pattern that is supplied by the DRAM is a high frequency clock pattern, instead of the LFSR. This clock pattern is sent only to the DQ signals that have a setting of 1 in the corresponding DQ Opcode location in the **Read LFSR Assignments register**. The first UI of the pattern will have a value of 0. The second UI will have a value of 1, and this will continue to toggle for each subsequent UI.

The state of the LFSR will not change when an MRR to MR31 occurs if the associated **LFSR Pattern Option** is set to 1 in MR25[1] for LFSR0 or MR25[2] for LFSR1, designating the clock pattern. The state of both LFSR0 and LFSR1 will also not change when an MRR to MR31 occurs if the serial mode is selected by setting MR25[0] = 0. The **Read LFSR Assignments** settings have no impact on whether or not the LFSR state progresses with each MRR to MR31. Only the **Read Training Pattern Format** and **LFSR Pattern Option** settings determine whether the LFSR is actively computing next states.

4.17.3 Read Training Pattern Examples

Table 100 shows the bit sequence of the Read Training Pattern, for the following programming:

Read Training Pattern Format = 0 (Serial)
LFSR0 Pattern Option = 0 (These are don't cares when in Serial Read Training Pattern Format)
LFSR1 Pattern Option = 0 (These are don't cares when in Serial Read Training Pattern Format)
Read Pattern Data0/LFSR0 = 0x1C
Read Pattern Data1/LFSR1 = 0x59
Read Pattern Invert - Lower DQ Bits = 0x55
Read Pattern Invert - Upper DQ Bits = 0x55

Table 100 — Serial Bit Sequence Example

Pin	Invert	Bit Sequence															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQL0	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL1	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQL2	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL3	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQL4	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL5	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQL6	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL7	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU0	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU1	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU2	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU3	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU4	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU5	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU6	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU7	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0

4.17.3 Read Training Pattern Examples (cont'd)

Table 101 shows the bit sequence of the Read Training Pattern, for the following programming:

Read Training Pattern Format = 1 (LFSR)
LFSR0 Pattern Option = 0
LFSR1 Pattern Option = 0
Read Pattern Data0/LFSR0 = 0x5A
Read Pattern Data1/LFSR1 = 0x3C
Read LFSR Assignments = 0xFE
Read Pattern Invert - Lower DQ Bits = 0x00
Read Pattern Invert - Upper DQ Bits = 0xFF

Table 101 — LFSR Bit Sequence Example

Pin	Invert	LFSR	Bit Sequence															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQL0	0 (No)	0	0	0	1	1	0	0	0	0	0	0	1	1	1	0	1	0
DQL1	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL2	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL3	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL4	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL5	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL6	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL7	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQU0	1 (Yes)	0	1	1	0	0	1	1	1	1	1	1	0	0	0	1	0	1
DQU1	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU2	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU3	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU4	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU5	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU6	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU7	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1

4.17.3 Read Training Pattern Examples (cont'd)

Table 102 shows the bit sequence of the Read Training Pattern, for the following programming:

Read Training Pattern Format = 1 (LFSR)
LFSR0 Pattern Option = 0
LFSR1 Pattern Option = 1 (Clock Pattern Option)
Read Pattern Data0/LFSR0 = 0x00 (When the LFSR seed is set to 0, this produces a constant 0 pattern)
Read Pattern Data1/LFSR1 = 0x3C (This value is a don't care when LFSR1 Pattern Option = 1)
Read LFSR Assignments = 0x04
Read Pattern Invert - Lower DQ Bits = 0xFB
Read Pattern Invert - Upper DQ Bits = 0xFB

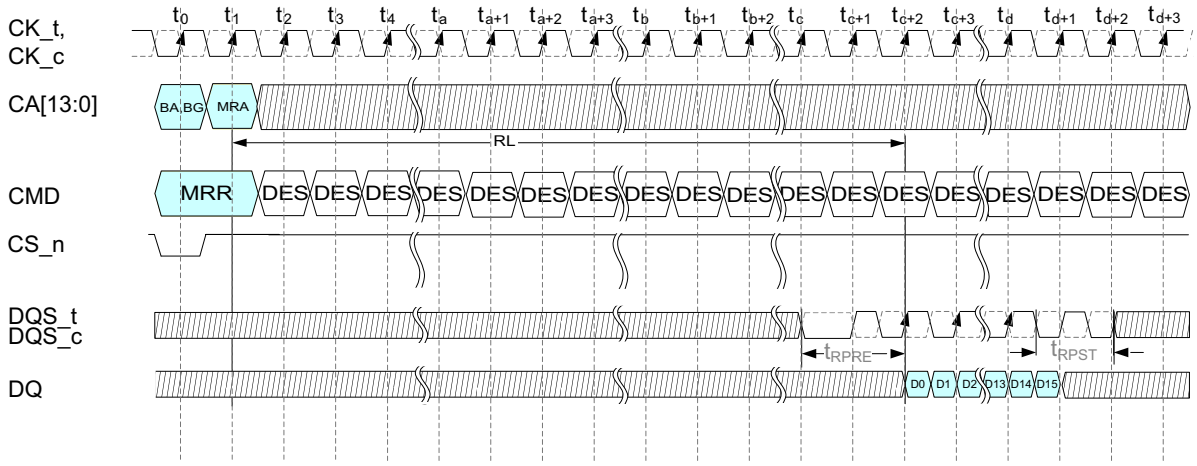
Table 102 — LFSR Bit Sequence Example

Pin	Invert	LFSR	Bit Sequence															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQL0	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL1	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL2	0 (No)	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
DQL3	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL4	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL5	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL6	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL7	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU0	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU1	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU2	0 (No)	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
DQU3	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU4	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU5	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU6	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU7	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

4.17.4 Read Training Pattern Timing Diagrams

The timing of the data return and strobe sequence should match that of a Read operation. The timing of the Read Training Pattern will be similar to the MRR operation, with the exception that the MRR to the address that invokes the Read Training Pattern will be a full BL16 pattern. The timing between MRR commands to access the Read Training Pattern is defined as tMRR_p, which supports back to back data patterns. This is faster than a normal MRR to MRR condition which is defined as tMRR.

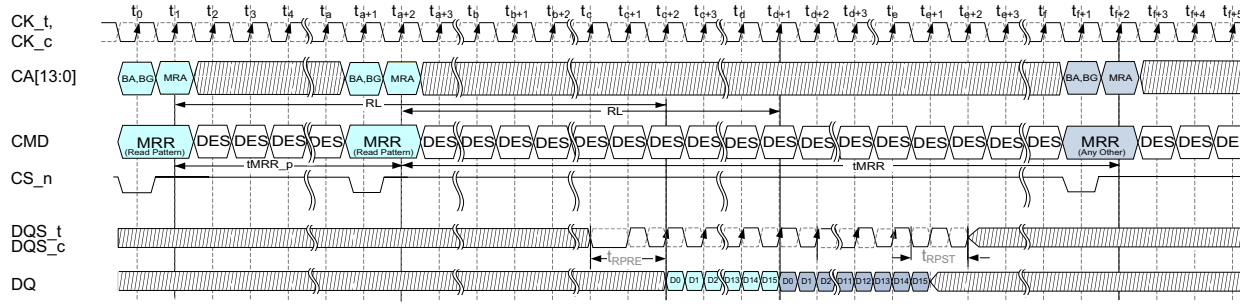
The timing diagram in Figure 96 shows the general timing sequence for an MRR that accesses the Read Training Pattern:



NOTE The Read Training Pattern shall align to the DDR5 preamble timings.

Figure 96 — Timing Diagram for Read Training Pattern

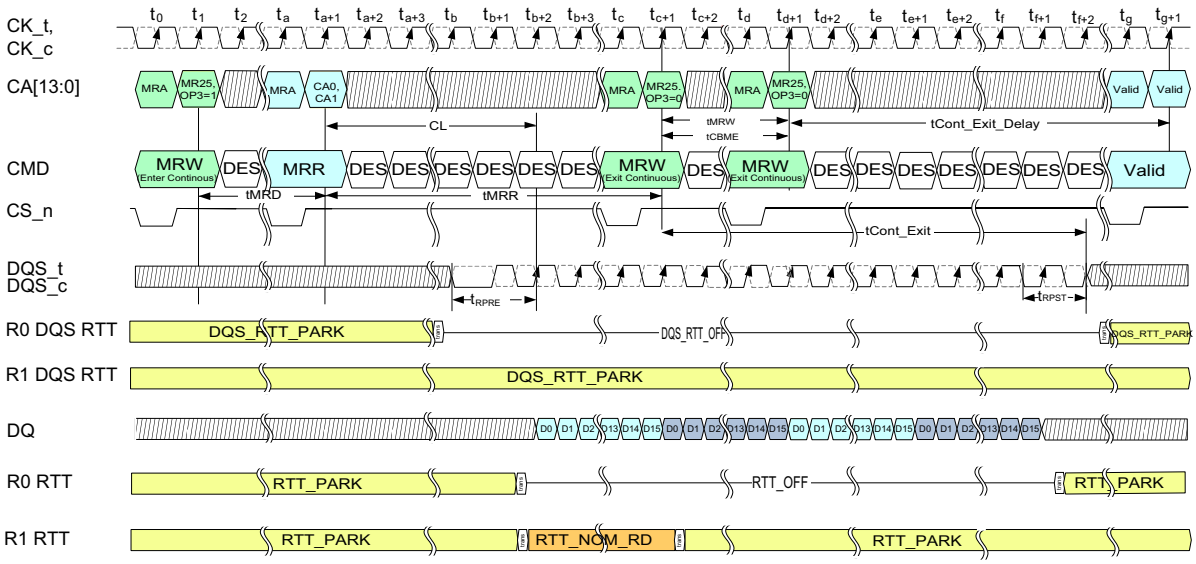
The Read Training Pattern must also support back to back traffic, for any number of MRR commands sequenced every 8 tCK. The timing diagram in Figure 97 shows a back to back pattern example:



NOTE The Read Training Pattern shall align to the DDR5 preamble timings.

Figure 97 — Timing Diagram for Back to Back Read Training Patterns

4.17.4 Read Training Pattern Timing Diagrams (cont'd)



NOTE 1 The Read Training Pattern shall align to the DDR5 preamble timings and will exit after the MRW (Continuous Exit encoding) has been received and but before tCont_Exit has expired. During tCont_Exit, the data output may not follow the read pattern data.

NOTE 2 Host responsible for proper setting of RTT_PARK of the non-target rank is programmed to align with RTT_NOM_RD, if desired

Figure 98 — Timing Diagram for Continuous Burst Mode Read Training Patterns

Table 103 — Timing Parameters for Read Training Patterns

Parameter	Symbol	Min	Max	Units	Notes
Registration of MRW Continuous Burst Mode Exit to next valid command delay	tCont_Exit_Delay	tCont_Exit+tMRD	-	-	
Registration of MRW Continuous Burst Mode Exit to end of training mode	tCont_Exit	-	RL+BL/2+10nCK	-	
Maximum delay between first exit continuous burst mode MRW command and the second exit continuous burst mode MRW command	tCBME	-	CL-10nCK		

4.18 Read Preamble Training Mode

4.18.1 Introduction

Read preamble training supports read leveling of the host receiver timings. This mode supports MRR transactions that access the Read Training Pattern, and cannot be used during any other data transactions. Just like Read Training Pattern, Read Preamble Training needs to be entered with CRC disabled. Read preamble training changes the read strobe behavior such that the strobes are always driven by the DRAM, and only toggle during a 1tCK preamble plus the actual burst of the read data. There is no toggle during postamble time. This mode enables the host to detect the timing of when the first data and associated strobe is returned after a read command.

4.18.2 Entry and Exit for Preamble Training Mode

The DRAM enters Read Preamble Training Mode by setting MR2:OP[0] = 1. Read Preamble Training Mode is exited by setting MR2:OP[0] = 0. Read Preamble Training should not be disturbed by an ACT command until the completion of the training.

Table 104 — MR2 Register Information - for Reference only - See Mode Register Section for Details

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Internal Write Timing	RFU	Device 15 MPSM	CS Assertion Duration (MPC)	Max Power Saving Mode (MPSM)	2N Mode	Write Leveling Training	Read Preamble Training

Function	Register Type	Operand	Data	Notes
Read Preamble Training	R/W	OP[0]	0B: Normal Mode (Default) 1B: Read Preamble Training	

4.18.3 Preamble Training Mode Operation

Once the DRAM is placed in Read Preamble Training Mode, the only data transactions supported are MRR commands. Other data transactions and some non-data transactions are not allowed during Read Preamble Training Mode. Commands allowed or not allowed are as follows:

1. Allowed while in Preamble Training Mode: MPC functions allowed when current state is “Active”, MRW, MRR, REFab, REFsb, RFMab, RFMsb, NOP
2. Not allowed while in Preamble Training Mode: MPC functions only allowed when current state is “All Banks Idle”, ACT, WRP, WRPA, WR, WRA, RD, RDA, VrefCA, VrefCS, PREab, PREsb, PREpb, SRE, SREF, PDE, PDX

Once READ Preamble Training is enabled, the device will drive DQS_t LOW and DQS_c HIGH within tSDOn and remain at these levels until an MRR command is issued.

During read preamble training, a 1 tCK preamble will be used instead of the programmed DQS preamble setting. Once the MRR command is issued, the device will drive DQS_t/DQS_c after CL-tRPRE (where tRPRE=1CK), like a normal READ burst with the Read DQS Offset setting programmed in MR40 applied. In response to the MRR to the designated Read Training Pattern Address, the device must also drive the DQ pattern as per the Read Pattern configuration while in this mode. The MRR commands may be sequenced to enable back to back bursts on the DQ bus.

Read preamble training mode is exited within tSDOff after setting MR2:OP[0].

The following figure shows the timing for the strobe driven differential low after Read Preamble Training Mode is enabled, and also shows the strobe timings including a 1tCK Preamble, after an MRR command to access the Read Training Pattern:

4.18.3 Preamble Training Mode Operation (cont'd)

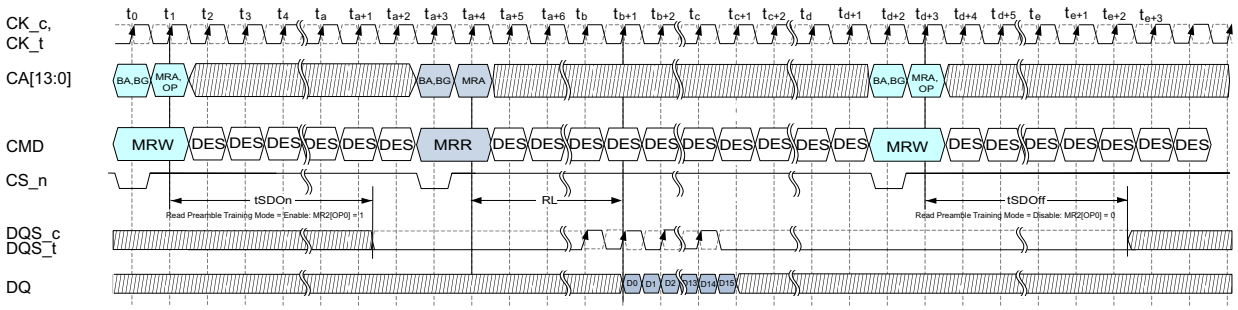


Figure 99 — Timing Diagram for Read Preamble Training Mode Entry, Read Training Pattern Access, and Read Preamble Training Mode Exit

Table 105 — Timing parameters for Preamble Training Mode

Parameter	Symbol	Min	Max
Delay from MRW Command to DQS Driven	tSDOn	-	Max(12nCK, 20ns)
Delay from MRW Command to DQS Disabled	tSDOff	-	Max(12nCK, 20ns)

4.19 CA Training Mode (CATM)

4.19.1 Introduction

The CA Training Mode is a method to facilitate the loopback of a logical combination of the sampled CA[13:0] signals. In this mode, the CK is running, and the CS_n qualifies when the CK samples the CA signals. A loopback equation that includes all the CA signals results in an output value that is sent asynchronously on the DQ signals back to the host memory controller. The host timings between CS_n, CK, and CA[13:0] signals can then be optimized for proper alignment. When the DRAM is in this mode, no functional commands are executed in the DRAM. The functional command interface is restored only after exiting this mode, which requires a CS_n assertion of two or more consecutive tCK. Prior to entering the CA Training Mode, the CS_n signal must be aligned to the CK to meet the CS_n to CK timing specifications. This assumes that CS Training has been completed to determine the correct CS_n timings on the host, so the timing window for the CS to be met to ensure enought setup or hold timing margin prior to entering Command/Address training mode. Chip select training, through CSTM, can be used to accomplish this.

4.19.2 Entry and Exit for CA Training Mode

The CA Training Mode is enabled through an MPC command, with the opcode designated for CA Training Mode Entry**.** Once this MPC command has executed no other commands will be interpreted by the DRAM. Only the sampling of the CA signals, evaluation of the XOR result, and loop back to the DQ's will occur. While in CA Training Mode, the CS_n signal will only assert for a single tCK at a time. The maximum sampling rate on the CA signals will be every 4tCK.

When the CA Training Mode has completed successfully, the CA Training Mode is disabled by asserting CS_n for 2 or more cycles in a row, while sending a NOP command on the CA bus.

4.19.3 CA Training Mode (CATM) Operation

In CA Training Mode, the CA values are sampled in the same way as for functional operation, where the CS_n qualifies which cycle the sampling occurs, and the sample is captured by the rising CK edge. Unlike functional operation, there is no concept of multiple cycle commands in CA Training Mode. Sampling of the CA signals ONLY occurs when CS_n is asserted. Once the CA signals are sampled, the values are XOR'd to produce an output value. This output value is driven on all the DQ pins, as a pseudo-static value. These output values will be held until the next sample is captured on the CA bus, according to the CS_n assertion.

During CA Training Mode the CA ODT is enabled as for functional operation. The VrefCA is Group According to the functional setting. The timing requirements for the CA bus, CK_t, CK_c, and CS_n are the same as for functional operation.

The delay from when the CA signals are sampled during the CS_n assertion and when the output of the XOR computation is driven on the DQ pins is specified as t_{CATM_Valid}, as shown in the following figure. CS_n shall be asserted every 4tCK or with greater than 4tCK separation between assertions, and thus the CA XOR output shall transition every 4tCK or greater. The following figure demonstrates an example where two CS_n assertions occur with a separation of 4tCK. The DRAM will exit CA Training Mode when the CS_n is asserted for 2 or more consecutive cycles but limited to 8 cycles.

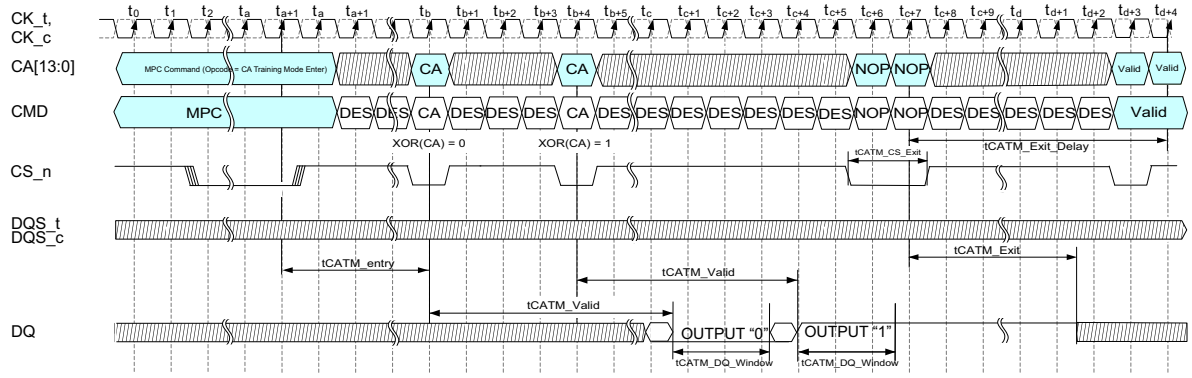


Figure 100 — Timing Diagram for CA Training Mode

4.19.3 CA Training Mode (CATM) Operation (cont'd)

Table 106 — AC Parameters for CA Training Mode

Symbol	Description	Min	Max	Unit	Note
tCATM_Entry	Registration of CATM entry command to start of training samples time	20	-	ns	
tCATM_Exit	Registration of CATM exit CS_n assertion to end of training mode. This is when DQ is no longer driven by the DRAM	-	14	ns	
tCATM_Exit_Delay	Registration of CATM exit to next valid command delay	20	-	ns	
tCATM_Valid	Time from sample evaluation to output on DQ bus	-	20	ns	
tCATM_DQ_Window	Time output is available on DQ Bus	2	-	nCK	1
tCATM_CS_Exit	CS_n assertion duration to exit CATM	2	8	nCK	

NOTE 1 This timing parameter is applied to each DQ independently, not all-DQs valid window perspective.

4.19.3.1 CA Loopback Equations

The CATM Output is computed based on the CS_n assertion and the values of the CA inputs. The following table clarifies the output computation.

Table 107 — CA Training Mode Output

CS_n	CATM Output
0	XOR(CA[13:0]) [1]
1	Hold previous value

NOTE 1 The XOR function occurs after mirroring/inversion recovery, and only includes signals supported on the DRAM, i.e., may not include CA[13], depending on density (including stacking). If CA[13] is not needed for the DRAM's density, the logical value shall be considered 0 for the XOR computation, though as indicated in the pin description table for MIR, the ball location associated with CA13's logical input (which switches with CA12) shall be connected to VDDQ.

4.19.3.2 Output Equations

Table 108 shows which signals will transmit the output of the CA Training Mode loopback equation. These values are driven asynchronously as pseudo-static values, updating with a new output at a time t_{CATM_Valid} after each CS_n assertion.

Table 108 — Output Equations per Interface Width

Output	X16	X8	X4
DQ0	CATM Output	CATM Output	CATM Output
DQ1	CATM Output	CATM Output	CATM Output
DQ2	CATM Output	CATM Output	CATM Output
DQ3	CATM Output	CATM Output	CATM Output
DQ4	CATM Output	CATM Output	
DQ5	CATM Output	CATM Output	
DQ6	CATM Output	CATM Output	
DQ7	CATM Output	CATM Output	
DML			
TDQS_c			
DQSL_t			
DQSL_c			
DQ8	CATM Output		
DQ9	CATM Output		
DQ10	CATM Output		
DQ11	CATM Output		
DQ12	CATM Output		
DQ13	CATM Output		
DQ14	CATM Output		
DQ15	CATM Output		
DMU			
DQSU_t			
DQSU_c			

4.20 CS Training Mode (CSTM)

4.20.1 Introduction

The CS Training Mode is a method to facilitate the loopback of a sampled sequence of the CS_n signal. In this mode, the CK is running, and the CA signals are held in a NOP command encoding state. Once this mode is enabled and the DRAM devices are selected to actively sample and drive feedback, The DRAM will sample the CS_n signal on the rising edge of CK. Every set of four CK rising edge samples will be included in a logical computation to determine the CSTM Output result that is sent back to the host on the DQ bus. Once sampling begins, the DRAM must maintain the consecutive grouping of the samples every 4 tCK. When the CS_n Sample[0] and Sample[2] results in a logic 0 and the CS_n Sample[1] and Sample[3] results in a logic 1, the DRAM will drive a 0 on all the DQ signals. There is no requirement to drive any strobes, and the output signal could transition as often as every 4 tCK.

4.20.2 Entry and Exit for CS Training Mode

The CS Training Mode is enabled when the host sends an MPC command with the opcode for CS Training Mode Entry. Since CS Training shall occur prior to establishing alignment between CK and CS_n signals, the MPC command extends beyond multiple tCK cycles, during which the CS_n signal is asserted. When the DRAM is in this mode, commands are still actively processed. The only commands that should be sent by the host memory controller while CS Training Mode is enabled are the NOP command and the MPC to exit CS Training Mode. Any other command may produce unreliable results. Once the DRAM has CS Training Mode enabled, the DRAM begins sampling on every rising CK edge, with the 4-sample groups looping consecutively. Depending on the value of the samples, the DQ signals are driven high or low. Prior to entering CS Training Mode, the DQ signals are not driven by the DRAM and are terminated according to the default RTT_PARK setting. After CS Training Mode is enabled, the DQ signal will begin driving the output values based on the CS Training Mode samples. Once the DQ signals are driven by the DRAM, RTT_PARK termination will no longer be applied, similar to a READ operation.

To exit CS Training Mode, an MPC command shall be sent to disable CS Training Mode. Even though the timing relationship between CS_n and CK is understood when exiting CS Training Mode, the host is required to send a Multi-Cycle CS_n assertion during the MPC command or a single tCK assertion while MR2:OP[4]=0_B.

4.20.3 CS Training Mode (CSTM) Operation

In CS Training Mode, the CS_n values are sampled on all CK rising edges. Each group of 4 consecutive samples is evaluated in pairs, and then the two pairs are combined with a logical OR prior to sending to the DQ output. The samples evaluation to determine the output is as follows:

Table 109 — Sample Evaluation for Intermediate Output[0]

Output[0]	CS_n Sample[0]	CS_n Sample[1]
1	0	0
0	0	1
1	1	0
1	1	1

Table 110 — Sample Evaluation for Intermediate Output[1]

Output[1]	CS_n Sample[2]	CS_n Sample[3]
1	0	0
0	0	1
1	1	0
1	1	1

Table 111 — Sample Evaluation for Final CSTM Output

CSTM Output [1]	Output[0]	Output[1]
0	0	0
1	0	1
1	1	0
1	1	1

NOTE 1 When there is no change on the CSTM Output from previous evaluation, DQ shall continue to drive same value continuously with no switching on the bus.

4.20.3 CS Training Mode (CSTM) Operation (cont'd)

During CS Training Mode the CA ODT is enabled as for functional operation. The VrefCA is Group According to the functional setting (through the VrefCA Command).

The delay from when the CS_n signals are sampled during the fourth CK rising edge (Sample[3]) to when the output of the sample evaluation is driven to a stable value on the DQ pins is specified as tCSTM_Valid, as shown in Figure 101. The details of the tCSTM_entry, tCSTM_exit, and tCSTM_DQ_Window are also illustrated.

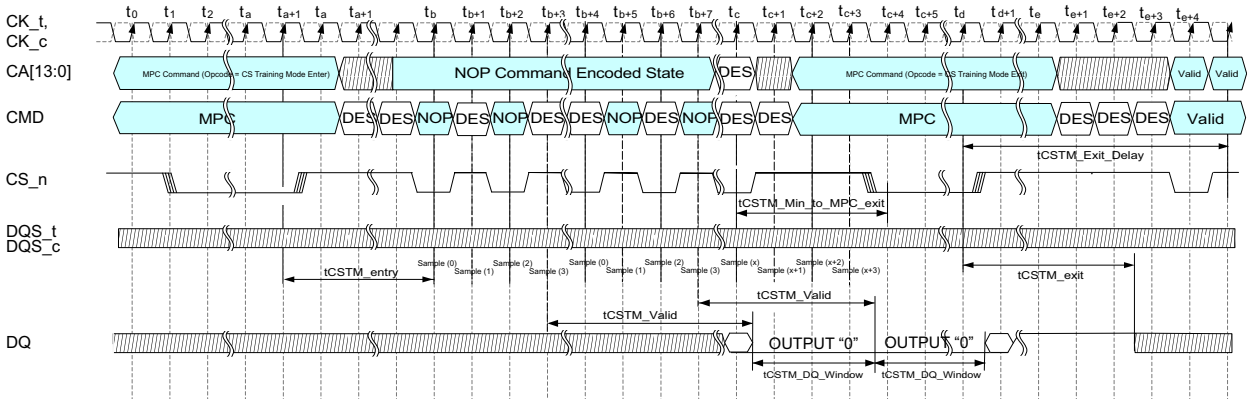
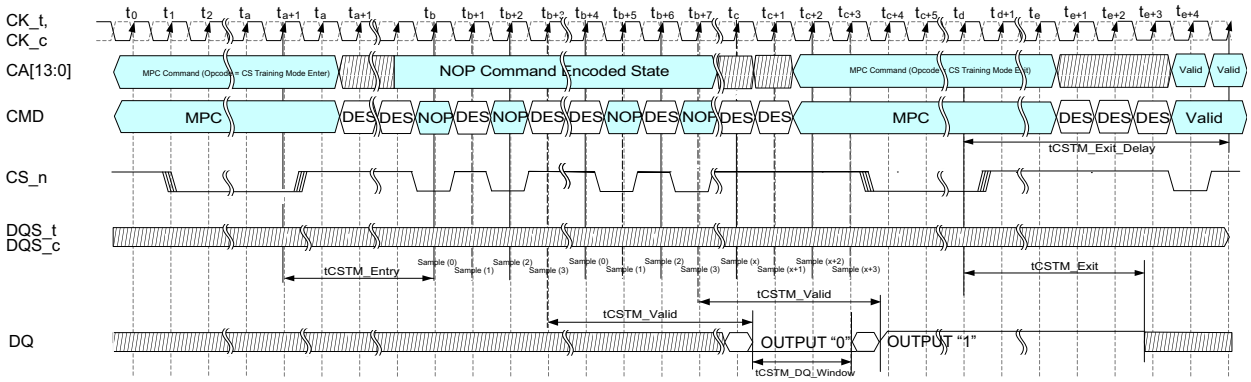


Figure 101 — Timing Diagram for CS Training Mode with Consecutive Output Samples = 0

Figure 102 illustrates an example where the DQ Output switches from a logic 0 to a logic 1 value, demonstrating the minimum tCSTM_DQ_Window:



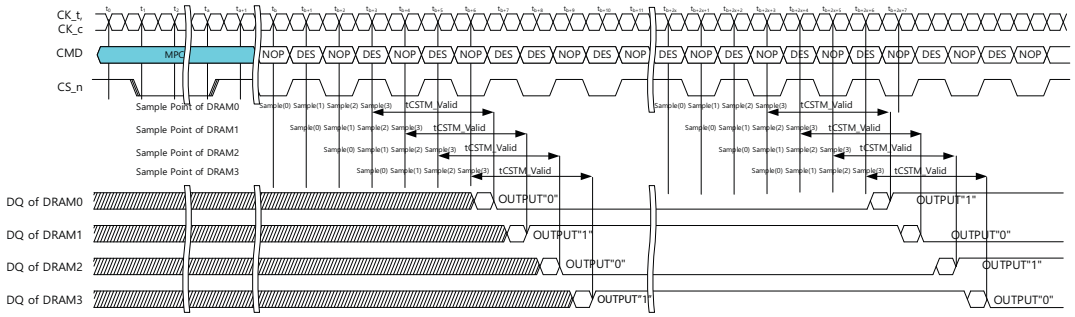
NOTE 1 See MPC Command for details on Setup, Hold and command register time.

NOTE 2 The CA bus must meet setup and hold times on any clock where it is possible that CS_n might be sampled low while in CS training mode.

Figure 102 — Timing Diagram for CS Training Mode with Output Sample Toggle

4.20.3 CS Training Mode (CSTM) Operation (cont'd)

When host trains CS_n timing for DDR5 by using CSTM, CS_n sampling timing for each DRAM could be different from each other because the variation of internal timing is different for each DRAM. Therefore, even though the CS setup/hold time is appropriate for each DRAM, 4-tCK CS_n sampling window which may have different starting points could appear differently as shown in Figure 103. Host should train CS_n timing based on asserting every edge of CS_n to cover multiple DRAMs without exiting CSTM.



Note 1 See MPC Command for details on Setup, Hold and command register time.

Figure 103 — Timing Diagram for CS Training Mode with Multiple DRAMs Output Sample Toggle

Table 112 — AC Parameters for CS Training Mode

Symbol	Description	Min	Max	Unit	Note
tCSTM_Entry	Registration of CSTM entry command to start of training samples time	20	-	ns	
tCSTM_Min_to_MPC_exit	Min time between last CS_n pulse and first pulse of MPC Command to exit CSTM	4	-	nCK	
tCSTM_Exit	Registration of CSTM exit command to end of training mode	-	20	ns	
tCSTM_Valid	Time from sample evaluation to output on DQ bus	-	20	ns	
tCSTM_DQ_Window	Time output is available on DQ Bus	2	-	nCK	1
tCSTM_Exit_Delay	Registration of CATM exit to next valid command delay	20	-	ns	

NOTE 1 This timing parameter is applied to each DQ independently, not all-DQs valid window perspective.

4.20.3.1 Output Signals

Table 113 shows which signals will transmit the output of the CS Training Mode loopback sample evaluation. These values are driven asynchronously, but may switch as often as every 4tCK.

Table 113 — CS Sampled Output per Interface Width

Output	X16	X8	X4
DQ0	CSTM Output	CSTM Output	CSTM Output
DQ1	CSTM Output	CSTM Output	CSTM Output
DQ2	CSTM Output	CSTM Output	CSTM Output
DQ3	CSTM Output	CSTM Output	CSTM Output
DQ4	CSTM Output	CSTM Output	
DQ5	CSTM Output	CSTM Output	
DQ6	CSTM Output	CSTM Output	
DQ7	CSTM Output	CSTM Output	
DML			
TDQS_c			
DQSL_t			
DQSL_c			
DQ8	CSTM Output		
DQ9	CSTM Output		
DQ10	CSTM Output		
DQ11	CSTM Output		
DQ12	CSTM Output		
DQ13	CSTM Output		
DQ14	CSTM Output		
DQ15	CSTM Output		
DMU			
DQSU_t			
DQSU_c			

4.21 Write Leveling Training Mode

4.21.1 Introduction

The DDR5 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the memory controller to set the timings of the WRITE DQS signaling according to the Write Latency timing specification at the DRAM. Therefore, the DDR5 SDRAM supports a 'write leveling' feature to allow the controller to compensate for channel skew. The DDR5 Write Leveling Training also allows for an unmatched path between CK and DQS within the DRAM, and thus supports an internal Write Leveling Training flow to account for the difference in internal delays.

The DDR5 DRAM also provides a programmable timing in its write logic, controlled by the Write Leveling Internal Cycle Alignment (WICA) mode register (MR3), which provides a means for improved performance of the device's receiver. The proper setting of this register shall be determined by the memory controller, either as described in the sections below, or by some other means. This delay setting is specific to each DRAM, its Write Preamble setting, and the operating frequency being used. PDA select ID is allowed while in WL training mode to program settings specific to each DRAM. Once the proper setting has been determined for a given WICA byte, Write preamble setting, and operating frequency, that setting may be subsequently restored to the DRAM after reset, power-cycle, or return to a previously used operating frequency.

The memory controller can use the 'write leveling' feature and feedback from the DDR5 DRAM to adjust the controller's differential DQS (DQS_t - DQS_c) output delay to align to the phase and cycle that corresponds to the CAS Write Latency (CWL) delay after the WRITE command. The memory controller involved in the leveling must have an adjustable delay setting on the DQS pins to align the rising edge of differential DQS with the timing at the receiver that is the pin-level Write Latency (External Write Leveling Training), and to align DQS with the internal DRAM Write Latency timing point (Write Leveling Internal Cycle Alignment). The internal DRAM Write Latency timing point may be skewed from the pin-level Write Latency timing point. The host will minimize this skew (tDQSoffset) through the Write Leveling Training flow.

Since the system and DIMM delays vary, the DRAM will support the ability for the host to align the DQS timings with a pin-level Write Latency differential CK (CK_t-CK_c) edge. This alignment is referred to as External Write Leveling. Once the DQS host timings are aligned at the DRAM Write Latency timing, the internal DRAM timings are optimized for lowest power and internal delay. This is accomplished when the host enables the Internal Write Timing setting in MR2. In order to compensate for the difference in delay, the host will execute an Internal Write Leveling Training sequence, which includes sweeping the Write Leveling Internal Cycle Alignment (WICA) settings in MR3 (Write Leveling Internal Cycle Alignment Operation) and then finalizing the differential DQS phase and offset (Write Leveling Internal Phase Alignment and Final Host DQS Timing Operation).

During Write Leveling Training (both External and Internal), the DQS pattern shall include the full programmed write preamble and only the first toggle of the normal data burst sequence. The DRAM will sample the Internal Write Leveling Pulse relative to the first DQS toggle of the data burst sequence (last rising differential DQS edge sent by the host) and asynchronously feed back the result of this sample on the DQ bus, transitioning between tWLOmin and tWLOmax. If the DQ bus output is LOW at tWLOmax, the Internal Write Leveling Pulse signal was sampled while it was deasserted (LOW). Likewise, if the DQ bus output is HIGH at tWLOmax, the Internal Write Leveling Pulse signal was sampled while it was asserted (HIGH). The sampled feedback state will remain on the DQ bus until a subsequent Write Leveling sample changes the state, or until Write Leveling Training is exited.

The Internal Write Leveling Pulse is generated in response to a WRITE command, and held statically low otherwise. To perform the Write Leveling training, the controller repeatedly sends a WRITE command, delays DQS, and monitors the DQ feedback after tWLOmax until a transition from 0 to 1 is detected, indicating alignment with the Internal Write Leveling Pulse.

During Internal Write Leveling Training flows, the host will apply an offset to the starting point or the final setting of the DQS-signals. The offsets are referred to as WL_ADJ_start and WL_ADJ_end. This will minimize the tDQSoffset variation across different DRAM devices. The WL_ADJ_start and WL_ADJ_end values depend on the tWPRE setting.

When External and Internal Write Leveling Training flows are complete and the final WL_ADJ_end offset has been applied to the DQS timings, the DQS is phase aligned and cycle aligned for write operations. During the training sequence the DRAM in Write Leveling training mode will apply ODT to the strobes in the same way as for functional operation. All non-target ranks (which will not be in Write Leveling Training Mode) will apply ODT as defined for functional operation. Prior to executing the DDR5 Write Leveling Training Flow, the DRAM tWPRE value must be configured to the functional operation setting.

Note: DQS ODT is based on a DQS PARK Mode and is not enabled and disabled with DQ ODT timings.

4.21.2 Write Leveling Mode Registers

The MR fields for Write Leveling Training, Internal Write Timing, and Write Leveling Internal Cycle Alignment are part of MR2 and MR3 (optionally MR7 as well). To enter Write Leveling Training Mode, the controller shall program MR2:OP[1]=1. Likewise, to exit Write Leveling Training Mode, the controller will program MR2:OP[1]=0. Write Leveling Internal eCycle aAlignment offers two nibbles to control the upper and lower DQ bytes. The lower byte WL internal Cycle alignment is intended for x4, x8 and x16 configurations, while the upper byte is only for x16 configurations.The Internal Write Timing, once enabled (MR2:OP[7]=1), shall remain enabled through the Internal Write Leveling Training flow and for functional operation. The host is responsible for incrementing the Write Leveling Internal Cycle Alignment setting until the Internal Write Leveling Pulse is pulled early enough to align with the differential DQS signal that was previously aligned with the pin-level Write Latency timing. The Write Leveling Internal Cycle Alignment setting only applies when the Internal Write Timing is enabled.

Only BL16 Mode is supported in Write Leveling Training Mode. DM and TDQS shall be disabled by the host (if previously enabled) by setting MR5:OP[5]=0 and MR5:OP[4]=0, respectively, prior to executing Write Leveling Training Mode.

4.21.3 External Write Leveling Training Operation

When Write Leveling Mode is enabled (MR2:OP[1]=1) and the Internal Write Timing is disabled (MR2:OP[7]=0), the DRAM will have an Internal Write Leveling pulse that indicates how the DQS signals shall be aligned to match the pin-level Write Latency timings. The rising edge of the Internal Write Leveling Pulse will align to the rising edge of the differential CK signal that coincides with CAS Write Latency (CWL), as shown in the following diagrams.

The differential DQS signals driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits shall carry the leveling feedback to the controller across the DRAM configurations x4, x8, and x16. On a x16 device, both byte lanes shall be leveled independently. Therefore, a separate feedback mechanism shall be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS) to Internal Write Leveling Pulse relationship whereas the lower data bits would indicate the lower diff_DQS(diff_LDQS) to Internal Write Leveling Pulse relationship. When training a x16 device, the data bits of a byte will remain in the “don’t care” state until its applicable DQS signals are toggled. Once the DQS signals are toggled, the DQs will follow the behavior previously described.

The following diagram shows the timing sequence to enter Write Leveling Training Mode, operation during Write Leveling Training Mode (with Internal Write Timings disabled), and the timing sequence to exit Write Leveling Training mode. An MRW command is sent to enable Write Leveling Training Mode. Prior to sending the MRW command to enable Write Leveling Training Mode, the host memory controller must drive the DQS signals differentially low. After tWLPEN time, the controller can send a WRITE command, followed by strobe pulses. The DQS signals shall always drive differentially low, except during the WRITE preamble and burst strobe sequence . There is no restriction as to how early the strobe pulses are sent, so long as they are no earlier than CWL/2 after the WRITE command. The DRAM will sample the Internal Write Leveling Pulse relative to the first DQS toggle of the data burst sequence and asynchronously feed back the result of this sample on the DQ bus, transitioning between tWLOmin and tWLOmax.

While in Write Leveling Training mode, the host controller may send ACT and PRE commands. The DRAM will ignore these commands. The address associated with the ACT and the WRITE commands may be any value. The following timing diagrams demonstrate the timing requirements associated with Write Leveling Training Mode Entry, the Internal Write Leveling Pulse alignment during External Write Leveling Training, and the DQ sample feedback timing.

4.21.3 External Write Leveling Training Operation (cont'd)

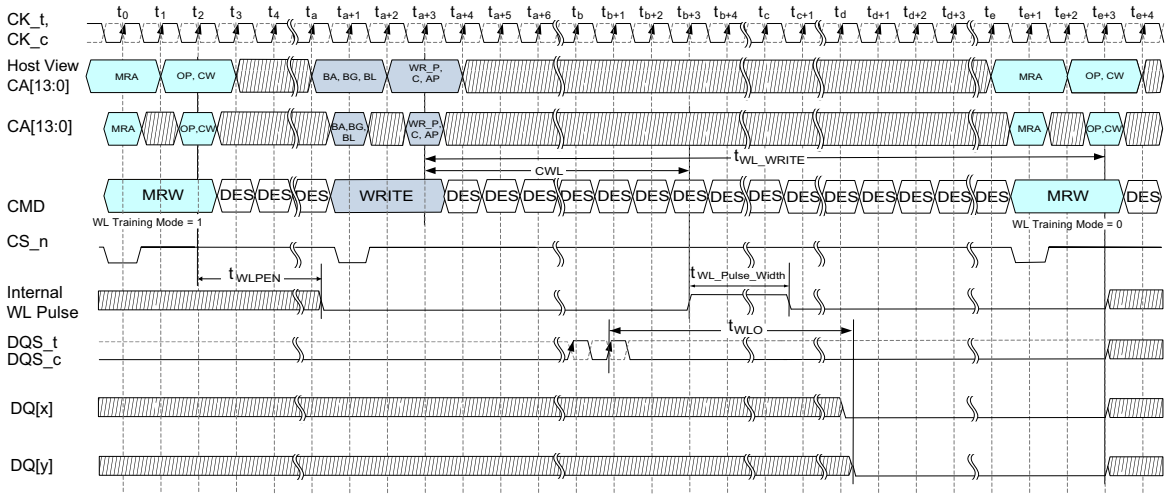


Figure 104 — Write Leveling Training Mode Timing Diagram (External Training, 2N Mode, 0 Sample)

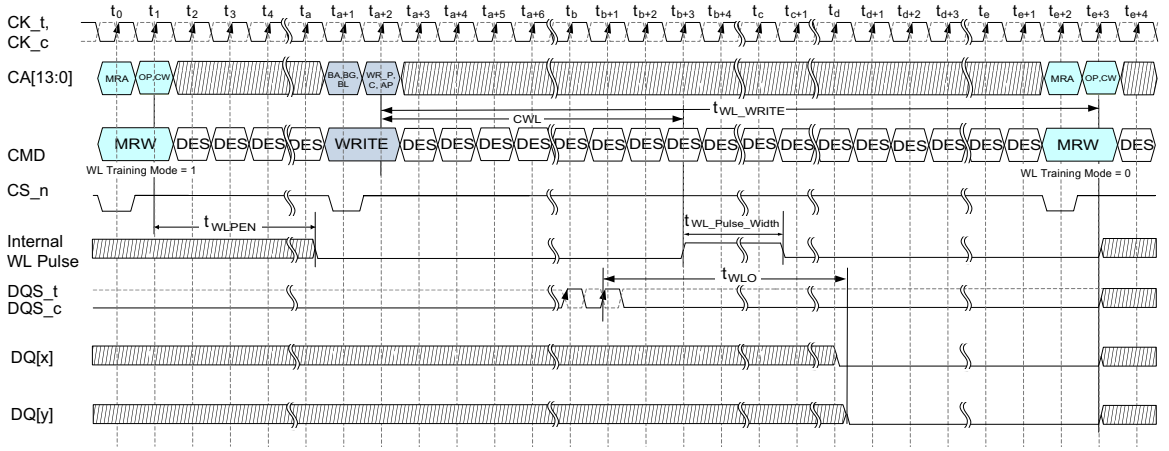


Figure 105 — Write Leveling Training Mode Timing Diagram (External Training, 1N Mode, 0 Sample)

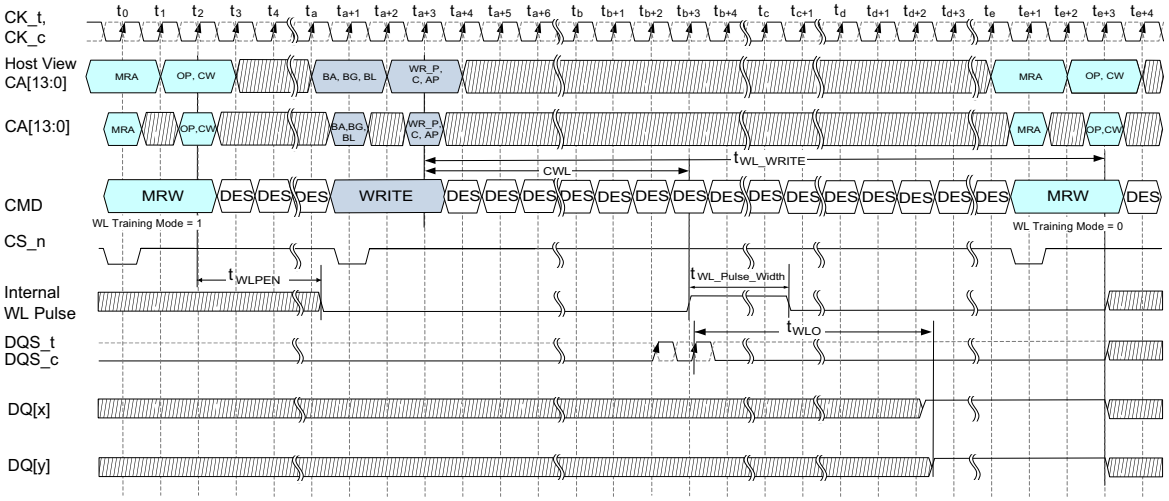


Figure 106 — Write Leveling Training Mode Timing Diagram (External Training, 2N Mode, 1 Sample)

4.21.3 External Write Leveling Training Operation (cont'd)

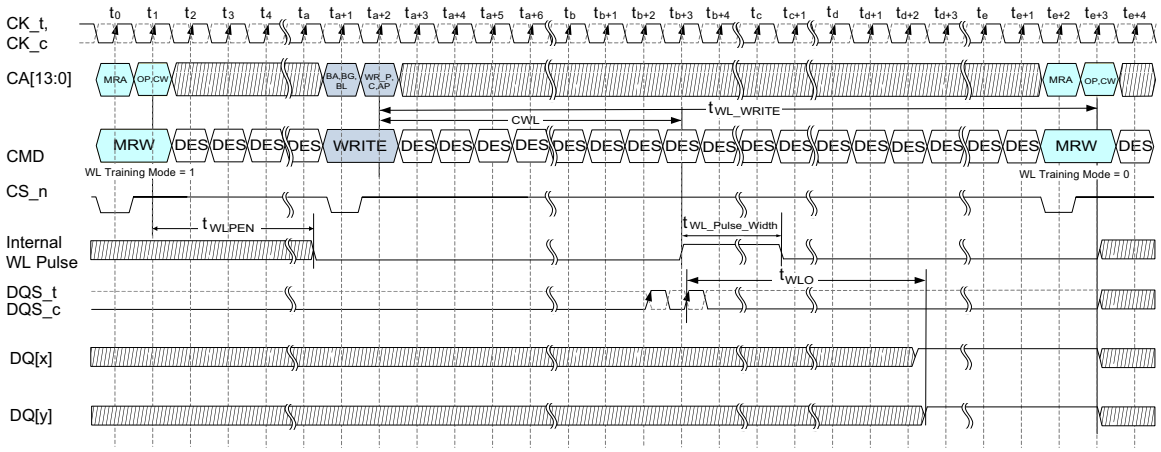


Figure 107 — Write Leveling Training Mode Timing Diagram (External Training, 1N Mode, 1 Sample)

The Memory controller initiates Write Leveling mode of all DRAMs in a rank by setting MR2:OP[1]=1. When entering write leveling mode, the DQ pins are in undefined driving mode. Since the controller levels one rank at a time, all non-target ranks will set Write Leveling Mode to disabled. The Controller may assert non-target ODT through the normal WRITE command protocol. DQS_RTT_PARK termination will apply to the DQS_t and DQS_c signals.

The Controller shall drive DQS differentially LOW prior to sending the MRW command to enable Write Leveling Training Mode. The WRITE command must occur after a delay of tWLPEN relative to when the MRW enabled Write Leveling Training Mode.

The DRAM will sample the Internal Write Leveling Pulse and asynchronously feed back the result of this sample on the DQ bus, transitioning between tWLOmin and tWLOmax. The controller can sample the state of any DQ bit after tWLOmax. Based on the sampled state, the controller decides to increment or decrement the DQS delay setting and launches the next WRITE command with associated DQS_t/DQS_c pulse (or pulse sequence) after some time, which is controller dependent. Once a 0 to 1 transition on the DQ bus is detected, the controller locks DQS delay setting and external write leveling is achieved for the device.

Write Leveling Training may be executed by issuing consecutive Write commands after entering Write Leveling Mode has been enabled (no requirement to exit and reenter between each Write command). The minimum Write to Write command spacing during Write Leveling Mode is tWL_Write and is defined as "max(CWL, last DQS differential toggle) + tWLO(max)+ 2nCK". An example of consecutive Write commands given during Write Leveling Training is shown in Figure 108:

4.21.3 External Write Leveling Training Operation (cont'd)

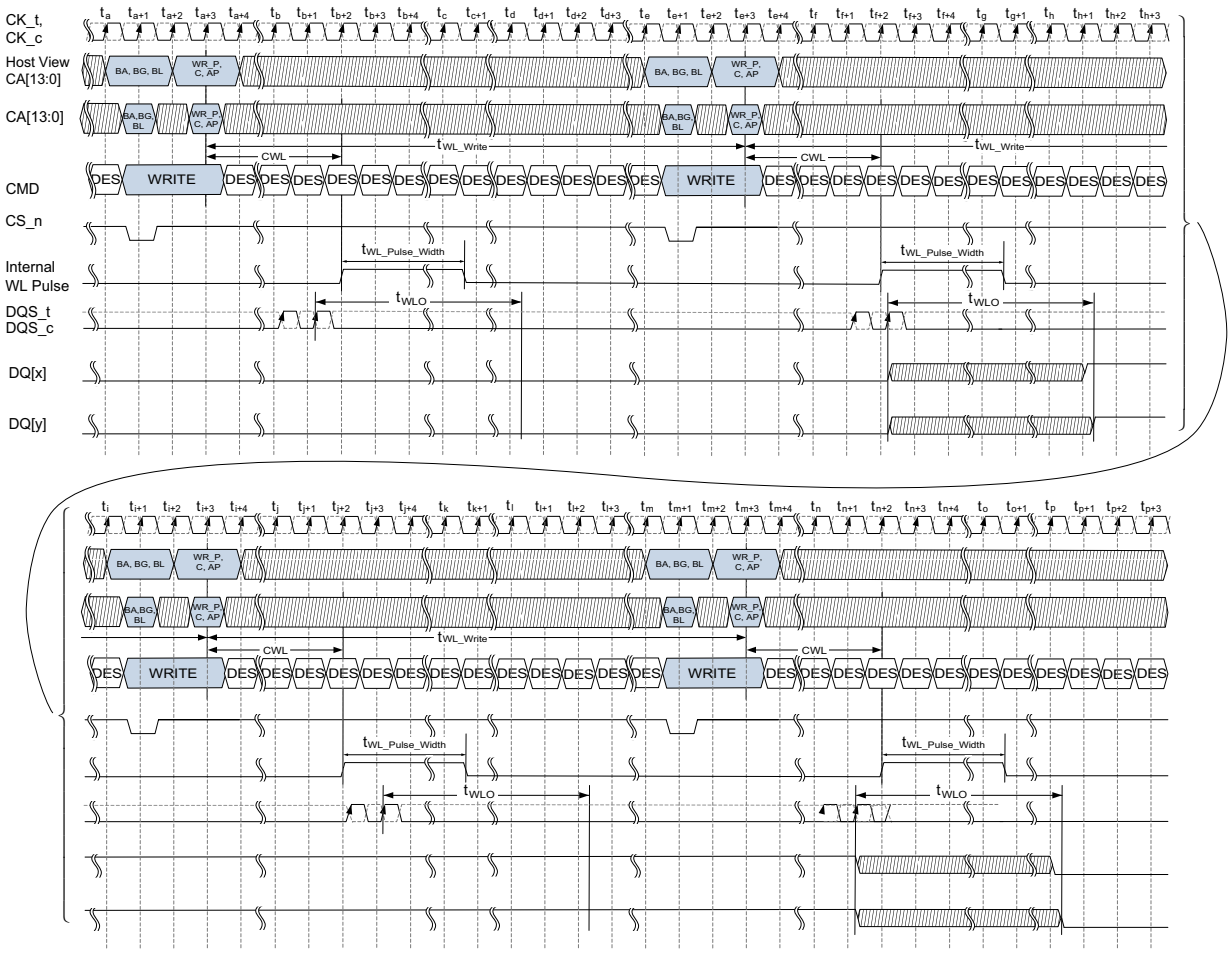


Figure 108 — Consecutive Write commands during Write Leveling Training Mode Example (External Training, 2N Mode, 4 Samples)

4.21.4 Write Leveling Internal Cycle Alignment Operation

After the external Write Leveling Training step is completed, and after the host DQS signals have been aligned to the pin-level Write Latency timing, the host will apply a negative offset (WL_ADJ_start) to the DQS timing. The WL_ADJ_start offset moves the DQS timing prior to the Internal Write Leveling Pulse (causing LOW observed on the DQ pins), and it is dependent on the tWPRE setting (shown in table below). This will be a reference point for aligning the ıInternal Write Leveling Pulse via the WICA settings in MR3.

The Internal Cycle Alignment training begins when an MRW command is issued to enable Internal Write Timing in MR2 (keeping OP[1]=1 and setting MR2:OP[7]=1). The host sweeps the Write Leveling Internal Cycle Alignment (WICA) delay settings in MR3, starting with the 0tCK offset default. Increasing the WICA mode register offset setting speeds up the timing of the WRITE command by reducing the WRITE Command to Internal Write Pulse delay until the DQS is aligned with the internal Write Leveling Pulse assertion. Alignment results in a logic HIGH on the DQ pins.

4.21.4 Write Leveling Internal Cycle Alignment Operation (cont'd)

Table 114 summarizes the WL_ADJ_start and WL_ADJ_end values per tWPRE setting:

Table 114 — WL_ADJ_Start and WL_ADJ_End Values per tWPRE Setting

WL_ADJ term	Description	tWPRE = 2 tCK	tWPRE = 3 tCK	tWPRE = 4 tCK [1]
WL_ADJ_start	Offset that the host applies to the DQS_t/DQS_c timing just after external Write Leveling alignment to Write Latency and prior the internal cycle alignment training.	-0.75 tCK	-1.25 tCK	-2.25 tCK
WL_ADJ_end	Offset that the host applies to the DQS_t/DQS_c timing after final phase alignment to the rising edge of the Write Leveling Internal Pulse. This will center the Write Leveling Internal Pulse rising edge within the preamble window.	1.25 tCK	1.75 tCK	2.75 tCK
NOTE 1 For tWPRE = 4 tCK, CL is required to be ≥ 30 during Write Leveling Training Mode operation. This is irrespective of the CL setting for tWPRE = 4 tCK during normal operation.				

Due to potential measurement errors that can occur during the internal Write Leveling Training, the DRAM may include an optional 0.5 tCK adjustment for optimizing the Internal Cycle Alignment. MR7:OP[0]=1 adds a +0.5 tCK adjustment for the lower byte of the DQs, while MR7:OP[1]=1, adds a +0.5 tCK adjustment for the upper byte of the DQs.

Figure 109 is an example of an Internal Write Leveling training flow with the addition of the +0.5tCK WICA adjustment (additional flow shown in blue).

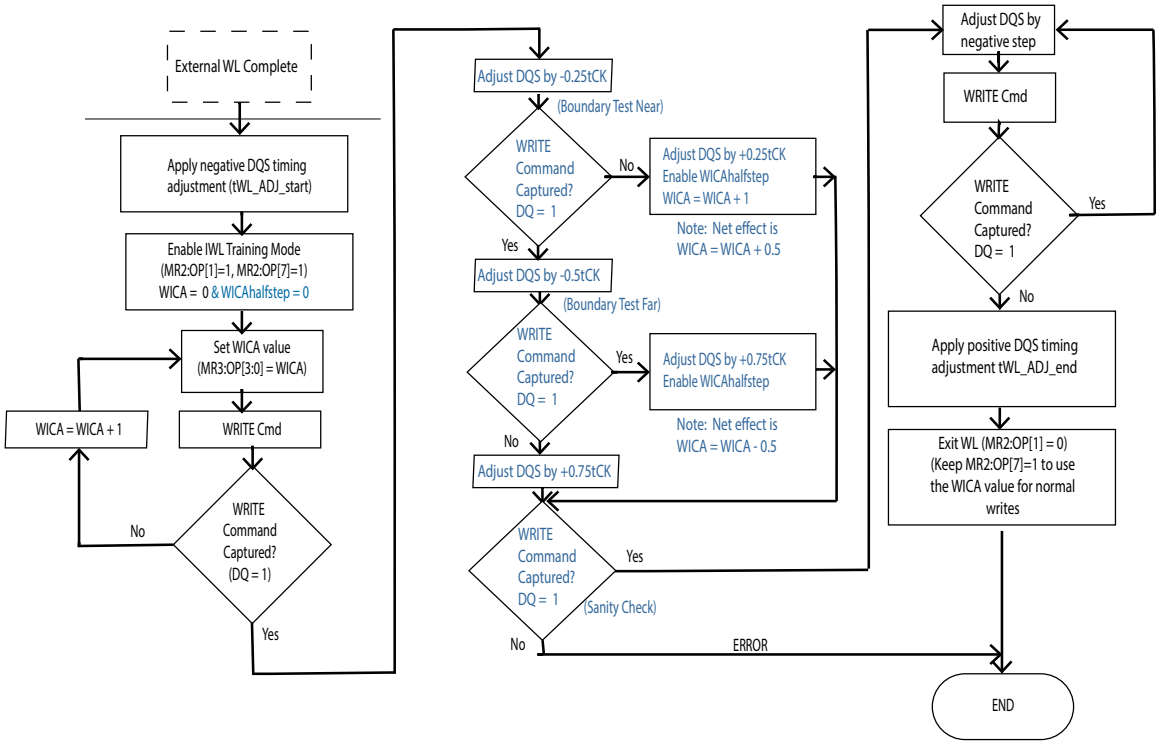


Figure 109 — Write Leveling Training Flow with Half Step WICA

4.21.4 Write Leveling Internal Cycle Alignment Operation (cont'd)

As previously noted, the DDR5 x16 devices allow for independent lower and upper byte Write Leveling Training and setting. Although unique values are preferred to optimize (minimize) tDQSoffset, setting both the lower and upper bytes to use the same WICA offset is allowed since the internal paths for both bytes are expected to be closely matched, meaning Internal Write Leveling Training that results in a differentbyte settings per byte indicates the internal paths are on a boundary between the two settings.When choosing a common WICA offset value, the startingvalues of the lower and upper WICA offset should differ by no more than one. The higher (smallest absolute value since the WICA values apply a negative offset) of the two values shall be programmed in both bytes of the DRAM to minimize the impact on the final training sweep

.

Lower Byte WICA	Upper Byte WICA	Common WICA
-4	-3	-3
-2	-3	-2

When choosing a common 0.5tCK WICA offset value, the WICA value programmed in both bytes of the DRAM shall be the same beforeapplying the 0.5tCK offset (if the byte values are different, the higher value shall be programmed in both bytes of the DRAM as noted above and the 0.5tCK offset step is skipped). If the 0.5tCK training indicates that one byte requires the +0.5tCK offset but the other byte does not, this also indicates the two bytes are on a boundary between the two settings. In this case, the +0.5tCK shall be applied to both bytes, resulting inthe higher (smallest absolute) value being used.

Lower Byte WICA	Lower Byte +0.5tCK WICA	Upper Byte WICA	Upper Byte +0.5tCK WICA	Common WICA
-4	n/a	-3	n/a	-3
-4	Yes	-4	No	-4+0.5 (-3.5 total)
-3	No	-3	Yes	-3+0.5 (-2.5 total)

When using a common WICA offset value approach to the Internal Write Leveling training, both bytes shall do the final training sweep after applying the common WICA offset value (both the full cycle and 0.5tCK WICA, if applicable).

The timing diagrams in Figure 110 and Figure 111 demonstrate Write Leveling Training operation when Internal Write Timings are enabled and the Internal Cycle Alignment is set such that the Internal Write Leveling Pulse has not yet reached the host DQS toggles.

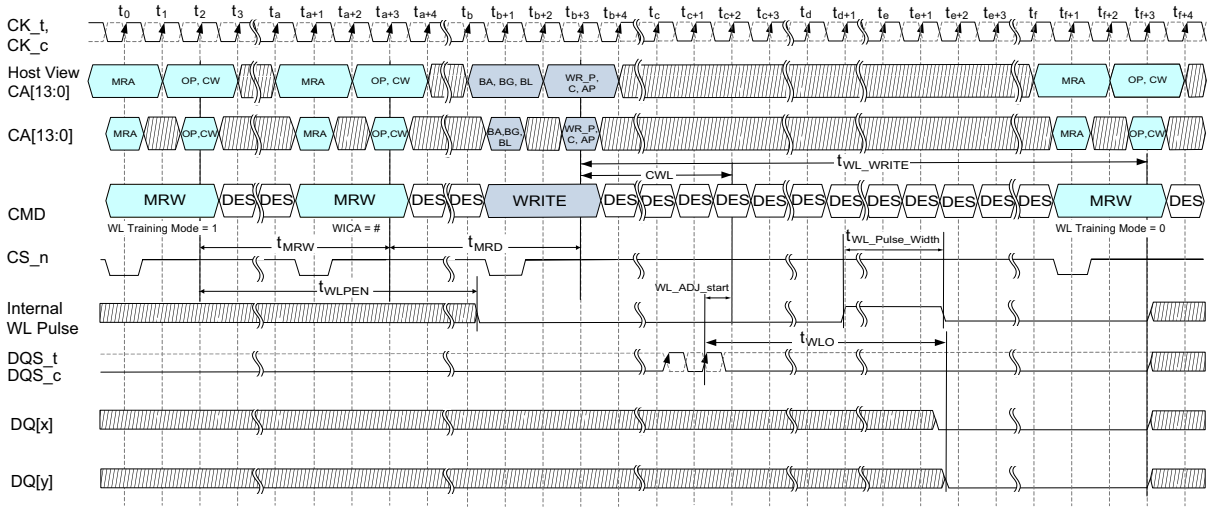


Figure 110 — Write Leveling Training Mode Timing Diagram (Internal Cycle Alignment, 2N Mode, 0 Sample)

4.21.4 Write Leveling Internal Cycle Alignment Operation (cont'd)

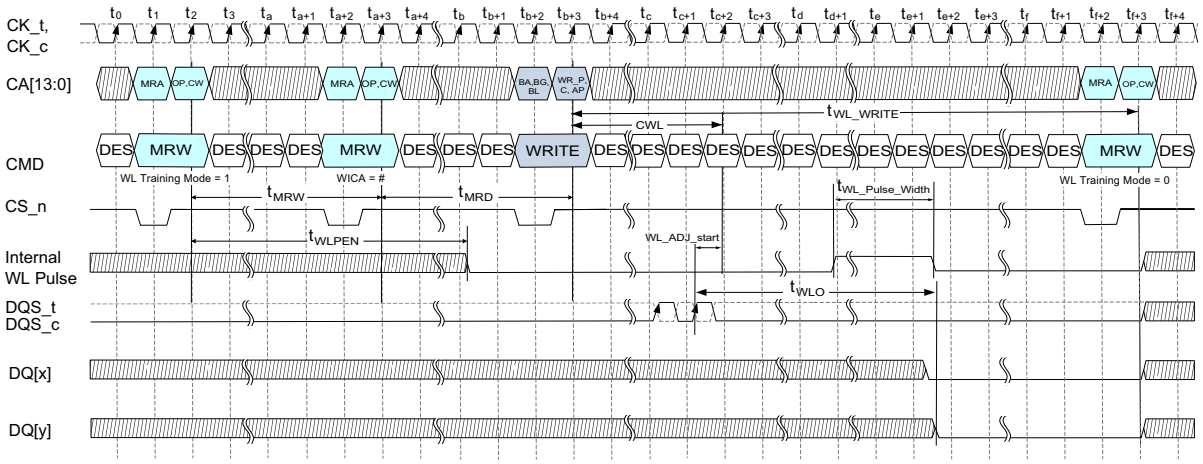


Figure 111 — Write Leveling Training Mode Timing Diagram (Internal Cycle Alignment, 1N Mode, 0 Sample)

The timing diagrams in Figure 112 and Figure 113 demonstrate Write Leveling Training operation when Internal Write Timings are enabled and the Internal Cycle Alignment is set such that the Internal Write Leveling Pulse has completed the coarse alignment to the host DQS timing.

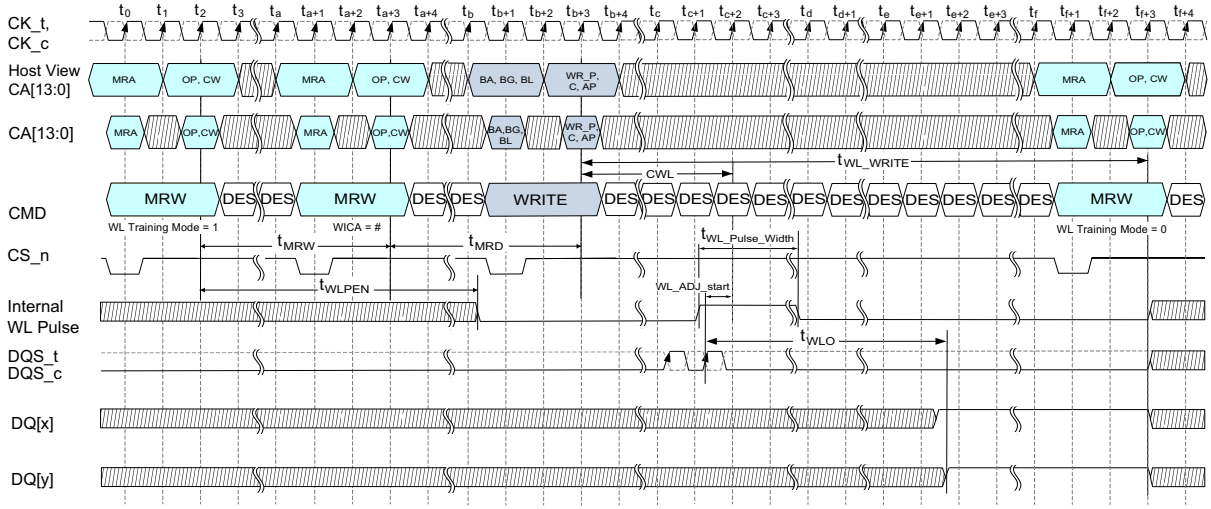


Figure 112 — Write Leveling Training Mode Timing Diagram (Internal Cycle Alignment, 2N Mode, 1 Sample)

4.21.4 Write Leveling Internal Cycle Alignment Operation (cont'd)

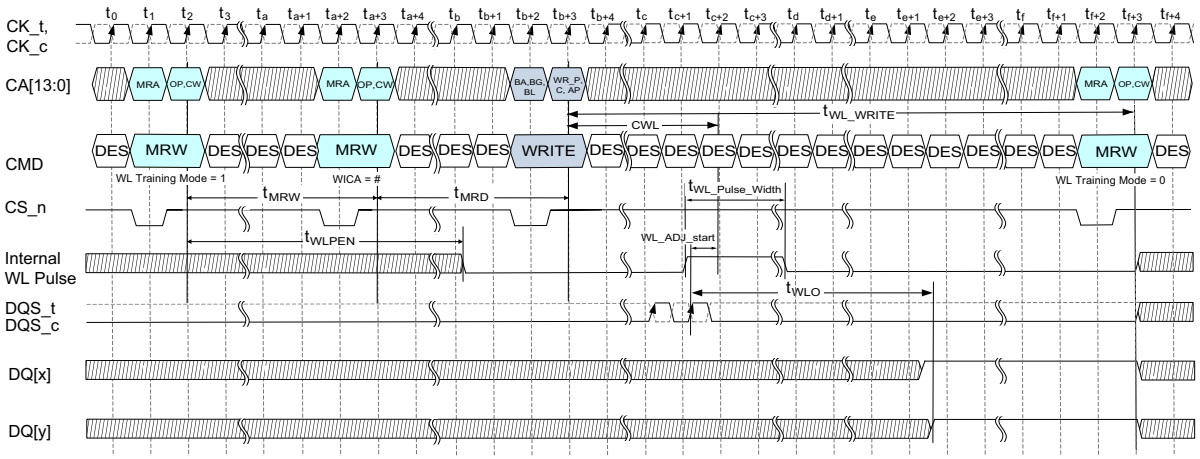


Figure 113 — Write Leveling Training Mode Timing Diagram (Internal Cycle Alignment, 1N Mode, 1 Sample)

4.21.4 Write Leveling Internal Cycle Alignment Operation (cont'd)

An example of Write Leveling Training internal Cycle Alignment executed by issuing consecutive Write commands after entering Write Leveling Mode has been enabled (no requirement to exit and reenter between each Write command) is shown in Figure 114.

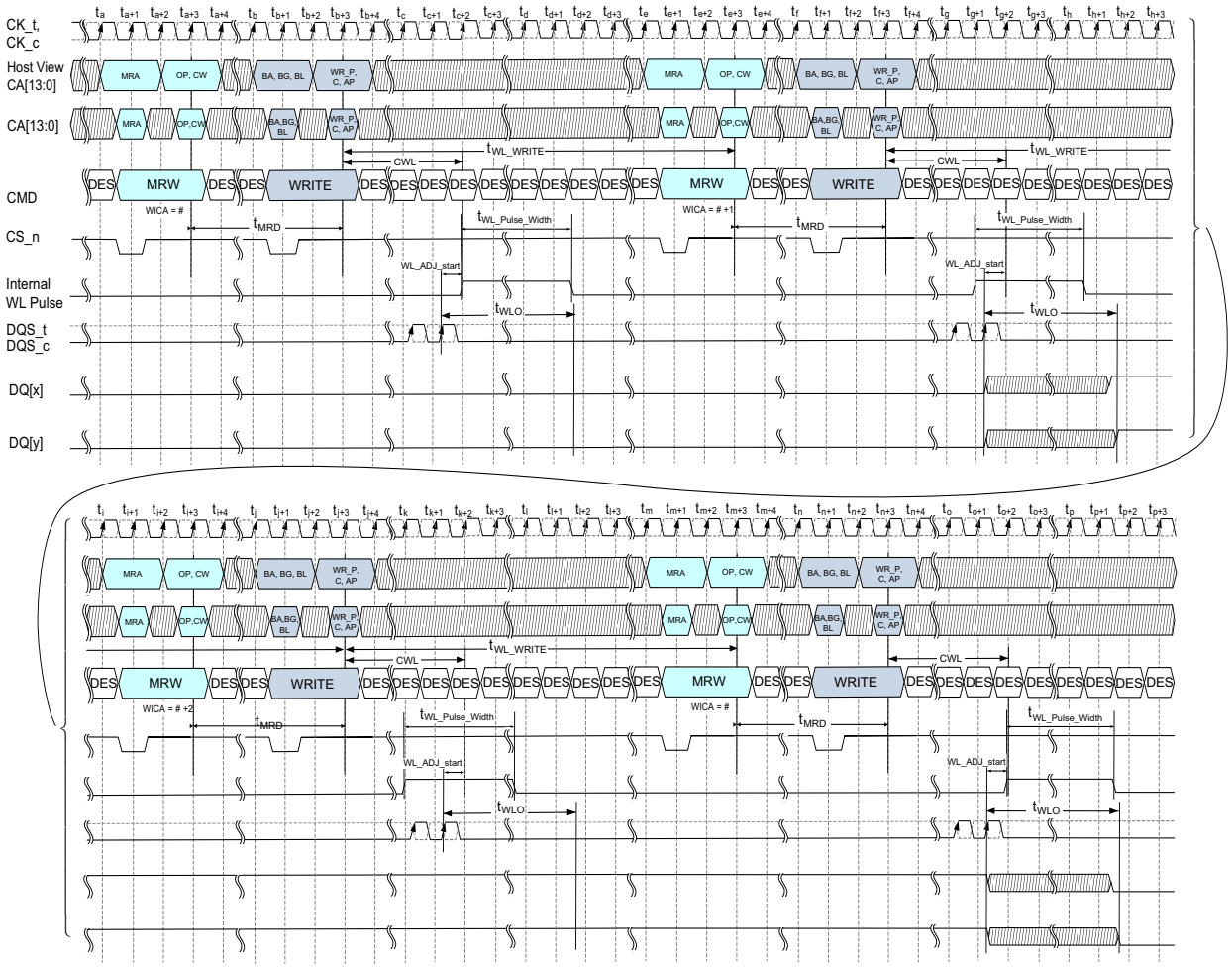


Figure 114 — Consecutive Write Commands during Write Leveling Training Mode Example (Internal Training, 2N Mode, 4 Samples)

4.21.5 Write Leveling Internal Phase Alignment and Final Host DQS Timing Operation

Once the Internal Cycle Alignment is achieved, the host shall perform a final fine sweep of the DQS timings with Internal Write Timing enabled (MR2:OP[7]=1) to establish an even closer phase alignment to the rising edge of the internal Write Leveling Pulse. Once this is complete, the host will then add a positive offset of WL_ADJ_end (dependent upon tWPRE) to the DQS timings. This results in a tDQSoffset between -0.5tCK and +0.5tCK with measurement adjustments of tWLS/tWLH, placing the rising edge of the Internal Write Leveling Pulse within the preamble. If the optional half step WICA process is used during Write Leveling training, this results in a tDQS offset between -0.25tCk and +0.25tCK with measurement adjustments of tWLS/tWLH. After the WL_ADJ_end offset has been applied, the host will disable Write Leveling Training Mode (MR2:OP[1]=0). The Internal Write Timing will remain enabled and the Internal Cycle Alignment setting will retain the coarse setting that was trained. After every reset, the host must either restore these settings or execute the full Write Leveling Training flow.

Figure 115 shows the timing relationships for the final placement of the host DQS–timings relative to the Internal Write Leveling Pulse. However, it is not necessary to execute this Write Leveling Training Mode Measurement to finalize the setting - this is only for illustration.

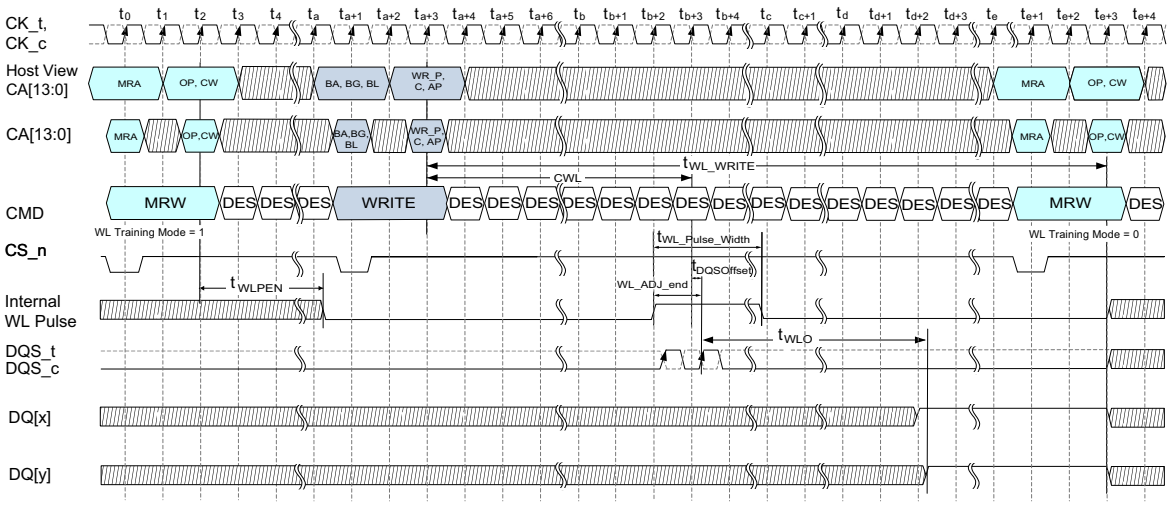


Figure 115 — Timing Diagram for Final Timings after Write Leveling Training is Complete (2N Mode)

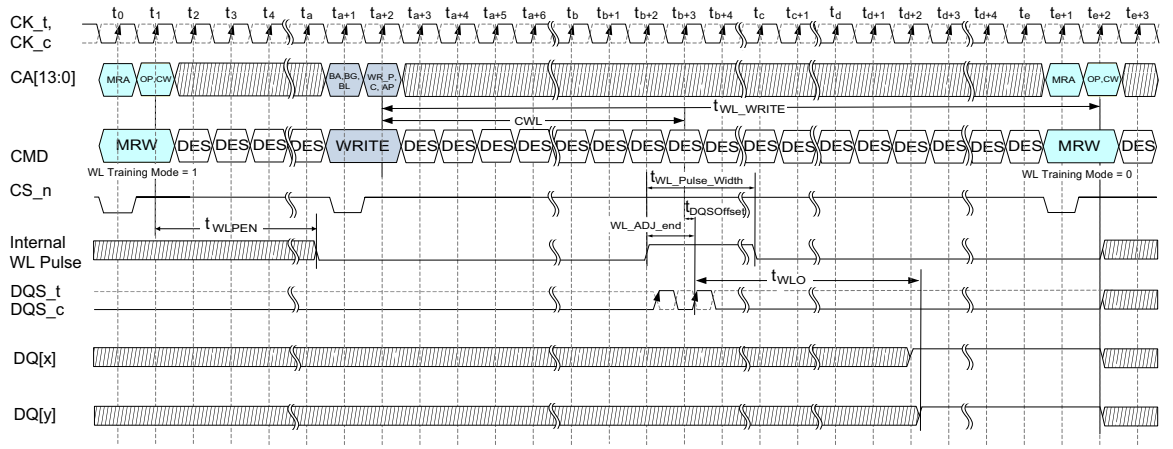


Figure 116 — Timing Diagram for Final Timings after Write Leveling Training is Complete (1N Mode)

4.21.5 Write Leveling Internal Phase Alignment and Final Host DQS Timing Operation (cont'd)

Table 115 summarizes the timing parameter ranges associated with Write Leveling Training Mode:.

Table 115 — Timing Parameter Ranges Associated with Write Leveling Training Mode

Parameter	Symbol	Min	Max	Units	Notes
Write Leveling Pulse Enable - Time from Write Leveling Training Enable MRW to when Internal Write Leveling Pulse logic level is valid	tWLPEN	-	15	ns	
Write leveling output	tWLO	-	9.5	ns	
Width of the Write Leveling Internal Pulse	tWL_Pulse_Width	2	-	tCK	1
Write Leveling Write to subsequent command spacing	tWL_Write	max(CWL, last DQS differential toggle) + tWLO(max)+ 2nCK	-		
NOTE 1 There is no Max limit for the tWL_Pulse_Width, but the Write Leveling Internal Pulse must begin at zero for each WRITE command.					

4.21.6 DRAM Termination During Write Leveling

When the DRAM is in Write Leveling Mode, the DQS_c/DQS_t termination (DQS_RTT_PARK) and the Command and Control termination (RTT_CA, RTT_CK, RTT_CS) will be the same as for functional operation. The DQ signals will not be terminated in the DRAM, but instead will be driving values to the controller. The host controller will apply termination for the DQ signals.

Table 116 — DRAM Termination During Write Leveling

ODT Enabled	DQS_t/DQS_c Termination	DQ Termination
RTT_WR	DQS_RTT_PARK	Off
RTT_PARK, RTT_WR disabled	DQS_RTT_PARK	Off
NOTE Termination for TDQS/DM is not included since TDQS and DM are disabled during Write Leveling Training Mode.		

4.22 Connectivity Test (CT) Mode

4.22.1 Introduction

The DDR5 memory device supports a connectivity test (CT) mode, which is designed to greatly speed up testing of electrical continuity of pin interconnection on the PC boards between the DDR5 memory devices and the memory controller on the SoC. Designed to work seamlessly with any boundary scan devices, the CT mode is required for **all** DRAM devices independent of density and interface width. This applies to x4, x8, and x16 interface widths. Contrary to other conventional shift register based test modes, where test patterns are shifted in and out of the memory devices serially in each clock, DDR5's CT mode allows test patterns to be entered in parallel into the test input pins and the test results extracted in parallel from the test output pins of the DDR5 memory device at the same time, significantly enhancing the speed of the connectivity check.

Prior to entering CT Mode, RESET_n is registered to High. The CT Mode is enabled by asserting the Test Enable (TEN) pin.

Once put in the CT mode by asserting the TEN pin, the DDR5 memory device effectively appears as an asynchronous device to the external controlling agent; after the input test pattern is applied, the connectivity test results are available for extraction in parallel at the test output pins after a fixed propagation delay. A reset of the DDR5 memory device is required after exiting the CT mode.

4.22.2 Pin Mapping

Only digital pins can be tested via the CT mode. For the purpose of connectivity check, all pins that are used for the digital logic in the DDR5 memory device are classified as one of the following types:

1. Test Enable (TEN) pin: when asserted high, this pin causes the DDR5 memory device to enter the CT mode. In this mode, the normal memory function inside the DDR5 memory device is bypassed and the IO pins appear as a set of test input and output pins to the external controlling agent. The TEN pin is dedicated to the connectivity check function and will not be used during normal memory operation.
2. Chip Select (CS_n) pin: when asserted low, this pin enables the test output pins in the DDR5 memory device. When de-asserted, the output pins in the DDR5 memory device will be Hi-z. The CS_n pin in the DDR5 memory device serves as the CS_n pin when in CT mode.
3. Test Input: a group of pins that are used during normal DDR5 DRAM operation are designated as test input pins. These pins are used to enter the test pattern in CT mode. Most Test Input pins are input pins during normal operation. The ALERT_n pin is the only output pin that will be used as a Test Input during CT mode. The CK_t and CK_c pins are single-ended Test Input pins during CT Mode.
4. Test Output: a group of pins that are used during normal DDR5 DRAM operation are designated test output pins. These pins are used for extraction of the connectivity test results in CT mode.
5. Reset: Fixed high level for RESET_n is required during CT mode, same as normal function.

Table 117 shows the pin classification of the DDR5 memory device.

Table 117 — Pin Classification of DDR5 Memory Device in Connectivity Test (CT) Mode [1, 2]

Pin Type in CT Mode		Pin Names during Normal Memory Operation
Test Enable		TEN
Chip Select		CS_n
Test Inputs	A	CA[13:0]
	B	CK_t, CK_c
	C	ALERT_n
Test Outputs		DQL[7:0], DQU[7:0], DQSU_t, DQSU_c, DQSL_t, DQSL_c, DML_n, DMU_n, DM_n/TDQS_t, TDQS_c
Reset		RESET_n

NOTE 1 Test Outputs may contain the Upper and Lower label identification used with x16 devices. In the case of x4/x8 devices, the lower (L) identification may be removed.
NOTE 2 CAI and MIR input level do not affect to "Test Outputs" values.

Table 118 — Signal Description

Symbol	Type	Function
TEN	Input	Connectivity Test Mode is active when TEN is HIGH and inactive when TEN is LOW. TEN must be LOW during normal operation TEN is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of VDDQ.

4.22.3 Logic Equations

4.22.3.1 Min Term Equations

MTx is an internal signal to be used to generate the signal to drive the output signals. These internal signals are the same across all interface widths and densities.

Table 119 — Min Term Equations

Min Term	Intermediate Logic Nodes
MT0	XOR(CA[0,1,2,3,8,9,10,11])
MT1	XOR(CA[0,4,5,6,8,12,13], ALERT_n)
MT2	XOR(CA[1,4,9,12], CK_t, CK_c)
MT3	XOR(CA[2,5,7,10,13], CK_t)
MT4	XOR(CA[3,6,7,11], CK_c, ALERT_n)
MT0_B	!(MT0)
MT1_B	!(MT1)
MT2_B	!(MT2)
MT3_B	!(MT3)
MT4_B	!(MT4)

4.22.3.2 Output Equations

Table 120 — Output Equations per Interface Width

Output	X16	X8	X4
DQL0	MT0	MT0	MT0
DQL1	MT1	MT1	MT1
DQL2	MT2	MT2	MT2
DQL3	MT3	MT3	MT3
DQL4	MT0_B	MT0_B	
DQL5	MT1_B	MT1_B	
DQL6	MT2_B	MT2_B	
DQL7	MT3_B	MT3_B	
DML	MT4	MT4	
TDQS_c		MT4_B	
DQSL_t	MT4	MT4	MT4
DQSL_c	MT4_B	MT4_B	MT4_B
DQU0	MT0		
DQU1	MT1		
DQU2	MT2		
DQU3	MT3		
DQU4	MT0_B		
DQU5	MT1_B		
DQU6	MT2_B		
DQU7	MT3_B		
DMU	MT4		
DQSU_t	MT4		
DQSU_c	MT4_B		

NOTE Test Outputs may contain the Upper and Lower label identification used with x16 devices. In the case of x4/x8 devices, the lower (L) identification may be removed.

4.23 ZQ Calibration Commands

4.23.1 ZQ Calibration Description

The MPC command is used to initiate ZQ Calibration, which calibrates the output driver and command/address termination impedance across process, temperature, and voltage. ZQ Calibration occurs in the background of device operation.

There are two ZQ Calibration modes initiated with the MPC command: ZQCal Start, and ZQCal Latch. ZQCal Start initiates the DRAM's calibration procedure, and ZQCal Latch captures the calibration result and loads it into the DRAM's drivers and termination circuits.

A ZQCal Start command may be issued anytime the DRAM is in a state in which it can receive valid commands. There are two timing parameters associated with ZQ Calibration. tZQCAL is the time from when the ZQCal Start MPC command is sent to when the host can send the ZQCal Latch MPC command. tZQLAT is the time from when the ZQCal Latch MPC command is sent by the host to when the CA bus (and subsequently the DQ bus) can be used for normal operation. A ZQCal Latch Command may be issued anytime outside of power-down after tZQCAL has expired and all DQ bus operations have completed. The CA Bus must maintain a Deselect state during tZQLAT to allow CA ODT calibration settings to be updated.

Issuing consecutive ZQCAL Start commands is permitted, and subsequent commands not violating tZQCal of an ongoing ZQ calibration will initiate a new ZQ calibration operation. ZQCal Start commands violating tZQCal may or may not initiate a new ZQ calibration operation.In this case, tZQCal should be counted from the last issued ZQCal start command.

A ZQCal Latch command issued before the expiration of tZQCal may latch or relatch the results of a previous ZQ Calibration operation that completed the calibration. A ZQCal Latch command issued without rerunning the ZQ Calibration operation will relatch the results of the previous ZQ Calibration operation that completed.

The appropriate interval between ZQCal Start commands can be determined from the 'ODT Voltage and Temperature Sensitivity' tables and other application-specific parameters. One method for calculating the interval between ZQCal Start commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the DRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\textbf{ZQCorrection}}{\textbf{(TSens x Tdriftrate) + (VSens x Vdriftrate)}}$$

, where TSens = max(dRTTdT, dRondT) and VSens = max(dRTTdV, dRondV) define the DRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% / °C, VSens = 0.15% / mV, Tdriftrate = 1°C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$

Table 121 — ZQ Calibration Timing Parameters

Parameter	Symbol	Min/Max	Value	Unit
ZQ Calibration Time	tZQCAL	MIN	1	µs
ZQ Calibration Latch Time	tZQLAT	MIN	max(30ns,8nCK)	ns

Table 122 — ODT Temperature and Voltage Sensitivity

Change [1]	Min	Max	Unit
dRTTdT	-1.5	1.5	%/℃
dRTTdV	-0.15	0.15	%/mv
NOTE 1 Amount of changes might be design guaranteed, and actual numbers would be vendor specific.			

4.23.1 ZQ Calibration Description (cont'd)

Table 123 — Ron Temperature and Voltage Sensitivity

Change [1]	Min	Max	Unit
dRondT	-1.5	1.5	%/℃
dRondV	-0.15	0.15	%/mv
NOTE 1 Amount of changes might be design guaranteed, and actual numbers would be vendor specific.			

4.23.2 ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and VSS.

If the system configuration has more than one rank, and if the ZQ pins of both ranks are attached to a single resistor, then the SDRAM controller must ensure that the ZQ Cals do not overlap.

The total capacitive loading on the ZQ pin must not exceed the max external loading of 25 pF with the addition of the device ZQ pin cap (5 pF) for a total capacitive loading of 30 pF.

4.24 VrefCA Command

4.24.1 Introduction

The VrefCA setting must be set prior to training the CS_n and CA bus timings relative to CK. In order to accomplish this, DDR5-SDRAMs will support a 1-cycle command specifically for setting the VrefCA setting. This avoids any timing and/or default VrefCA setting issues with sending a 2-cycle MRW command, by enabling the host to extend the setup and hold time for the CA signals. In addition, the VrefCA command will support multiple cycles of CS_n assertion. The multiple cycles of CS_n assertion ensures the DRAM will capture the VrefCA command during at least one rising CK_t/CK_c edge.

Table 124 — VrefCA Command Definition

Function	Abbreviation	CS	CA Pins													NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
VrefCA Command	VrefCA	L	H	H	L	L	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	L	V	

4.24.2 VrefCA Command Timing

The following diagram illustrates a timing sequence example for the VrefCA command that occurs prior to CS and CA training. The command is sampled on every rising edge of CK_t/CK_c. The host shall ensure that the CA signals are valid during the entire CS_n assertion time. The timing of the CS_n assertion may not satisfy the setup/hold requirements around all CK_t/CK_c transitions, but it will satisfy the setup/hold requirements relative to at least one CK_t/CK_c rising edge.

Multi-cycle CS assertion is enabled or disabled by programming the mode register MR2:OP[4] bit. This timing relationship can always be used by the host to send the VrefCA commands even after training has been completed for the interface. For the DRAM to latch the VrefCA command in cases where the alignment between CS_n, CA, and CK may be unknown, the CA inputs shall reach the proper command state at least three cycles prior to CS_n transitioning from high to low, CS_n shall remain low for tVrefCA_CS, and CA shall remain in the proper command state for at least three cycles after CS_n transitions from low to high.

4.24.2 VrefCA Command Timing (cont'd)

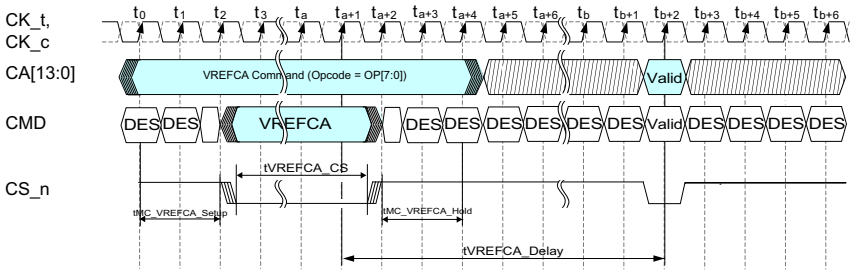


Figure 117 — Timing Diagram for VrefCA Command

Table 125 — AC Parameters for VrefCA Command

Symbol	Description	Min	Max	Unit	Note
tVrefCA_Delay	VrefCA command to any other valid command delay	tMRD	-	nCK	
tVrefCA_CS	Time CS_n is held low to register VrefCA command	3.5	8	nCK	1, 2
tMC_VREFCA_Setup	Min time between stable VREFCA command and first falling CS edge (SETUP)	3	-	nCK	3
tMC_VREFCA_Hold	Min time between first rising CS edge and stable VREFCA command (HOLD)	3	-	nCK	3

NOTE 1 Multiple cycles are used to avoid possible metastability of CS_n.
NOTE 2 At the end of CSTM and CATM, it is assumed that the host should be able to place the CS_n and the CA signals appropriately.
NOTE 3 This applies only to Multi-Cycle VREFCA commands when MR2:OP[4]=0_B.

4.25 VrefCS Command

4.25.1 Introduction

The VrefCS setting should be set, if needed, prior to training the CS_n and CA bus timings relative to CK. In order to accomplish this, DDR5-SDRAMs will support a 1-cycle command specifically for setting the VrefCS setting (similar to VrefCA). This avoids any timing and/or default VrefCS setting issues with sending a 2-cycle MRW command, by enabling the host to extend the setup and hold time for the CA signals. In addition, the VrefCS command will support multiple cycles of CS_n assertion. The multiple cycles of CS_n assertion ensures the DRAM will capture the VrefCS command during at least one rising CK_t/CK_c edge.

NOTE: The operation, functionality and timings for VrefCS are effectively the same as VrefCA with the exception of a different explicit command noted below and the fact that it modifies the VREF of the chip select pin vs the CA pins.

Table 126 — VrefCS Command Definition

Function	Abbreviation	CS	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
VrefCS Command	VrefCS	L	H	H	L	L	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	H	V	

4.25.2 VrefCS Command Timing

The following diagram illustrates a timing sequence example for the VrefCS command that occurs prior to CS and CA training. The command is sampled on every rising edge of CK_t/CK_c. The host shall ensure that the CA signals are valid during the entire CS_n assertion time. The timing of the CS_n assertion may not satisfy the setup/hold requirements around all CK_t/CK_c transitions, but it will satisfy the setup/hold requirements relative to at least one CK_t/CK_c rising edge.

Multi-Cycle CS assertion is enabled or disabled by programming the mode register MR2:OP[4] bit. This timing relationship can always be used by the host to send the VrefCS commands even after training has been completed for the interface. For the DRAM to latch the VrefCS command in cases where the alignment between CS_n, CA, and CK may be unknown, the CA inputs shall reach the proper command state at least three cycles prior to CS_n transitioning from high to low, CS_n shall remain low for tVrefCS_CS, and CA shall remain in the proper command state for at least three cycles after CS_n transitions from low to high.

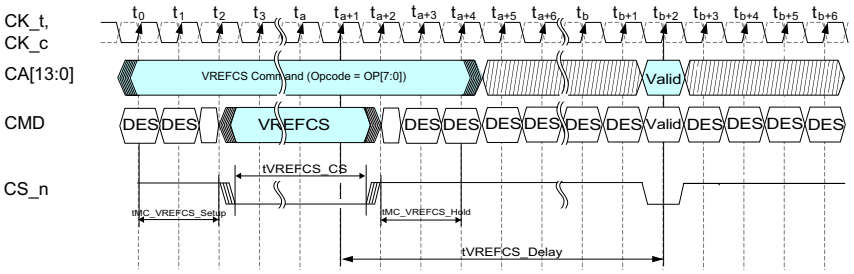


Figure 118 — Timing Diagram for VrefCS Command

Table 127 — AC Parameters for VrefCS Command

Symbol	Description	Min	Max	Unit	Note
tVrefCS_Delay	VrefCS command to any other valid command delay	tMRD	-	nCK	
tVrefCS_CS	Time CS_n is held low to register VrefCS command	3.5	8	nCK	1, 2
tMC_VREFCS_Setup	Min time between stable VREFCS command and first falling CS edge (SETUP)	3	-	nCK	3
tMC_VREFCS_Hold	Min time between first rising CS edge and stable VREFCS command (HOLD)	3	-	nCK	3

NOTE 1 Multiple cycles are used to avoid possible metastability of CS_n.
NOTE 2 At the end of CSTM and CATM, it is assumed that the host should be able to place the CS_n and the CA signals appropriately.
NOTE 3 This applies only to Multi-Cycle VREFCS commands when MR2:OP[4]=0_B.

4.26 VrefCA Training Specification

The DRAM internal VrefCA specification parameters are voltage operating range, stepsize, VrefCA set tolerance, VrefCA step time and Vref valid level.

The voltage operating range specifies the minimum required VrefCA setting range for DDR5 DRAM devices. The minimum range is defined by VrefCAmax and VrefCAmin as depicted in Figure 119.

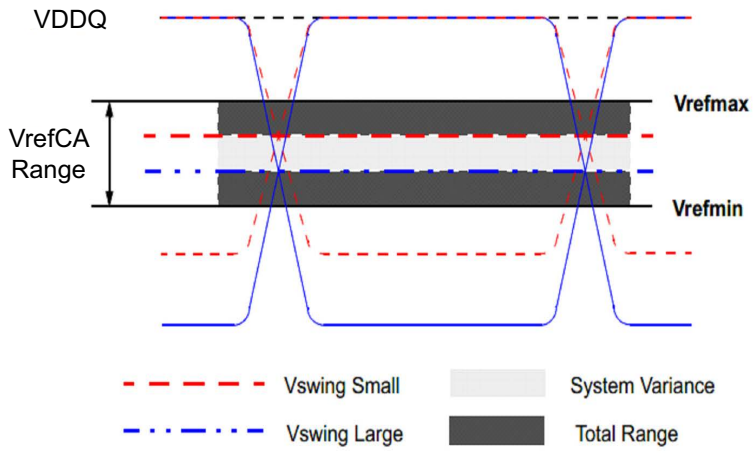


Figure 119 — VrefCA Operating Range (Vrefmin, Vrefmax)

The VrefCA stepsize is defined as the stepsize between adjacent steps. For a given design the DRAM VrefCA step size must be within the range specified.

The VrefCA set tolerance is the variation in the VrefCA voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for VrefCA set tolerance uncertainty. The range of VrefCA set tolerance uncertainty is a function of number of steps n.

The VrefCA set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max VrefCA values for a specified range. An illustration depicting an example of the stepsize and VrefCA set tolerance is shown in Figure 120.

4.26 VrefCA Training Specification (cont'd)

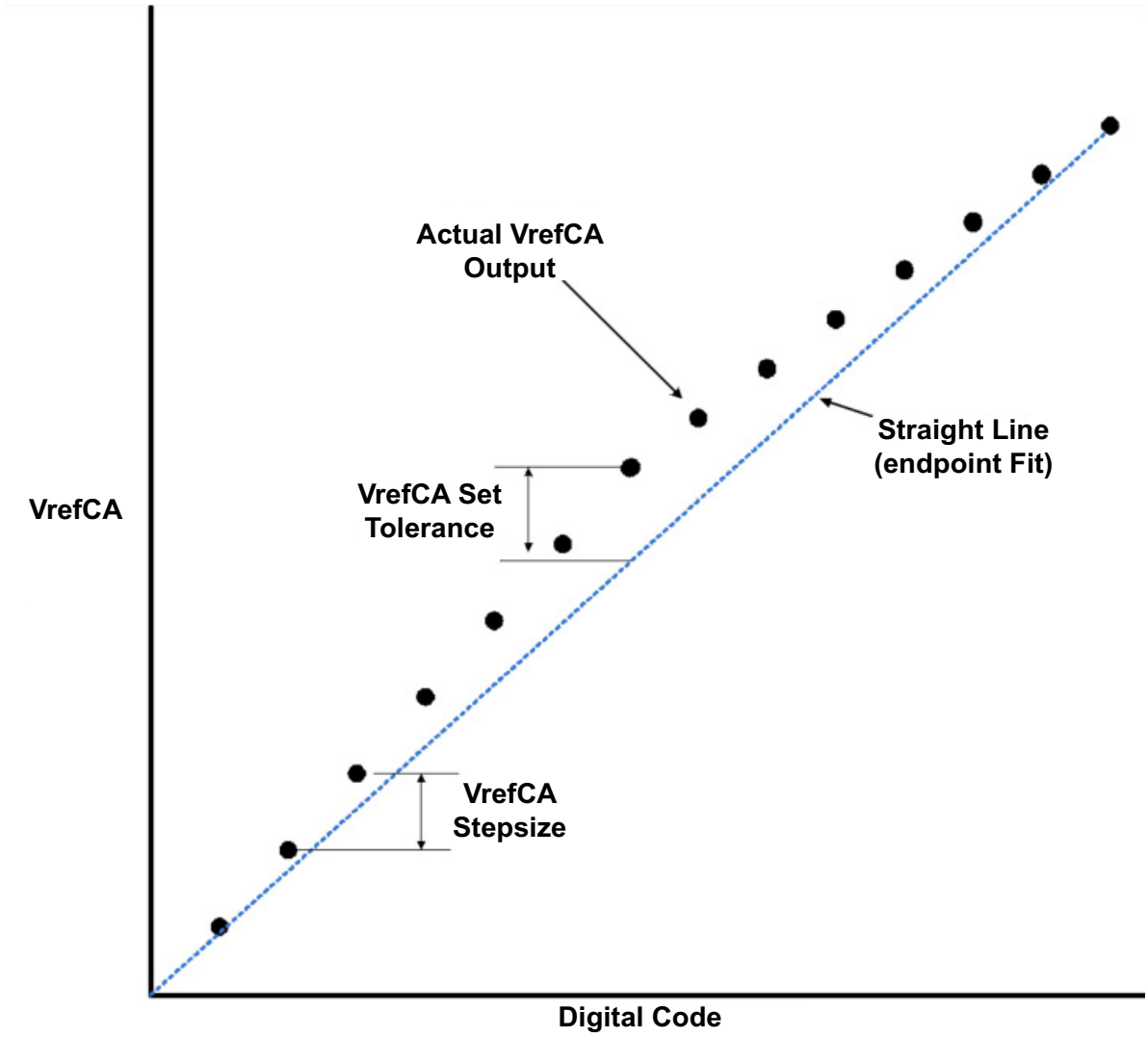


Figure 120 — Example of Vref Set Tolerance (only Max Case is Shown) and Stepsize

The VrefCA increment/decrement step times are defined by VrefCA_time. The VrefCA_time is defined from t0 to t1 as shown in Figure 121, where t1 is referenced to when the VrefCA voltage is at the final DC level within the VrefCA valid tolerance (Vref_val_tol).

The VrefCA valid level is defined by VrefCA_val tolerance to qualify the step time t1 as shown in Figure 121. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any VrefCA increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

t0 - is referenced to MPC Apply VREFCA and RTT_CA/CS/CK

t1 - is referenced to the VrefCA_val_tol

4.26 VrefCA Training Specification (cont'd)

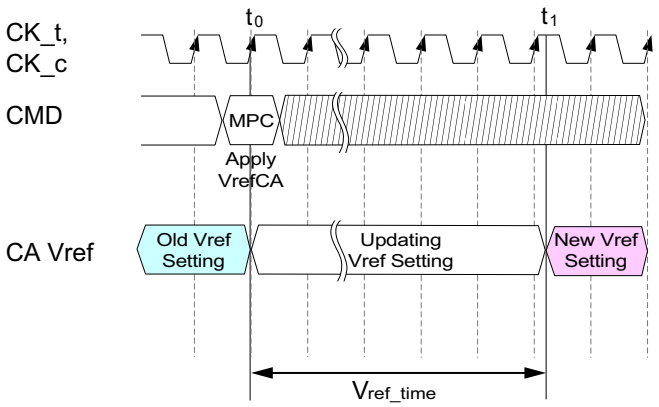


Figure 121 — Vref_Time Timing Diagram

The minimum time required between two Vref commands is VrefCA_time, shown as Vref_time in Figure 121.

A VrefCA command is used to store the VREF values into the VREF CA MR11. This mode register is only programmed via the command but is readable via a normal MRR.

4.26 VrefCA Training Specification (cont'd)

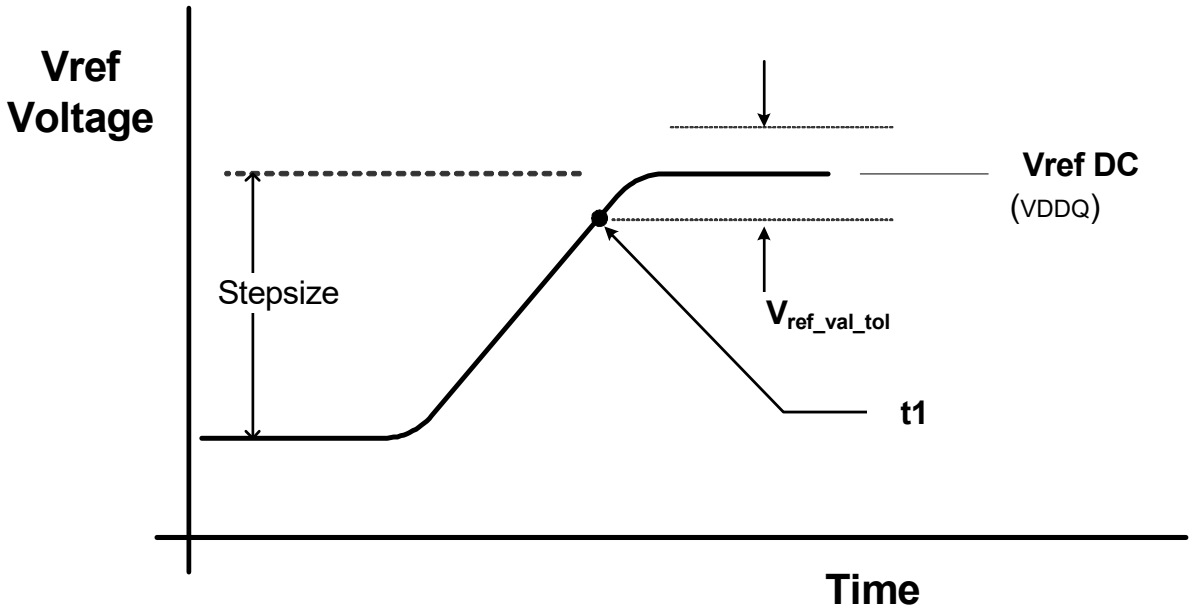


Figure 122 — Vref Step Single Stepsize Increment Case

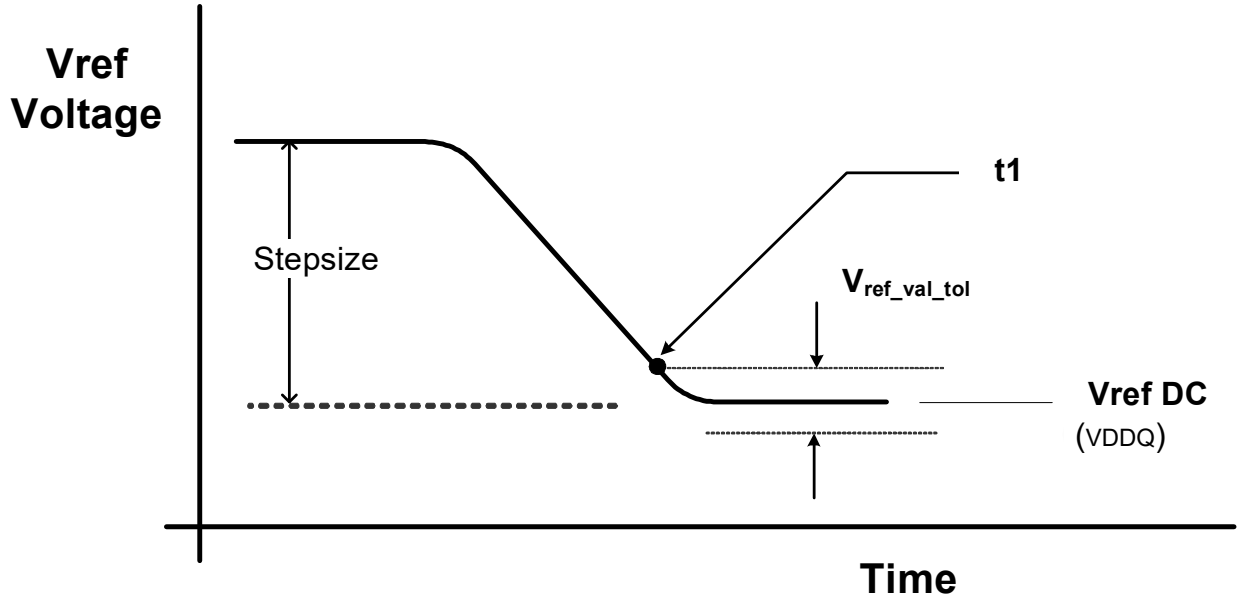


Figure 123 — Vref Step Single Stepsize Decrement Case

4.26 VrefCA Training Specification (cont'd)

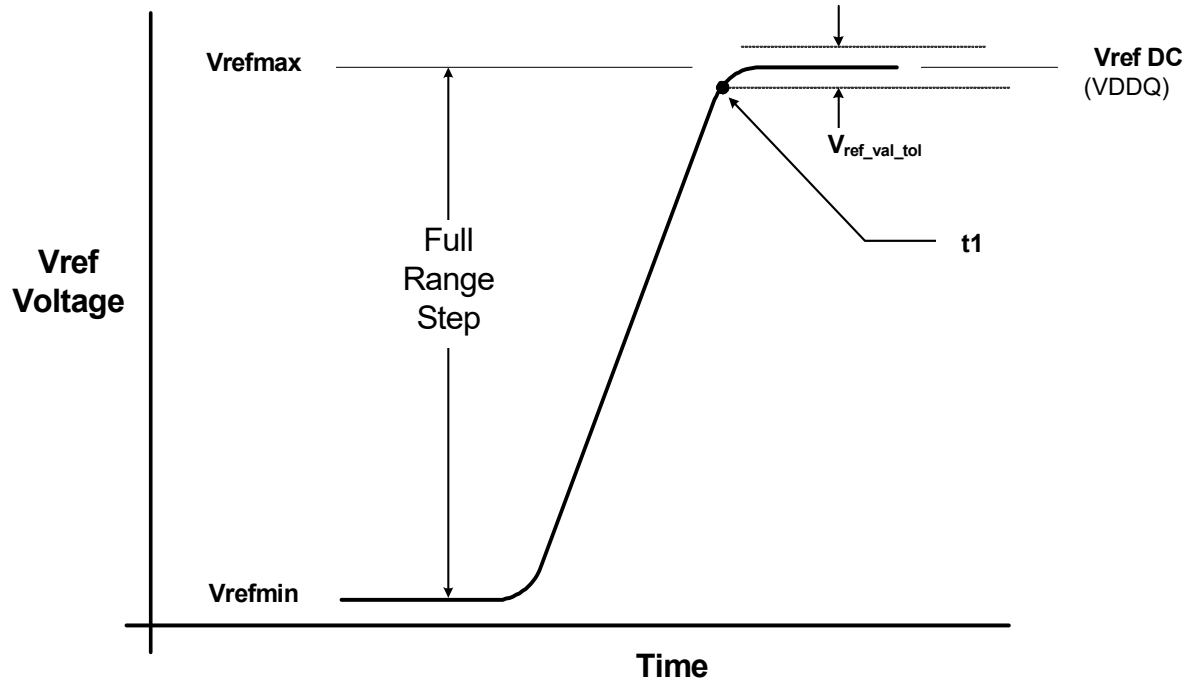


Figure 124 — Vref Full Step from Vrefmin to Vrefmax Case

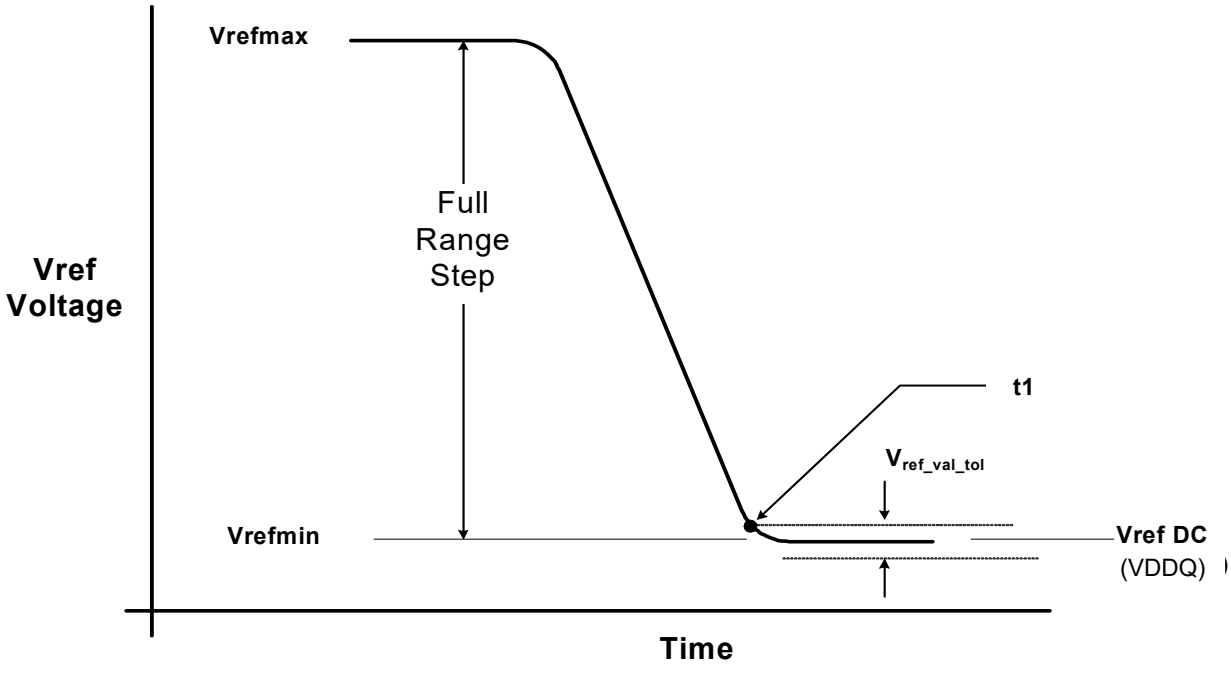


Figure 125 — Vref Full Step from Vrefmax to Vrefmin Case

4.26 VrefCA Training Specification (cont'd)

Table 128 — CA Internal VREF Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
VrefCA Max operating point	V_{refCA_max}	97.5%	-	-	VDDQ	1
VrefCA Min operating point	V_{refCA_min}	-	-	35%	VDDQ	1
VrefCA Stepsize	V_{refCA_step}	0.41%	0.50%	0.59%	VDDQ	2
VrefCA Set Tolerance	$V_{refCA_set_tol}$	-1.625%	0.00%	1.625%	VDDQ	3, 4, 6
	$V_{refCA_set_tol}$	-0.15%	0.00%	0.15%	VDDQ	3, 5, 7
VrefCA Step Time	V_{refCA_time}	-	-	300	ns	8
VrefCA Valid Tolerance	$V_{refCA_val_tol}$	-0.15%	0.00%	0.15%	VDDQ	9

NOTE 1 VrefCA DC voltage referenced to VDDQ_DC.

NOTE 2 VrefCA stepsize increment/decrement range. VrefCA at DC level.

NOTE 3 VrefCA_new = VrefCA_old ± n*VrefCA_step; n= number of steps; if increment use "+"; If decrement use "-"

NOTE 4 The minimum value of VrefCA setting tolerance = VrefCA_new - 1.625%*VDDQ. The maximum value of VrefCA setting tolerance = VrefCA_new + 1.625%*VDDQ. For n>4

NOTE 5 The minimum value of VrefCA setting tolerance = VrefCA_new - 0.15%*VDDQ. The maximum value of VrefCA setting tolerance = VrefCA_new + 0.15%*VDDQ. For n≤ 4

NOTE 6 Measured by recording the min and max values of the VrefCA output over the range, drawing a straight line between those points and comparing all other VrefCA output settings to that line

NOTE 7 Measured by recording the min and max values of the VrefCA output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other VrefCA output settings to that line

NOTE 8 Time from MPC (Apply VREFCA, VREFCS, RTT_CK/CS/CA) command to increment or decrement

NOTE 9 Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. VrefCA valid is to qualify the step times which will be characterized at the component level

4.27 VrefCS Training Specification

The DRAM internal VrefCS specification parameters are voltage operating range, stepsize, VrefCS set tolerance, VrefCS step time and Vref valid level.

The voltage operating range specifies the minimum required VrefCS setting range for DDR5 DRAM devices. The minimum range is defined by VrefCSmax and VrefCSmin as depicted in Figure 126.

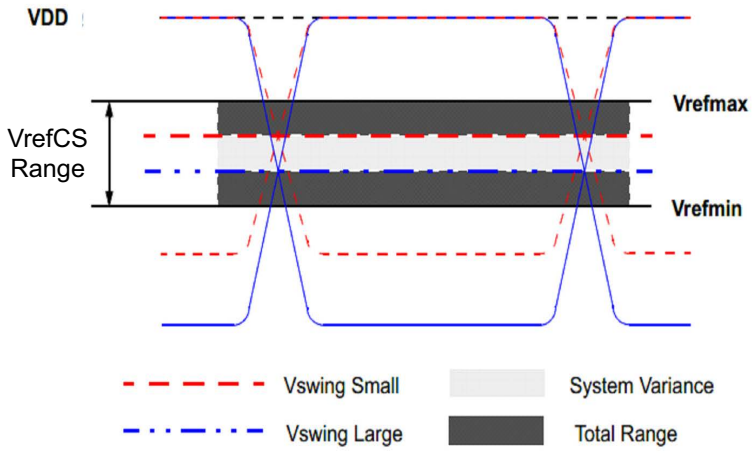


Figure 126 — VrefCS Operating Range (Vrefmin, Vrefmax)

The VrefCS stepsize is defined as the stepsize between adjacent steps. For a given design the DRAM VrefCS step size must be within the range specified.

The VrefCS set tolerance is the variation in the VrefCS voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for VrefCS set tolerance uncertainty. The range of VrefCS set tolerance uncertainty is a function of number of steps n.

The VrefCS set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max VrefCS values for a specified range. An illustration depicting an example of the stepsize and VrefCS set tolerance is shown in Figure 127.

4.27 VrefCS Training Specification (cont'd)

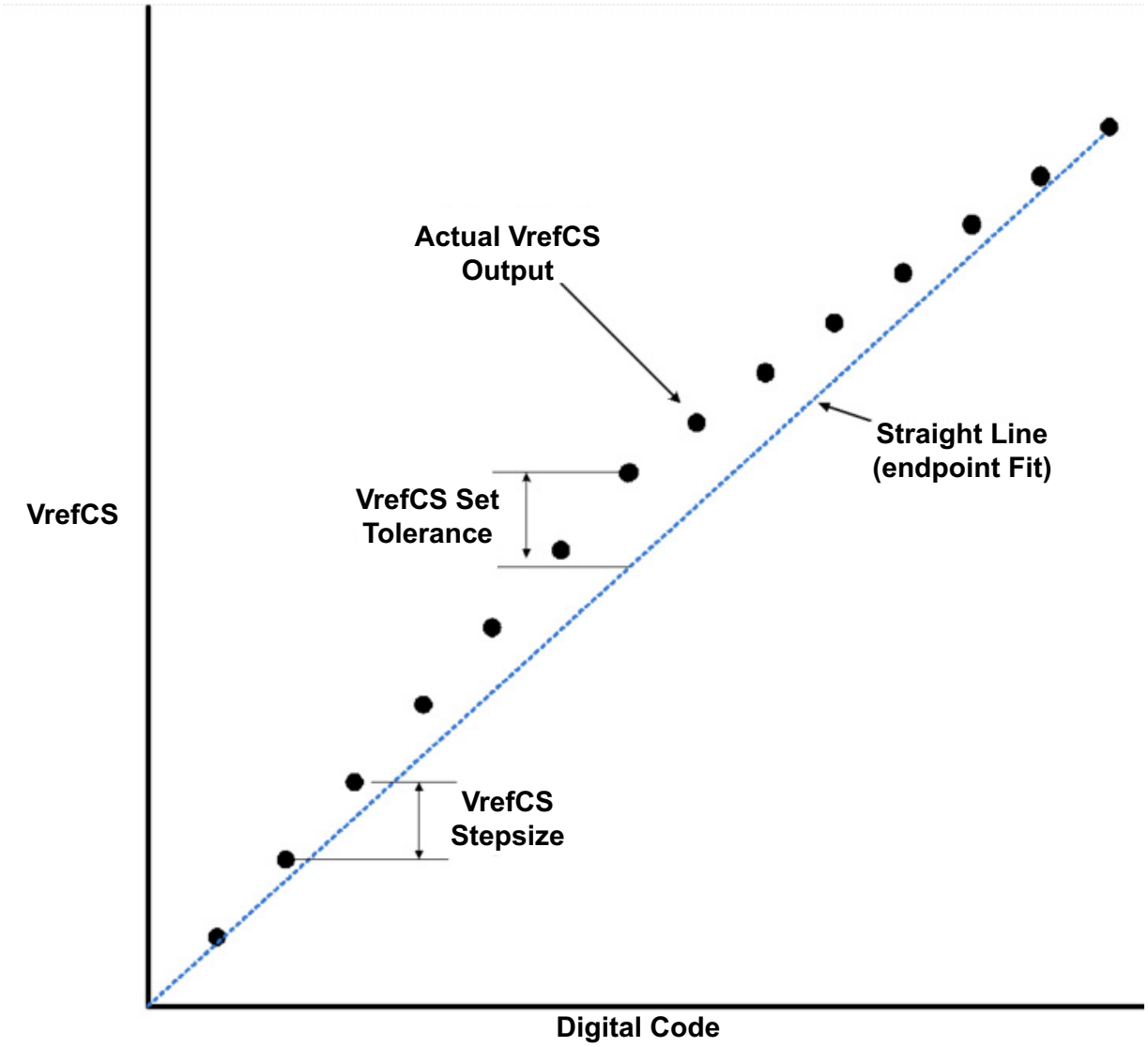


Figure 127 — Example of Vref Set Tolerance (only Max Case is Shown) and Stepsize

The VrefCS increment/decrement step times are defined by VrefCS_time. The VrefCS_time is defined from t0 to t1 as shown in Figure 128, where t1 is referenced to when the VrefCS voltage is at the final DC level within the VrefCS valid tolerance (VrefCS_val_tol).

The VrefCS valid level is defined by VrefCS_val tolerance to qualify the step time t1 as shown in Figure 128. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any VrefCS increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

t0 - is referenced to MPC Apply VREFCS and RTT_CA/CS/CK

t1 - is referenced to the VrefCS_val_tol

4.27 VrefCS Training Specification (cont'd)

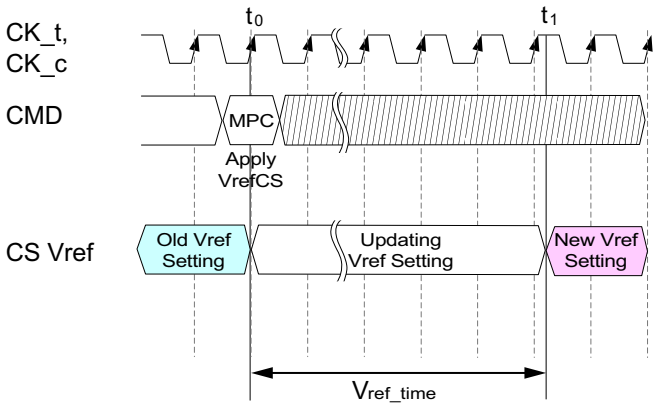


Figure 128 — Vref_Time Timing Diagram

The minimum time required between two Vref commands is VrefCS_time, shown as Vref_time in images above.

A VrefCS command is used to store the VREF values into the VREF CS MR12. This mode register is only programmed via the command but is readable via a normal MRR.

4.27 VrefCS Training Specification (cont'd)

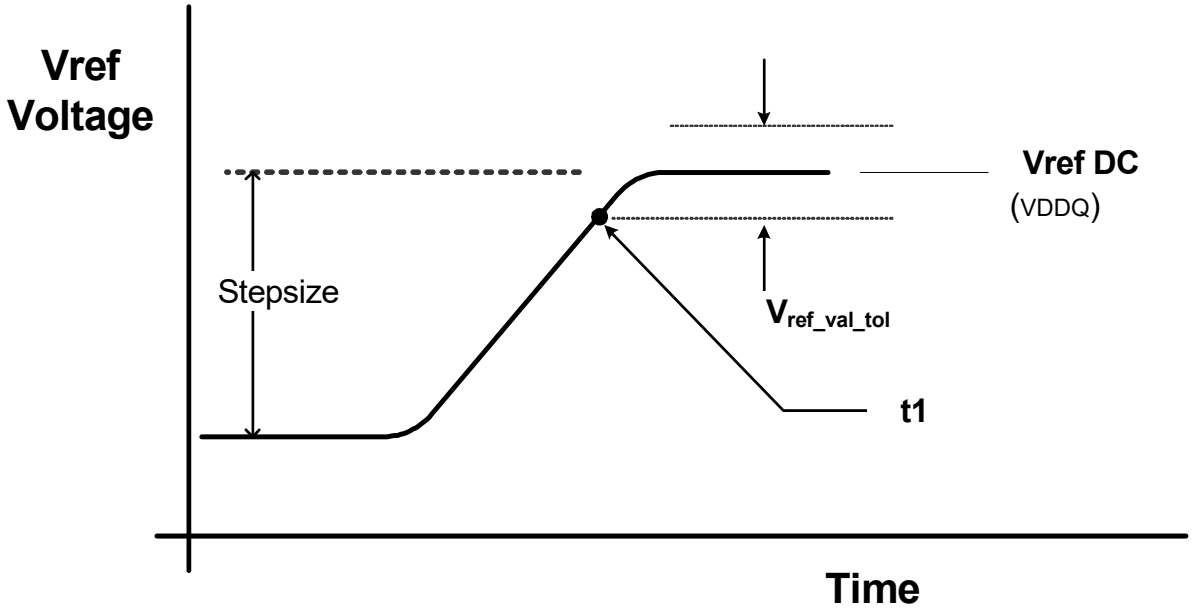


Figure 129 — Vref Step Single Stepsize Increment Case

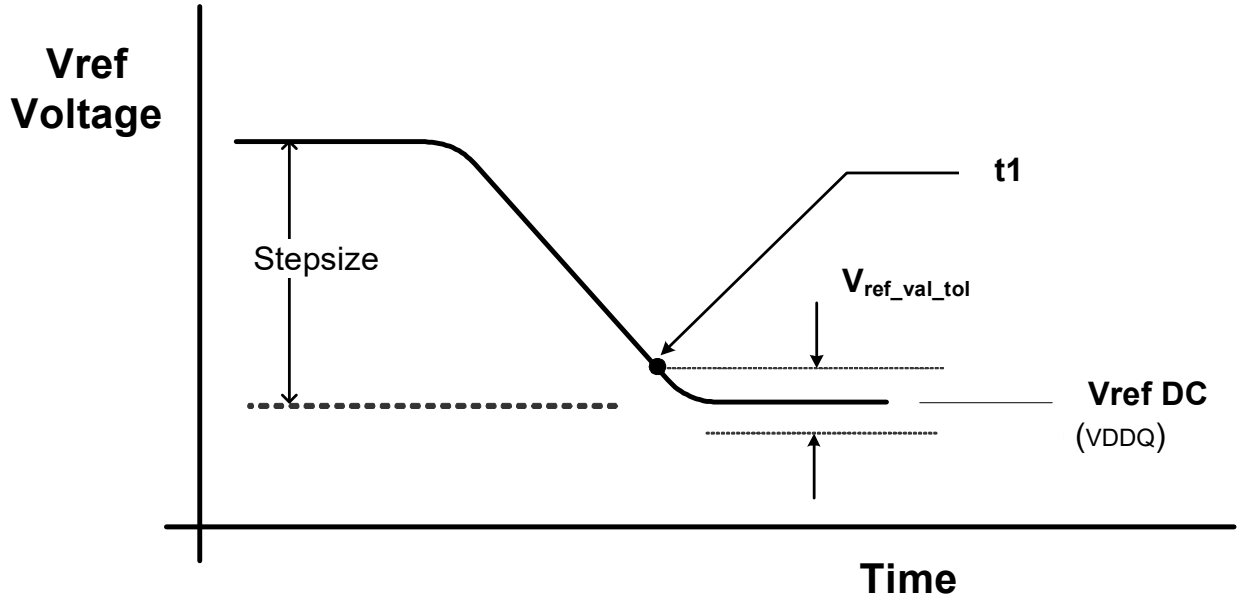


Figure 130 — Vref Step Single Stepsize Decrement Case

4.27 VrefCS Training Specification (cont'd)

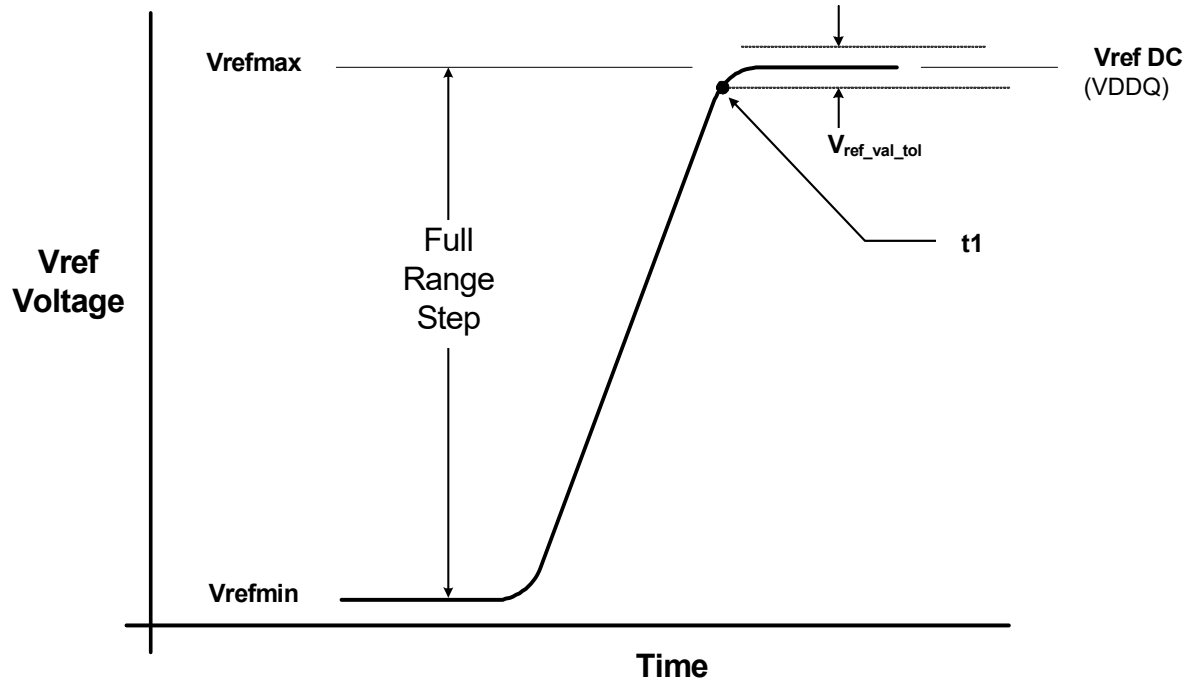


Figure 131 — Vref Full Step from Vrefmin to Vrefmax Case

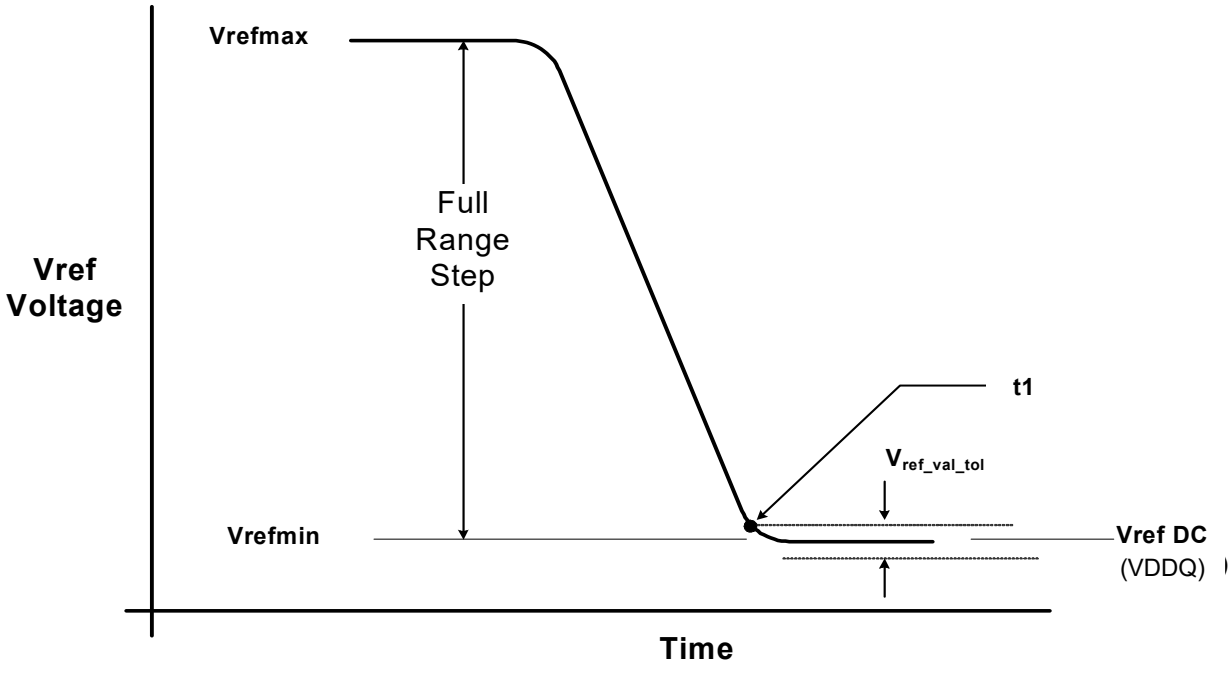


Figure 132 — Vref Full Step from Vrefmax to Vrefmin Case

4.27 VrefCS Training Specification (cont'd)

Table 129 — CS Internal VREF Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
VrefCS Max operating point	V_{refCS_max}	97.5%	-	-	VDDQ	1
VrefCS Min operating point	V_{refCS_min}	-	-	35%	VDDQ	1
VrefCS Stepsize	V_{refCS_step}	0.41%	0.50%	0.59%	VDDQ	2
VrefCS Set Tolerance	$V_{refCS_set_tol}$	-1.625%	0.00%	1.625%	VDDQ	3, 4, 6
	$V_{refCS_set_tol}$	-0.15%	0.00%	0.15%	VDDQ	3, 5, 7
VrefCS Step Time	V_{refCS_time}	-	-	300	ns	8
VrefCS Valid Tolerance	$V_{refCS_val_tol}$	-0.15%	0.00%	0.15%	VDDQ	9

NOTE 1 VrefCS DC voltage referenced to VDDQ_DC.

NOTE 2 VrefCS stepsize increment/decrement range. VrefCS at DC level.

NOTE 3 VrefCS_new = VrefCS_old + n*VrefCS_step; n= number of steps; if increment use "+"; If decrement use "-"

NOTE 4 The minimum value of VrefCA setting tolerance = VrefCS_new - 1.625%*VDDQ. The maximum value of VrefCS setting tolerance = VrefCS_new + 1.625%*VDDQ. For n>4

NOTE 5 The minimum value of VrefCS setting tolerance = VrefCS_new - 0.15%*VDDQ. The maximum value of VrefCS setting tolerance = VrefCSnew + 0.15%*VDDQ. For n< 4

NOTE 6 Measured by recording the min and max values of the VrefCS output over the range, drawing a straight line between those points and comparing all other VrefCS output settings to that line

NOTE 7 Measured by recording the min and max values of the VrefCS output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other VrefCS output settings to that line

NOTE 8 Time from MPC (Apply VREFCA, VREFCS, RTT_CK/CS/CA) command to increment or decrement

NOTE 9 Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. VrefCS valid is to qualify the step times which will be characterized at the component level

4.28 VrefDQ Calibration Specification

The DRAM internal VrefDQ specification parameters are voltage operating range, stepsize, VrefDQ set tolerance, Vref step time, and VrefDQ valid level.

The voltage operating range specifies the minimum required VrefDQ setting range for DDR5 DRAM devices. The minimum range is defined by VrefDQmax and VrefDQmin as depicted in Figure 133.

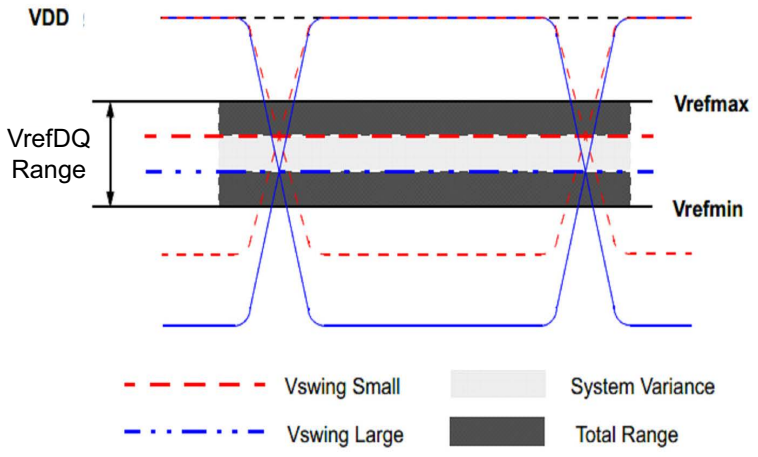


Figure 133 — VrefDQ Operating Range (VrefDQmin, VrefDQmax)

4.28 VrefDQ Calibration Specification (cont'd)

The VrefDQ stepsize is defined as the stepsize between adjacent steps. For a given design the DRAM VrefDQ step size must be within the range specified.

The VrefDQ set tolerance is the variation in the VrefDQ voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for VrefDQ set tolerance uncertainty. The range of VrefDQ set tolerance uncertainty is a function of number of steps n.

The VrefDQ set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max VrefDQ values for a specified range. An illustration depicting an example of the stepsize and VrefDQ set tolerance is shown in Figure 134.

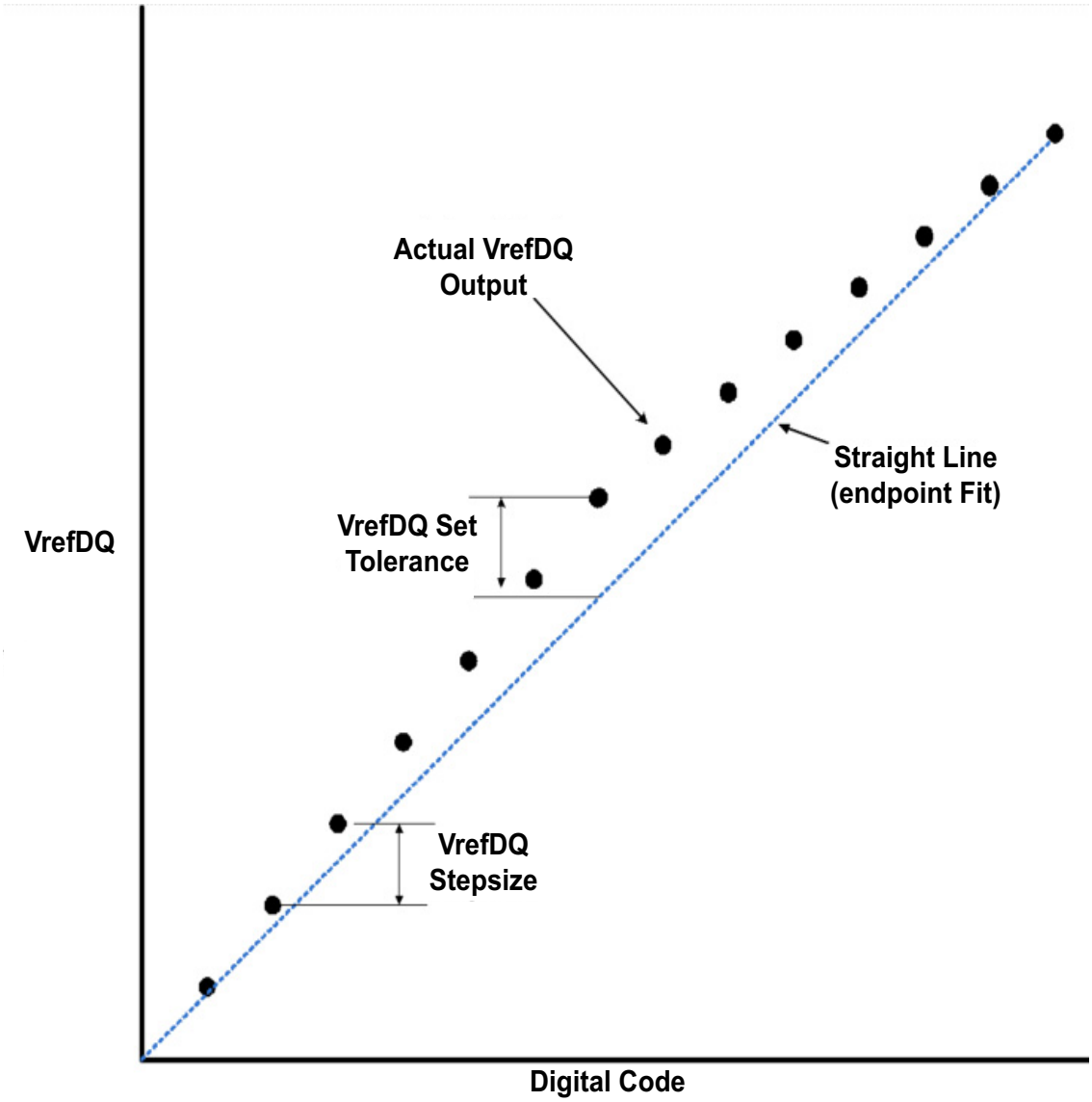


Figure 134 — Example of Vref Set Tolerance (only Max Case is Shown) and Stepsize

4.28 VrefDQ Calibration Specification (cont'd)

The VrefDQ increment/decrement step times are defined by VrefDQ_time. The VrefDQ_time is defined from t0 to t1 as shown in the Figure 135, where t1 is referenced to when the VrefDQ voltage is at the final DC level within the VrefDQ valid tolerance (VrefDQ_val_tol).

The VrefDQ valid level is defined by VrefDQ_val tolerance to qualify the step time t1 as shown in Figure 135. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any VrefDQ increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

t0 - is referenced to the MRW command which updates VrefDQ value

t1 - is referenced to the VrefDQ_val_tol

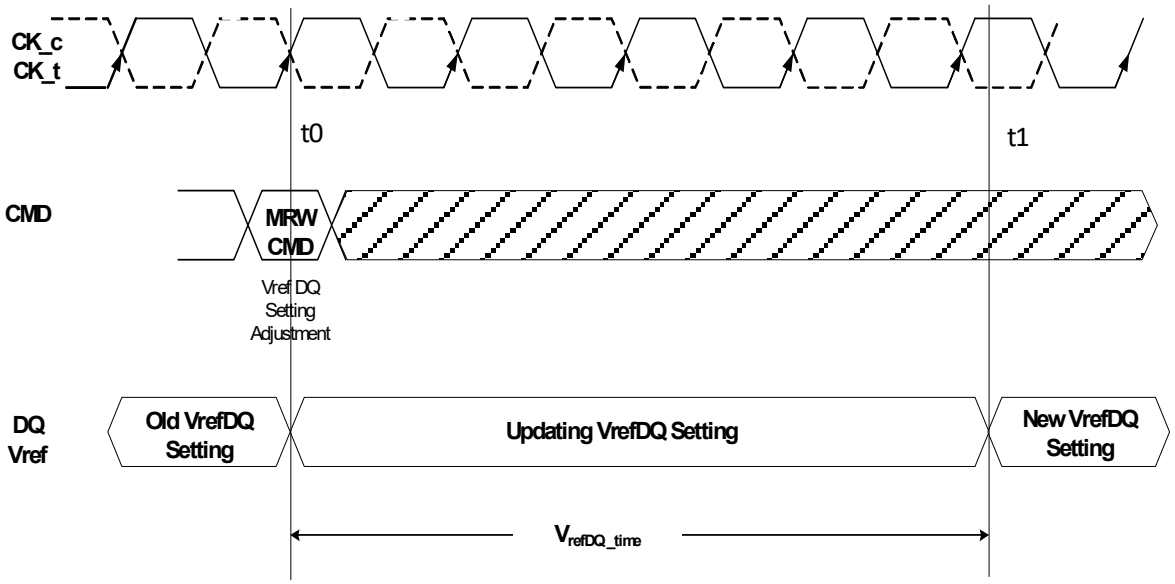


Figure 135 — VrefDQ_Time Timing Diagram

The minimum time required between two MRW commands which update VrefDQ settings is VrefDQ_time.

An MRW command is used to store the global VrefDQ values into the VrefDQ bits of MR10.

Additional per-pin VrefDQ trims are available for programming in MR118, MR126, MR134, ..., MR254, OP[7:4], up to a maximum of +/-3 VrefDQ steps. The combined global and per-pin VrefDQ settings shall never exceed the available VrefDQ range from 35.0% to 97.5%.

4.28 VrefDQ Calibration Specification (cont'd)

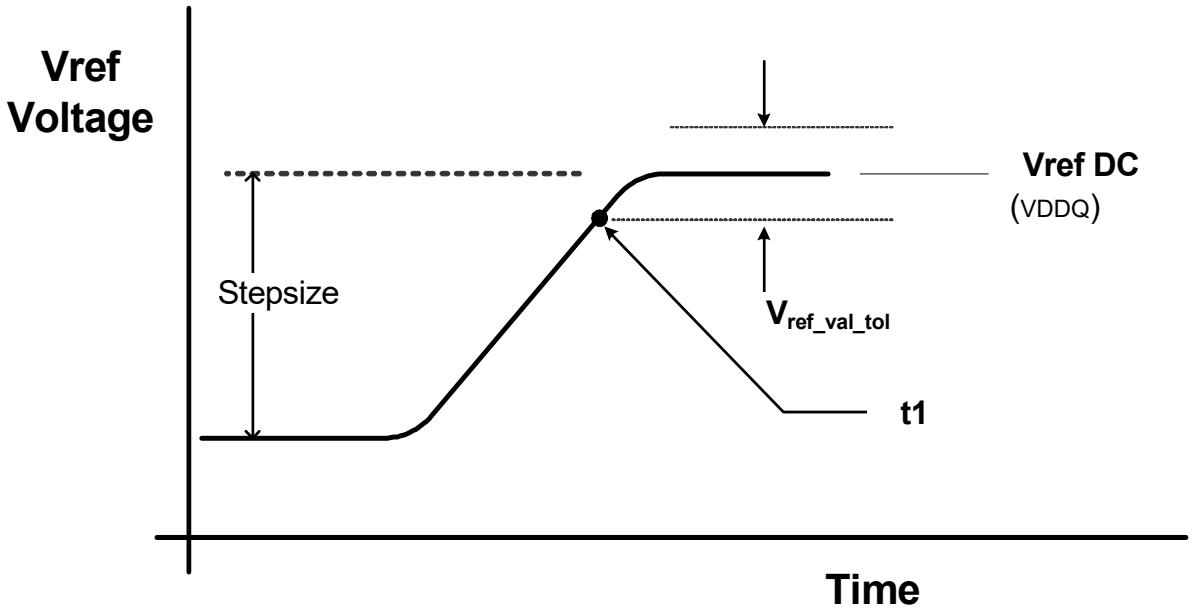


Figure 136 — VrefDQ Step Single Stepsize Increment Case

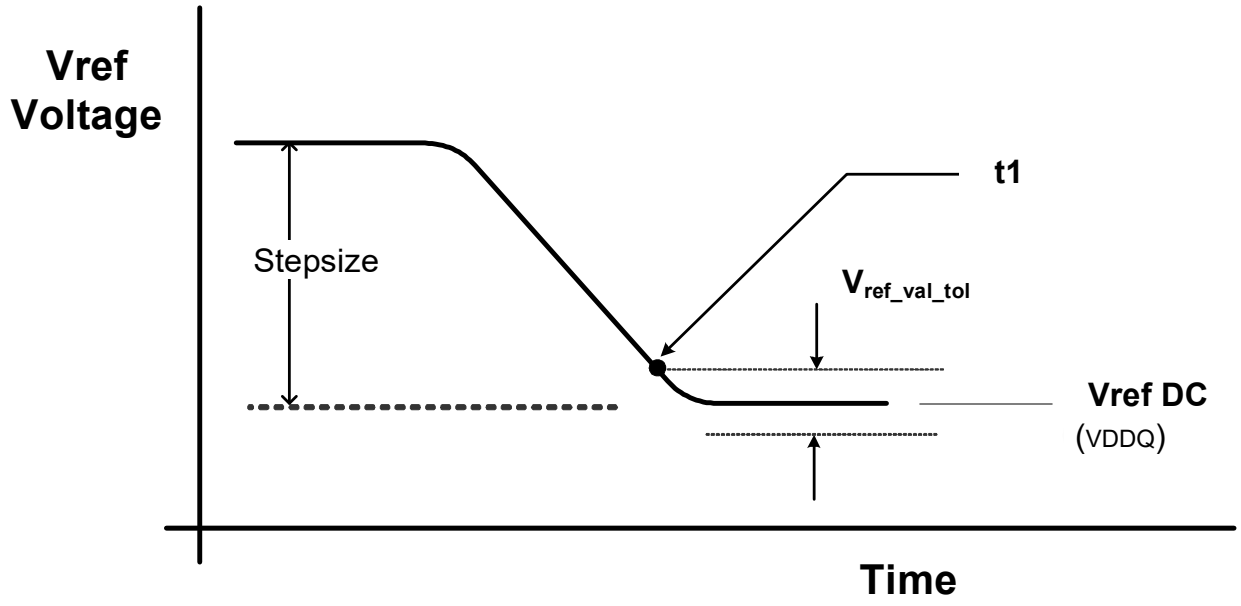


Figure 137 — VrefDQ Step Single Stepsize Decrement Case

4.28 VrefDQ Calibration Specification (cont'd)

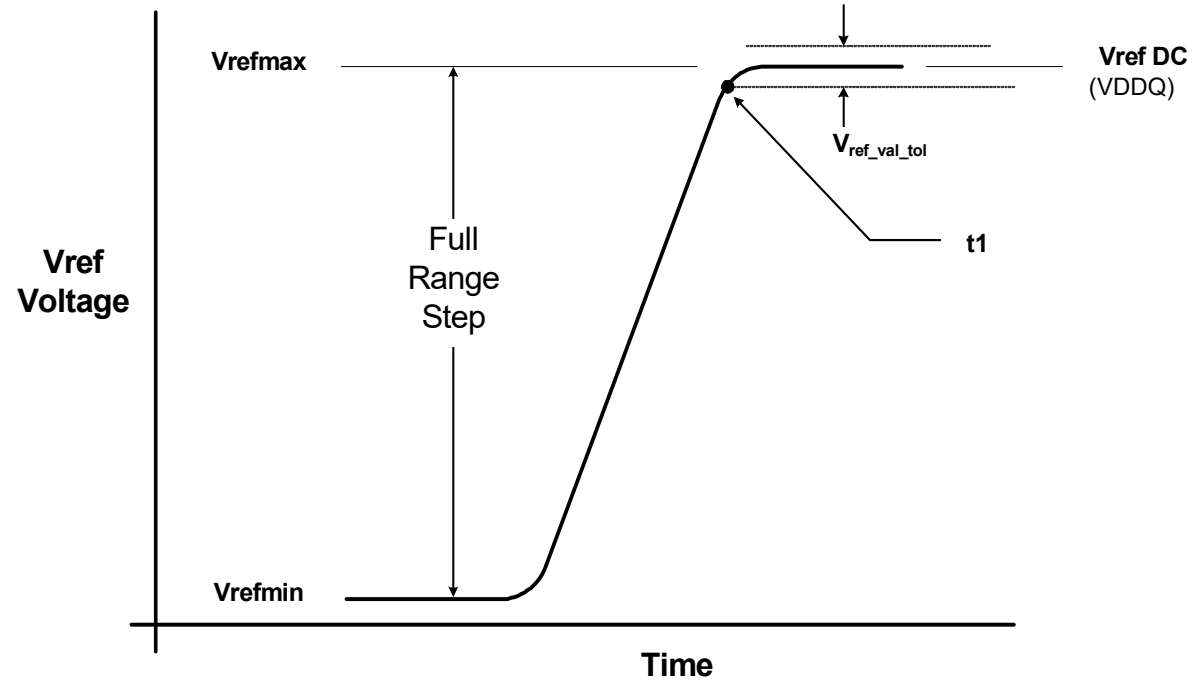


Figure 138 — VrefDQ Full Step from VrefDQmin to VrefDQmax Case

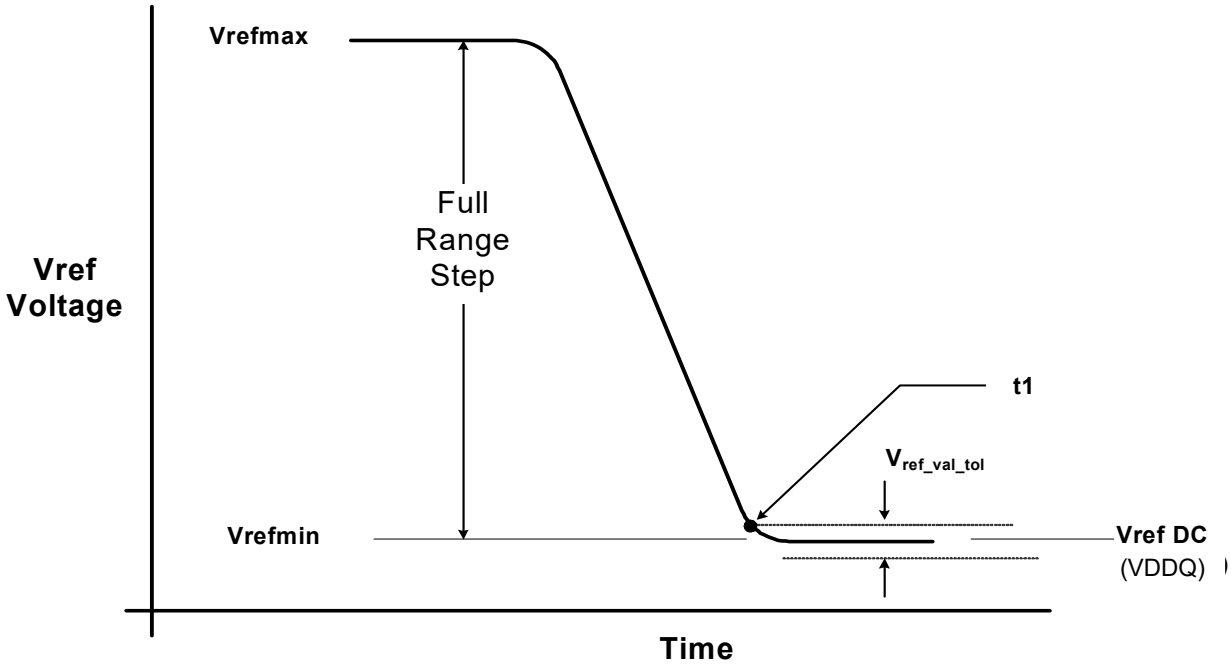


Figure 139 — VrefDQ Full Step from VrefDQmax to VrefDQmin Case

4.28 VrefDQ Calibration Specification (cont'd)

Table 130 — VrefDQ Internal Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
VrefDQ Max operating point	V_{refDQ_max}	97.5%	-	-	VDDQ	1
VrefDQ Min operating point	V_{refDQ_min}	-	-	35%	VDDQ	1
VrefDQ Stepsize	V_{refDQ_step}	0.41%	0.50%	0.59%	VDDQ	2
VrefDQ Set Tolerance	$V_{refDQ_set_tol}$	-1.625%	0.00%	1.625%	VDDQ	3, 4, 6
	$V_{refDQ_set_tol}$	-0.15%	0.00%	0.15%	VDDQ	3, 5, 7
VrefDQ Step Time	V_{refDQ_time}	-	-	150	ns	8, 10
		-	-	500	ns	
VrefDQ Valid Tolerance	$V_{refDQ_val_tol}$	-0.15%	0.00%	0.15%	VDDQ	9

NOTE 1 VrefDQ DC voltage referenced to VDDQ_DC.

NOTE 2 VrefDQ stepsize increment/decrement range. VrefDQ at DC level.

NOTE 3 VrefDQ_new = VrefDQ_old ± n*VrefDQstep; n= number of steps; if increment use "+"; If decrement use "-"

NOTE 4 The minimum value of VrefDQ setting tolerance = VrefDQ_new - 1.625%*VDDQ. The maximum value of VrefDQ setting tolerance = VrefDQ_new + 1.625%*VDDQ. For n>4.

NOTE 5 The minimum value of VrefDQ setting tolerance = VrefDQ_new - 0.15%*VDDQ. The maximum value of VrefDQ setting tolerance = VrefDQ_new + 0.15%*VDDQ. For n≤ 4.

NOTE 6 Measured by recording the min and max values of the VrefDQ output over the range, drawing a straight line between those points and comparing all other VrefDQ output settings to that line.

NOTE 7 Measured by recording the min and max values of the VrefDQ output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other VrefDQ output settings to that line.

NOTE 8 Time from MRW command updating VrefDQ to increment or decrement.

NOTE 9 Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. VrefDQ valid is to qualify the step times which will be characterized at the component level.

NOTE 10 The maximum value of VrefDQ step time = 150 ns for n<16 and 500 ns for n≥16, where n = number of steps.

4.29 Post Package Repair (PPR)

DDR5 supports Fail Row address repair, PPR which allows a simple and easy repair method in a system. Two methods are provided:

(a) Hard Post Package Repair (hPPR) for a permanent Row repair, and

(b) Soft Post Package Repair (sPPR) for a temporary Row repair. DDR5 also optionally supports MBIST PPR (mPPR) which is to be used in conjunction with the MBIST feature to automatically repair failling addresses based on the results of MBIST.

Entry into hPPR, sPPR, MBIST and mPPR is protected through a sequential MRW guard key to prevent unintentional PPR programming. The sequential MRW guard key is the same for hPPR, sPPR, MBIST and mPPR.

The hPPR/sPPR/MBIST/mPPR guard key requires a sequence of four MRW commands to be issued immediately after entering hPPR/sPPR/MBIST/mPPR, as shown in Figure 140. The guard key sequence must be entered in the specified order as stated and shown in the spec below and in Table 131. Any interruptions of the guard key sequence from other MRW/R commands or non-MR commands such as ACT, WR, RD is not allowed. Although interruption of the guard key entry is not allowed, if the guard key is not entered in the required order or is interrupted by other commands, the hPPR/sPPR/MBIST/mPPR mode will not execute and the offending command terminated the hPPR/sPPR/MBIST/mPPR entry may or may not execute correctly however the offending command will not cause the DRAM to lock up. Offending commands which will interrupt hPPR/sPPR/MBIST/mPPR include:

- Any interruptions of the guard key sequence from other MRW/R commands or non-MR commands
- MRW with CW = high
- 2 cycle commands with CS_n low on the 2nd cycle

Additionally, when the hPPR/sPPR/MBIST/mPPR entry sequence is interrupted, subsequent ACT and WR commands will be conducted as normal DRAM commands. If a hPPR/sPPR/MBIST/mPPR operation was prematurely interrupted and/or terminated, the MR23 OP[4:0] must be reset to "0" prior to performing another hPPR/sPPR/MBIST/mPPR operation. The DRAM does not provide an error indication if an incorrect hPPR/sPPR/MBIST/mPPR guard key sequence is entered.

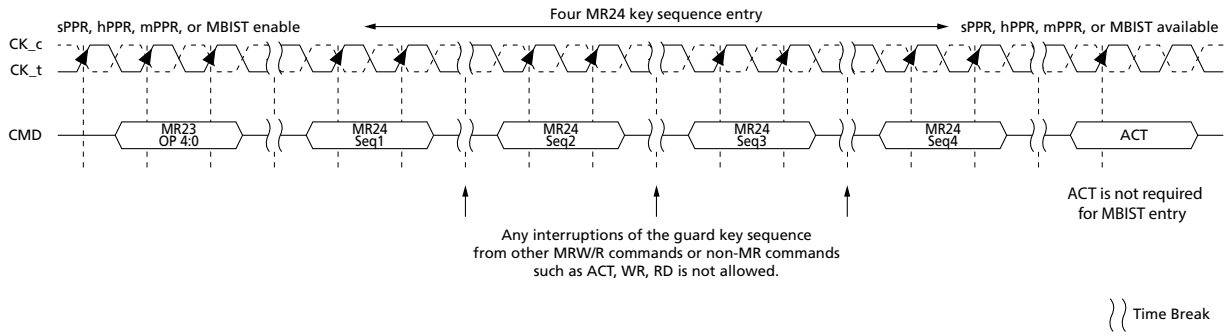


Figure 140 — Guard Key Timing Diagram

Table 131 — Guard Key Encoding for MR24

Guard Keys	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]	Notes
MR24 Seq1	1	1	0	0	1	1	1	1	
MR24 Seq2	0	1	1	1	0	0	1	1	
MR24 Seq3	1	0	1	1	1	0	1	1	
MR24 Seq4	0	0	1	1	1	0	1	1	

4.29 Post Package Repair (PPR) (cont'd)

Table 132 — sPPR vs hPPR vs mPPR

Item	sPPR	hPPR	mPPR	Note
Persistence of Repair	Volatile – Repaired as long as VDD is within Operating Range	Non-Volatile – repair is permanent after the repair cycle.	Non-Volatile – repair is permanent after the repair cycle	Soft Repair is erased when Vdd removed, device reset, or sPPR undo command performed to an unlocked sPPR row
Length of time to complete repair cycle	WL+ 8tCK+tWR	tPGM_hPPRa or tPGM_hPPRb	tSELFREPAIR	
# of Repair elements per repair region [1]	one per BG (Default) one per Bank (Optional)	at least one per BG	Vendor specific	There is no ability to know how many mPPR elements remain in an given repair region. Host must rely on MBIST transparency in MR to determine mPPR success
Simultaneous use of soft and hard repair within a repair region[1]	Previous hPPR are allowed before sPPR	Any outstanding sPPR must be cleared before an hPPR	Any outstanding sPPR must be cleared before MBIST or mPPR	
Repair Command	1 method - WR	1 method - WRA	1 method - WRA	
DRAM retains array data	Yes	No	No	

NOTE 1 Repair region is defined as the address space for which a single repair can be used. A repair region is either a BG or bank, depending on vendor implementation.

4.29.1 Hard PPR (hPPR)

With hPPR, DDR5 can correct at least one row address per Bank Group. The hPPR resource designation (MR54,55,56,57) will indicate the hPPR resource availability, and can be read/checked prior to implementing a repair. It is important to note that hPPR repairs are permanent; the Electrical-fuse cannot be switched back to un-fused states once it is programmed. The controller should prevent unintended the hPPR mode entry and repair. (i.e. During the Command/Address training period). Entry into hPPR is through a register enable, ACT command is used to transmit the bank and row address of the row to be replaced in DRAM. For the non-binary density, an ACT command with invalid row addresses, both MSB and MSB-1 address bits are "HIGH", shall not be allowed since it may consume the PPR resource. After tRCD time, a BL16 WRA command is used to select the individual DRAM through the DQ bits and to transfer the repair address to the DRAM. After program time, and PRE, the hPPR mode can be exited and normal operation can resume.

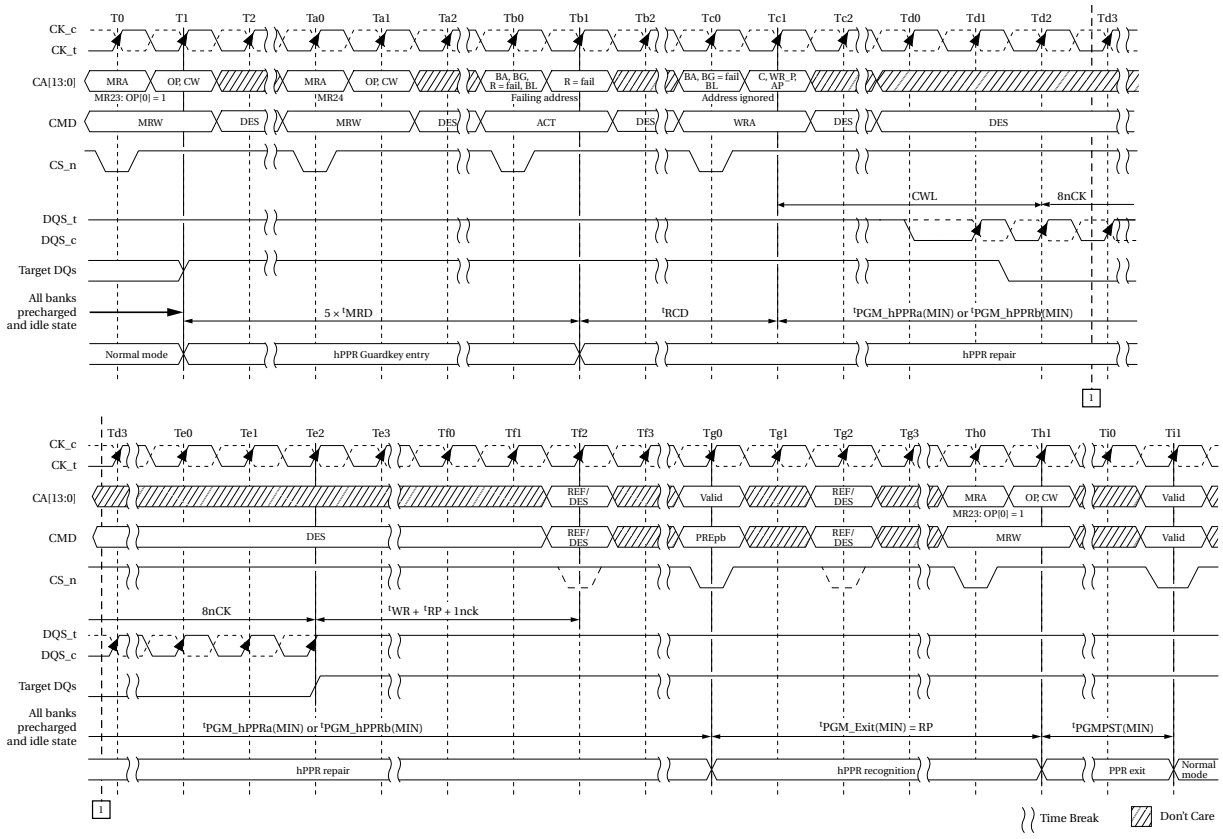
4.29.1.1 hPPR Fail Row Address Repair

1. Since the mode register address operand allows the user to execute hPPR resource, MRR of hPPR resource designation (MR 54, 55, 56, 57) needs to be read. After user's checking the hPPR resource availability of each bank from MRR, hPPR mode can be entered. If the MRR of hPPR resource designation (MR 54, 55, 56, 57) appears to not be available, the host controller should not issue hPPR mode.
2. Before entering 'hPPR' mode, all banks shall be in a precharged and idle state, and CRC Mode must be disabled.
3. Enable hPPR using MR23:OP[0]=1 and wait tMRD.
4. Issue guard key as four consecutive MR24 OP[7:0] MRW commands each with a unique address field OP[7:0]. Each MRW command should be spaced by tMRD.
5. Issue ACT command with the CID bits, Bank Group, Bank and Row fail address. Write data is used to select the individual DRAM in the rank for repair. For non 3DS DRAMs the CID bits need only be Valid, and are ignored by the DRAM.
6. After tRCD, Issue WRA with a valid address. The DRAM will ignore the address given with the WRA command.
7. After WL(WL=RL-2), DQ{3:0] of target DRAM must be LOW for 8tCK. If HIGH is driven to DQ[3:0] of a DRAM for 8tCK, then DRAM does not conduct hPPR and retains data if REF/REFsb command is properly issued. If more than one DRAM shares the same command bus, DRAMs that are not being repaired must have DQ[3:0] driven HIGH for 8tCK. If all of the DQ[3:0] data bits are neither all LOW nor all HIGH for 8tCK, then hPPR mode execution is unknown. For x8 and x16 devices, data bits other than DQ[3:0] are don't cares. Note that a previous versions of the spec required ALL DQs to be high or low, but this was changed to DQ[3:0] to accomodate ECC UDIMMs and SoDIMMs. Check with the DRAM vendor for their specific implementation.
8. Wait tPGM_hPPRa or tPGM_hPPRb to allow DRAM repair at the target row address to occur internally, and then issue PRE command.
9. Wait tPGM_Exit(min) after PRE command to allow DRAM to recognize repaired row address.
10. Exit hPPR by setting MR23:OP[0]=0.
11. DDR5 will accept any valid command after tPGMPST(min).
12. In the case of multiple addresses to be repaired, repeat Steps 3 to 10.
13. For a 3DS device, the target die for the hPPR is selected by the CID[3:0] bits in the ACT, WRA and PRE commands. The CID bits must match in all three commands.

During hPPR mode, REF, REFsb commands are allowed, but array contents are not guaranteed. Upon receiving a REF or REFsb command in hPPR mode, the DRAM may ignore the Refresh operation but will not disrupt the repair operation. Other commands except REF/REFsb during tPGM can cause incomplete repair so no other command except REF is allowed during tPGM.

Once hPPR mode is exited with MR23:OP[0]=0 and tPGMPST, to confirm if target row is repaired correctly, host can verify by writing data into the target row and reading it back.

4.29.1.1 hPPR Fail Row Address Repair (cont'd)



NOTE 1 Allow REFab/REFsb(1X) from WL+8tCK+tWR+tRP+1tCK after WR, but does not guarantee array contents are refreshed during hPPR

NOTE 2 Timing diagram shows possible commands but not all shown can be issued at same time; for example if REF is issued at Te1, DES must be issued at Te2 as REF would be illegal at Te2. Likewise, DES must be issued tRFC prior to PRE at Tf0. All regular timings must still be satisfied.

Figure 141 — hPPR Fail Row Repair

4.29.1.2 Required Timing Parameters

Repair requires additional time period to repair Fail Row Address into Spare Row Address and the following timing parameters are required for PPR.

Table 133 — hPPR Timings

		DDR5-3200 to 9200		Unit	Note
Parameter	**Symbol**	**Min**	**Max**		
hPPR Programming Time: x4/x8	tPGM_hPPRa	1,000	-	ms	
hPPR Programming Time: x16	tPGM_hPPRb	2,000	-	ms	
hPPR RecognitionTime	tPGM_Exit	tRP	-	ns	
hPPR Program Exit and New Address Setting time	tPGMPST	50	-	µs	

4.29.2 Soft Post Package Repair (sPPR)

Soft Post Package Repair (sPPR) is a way to quickly, but temporarily, repair one row address per Bank Group on a DDR5 DRAM device, contrasted to hPPR which takes longer but is permanent repair of a row address. There are some limitations and differences between Soft Repair and a Hard Repair. Entry into sPPR is through a register enable, ACT command is used to transmit the bank and row address of the row to be replaced in DRAM. For the non-binary density, an ACT command with invalid row addresses, both MSB and MSB-1 address bits are “HIGH”, shall not be allowed since it may consume the PPR resource. After tRCD time, a BL16 WR command is used to select the individual DRAM through the DQ bits and to transfer the repair address into an internal register in the DRAM. After a write recovery time and PRE, the sPPR mode can be exited and normal operation can resume. Care must be taken that refresh is not violated for the other rows in the array during soft repair time. Also note that the DRAM will retain the soft repair information inside the DRAM as long as VDD remains within the operating region. If DRAM power is removed or the DRAM is RESET, the soft repair will revert to the un-repaired state. hPPR and sPPR may not be enabled at the same time. sPPR must have been disabled, cleared and unlocked (if DRAM supports optional sPPR undo/lock) prior to entering hPP,R, MBIST or mPPR modes.

With sPPR, DDR5 can repair one Row address per BG (Default) or one row address per bank (Optional). If the hPPR resources for a BG are used up, the bank group will have no more available resources for soft PPR. If a repair sequence is issued to a BG with no repair resources available, the DRAM will ignore the programming sequence.

Note that MR54 through MR57 are NOT updated by an sPPR. The host controller must remember which sPPR resources have been used since the last DRAM Reset.

The DRAM device may optionally support the sPPR Undo and sPPR Lock functions. The sPPR undo command will undo a previous sPPR and cause the sPPR resource to be taken back to its unused condition. The original row will appear back in the memory map at its original location following an sPPR undo. The sPPR Lock function will lock the specific sPPR resource at its current location and not allow another sPPR or an sPPR undo to be performed to that resource.

A row that has been replaced by a spare row need not be refreshed by the DRAM. Likewise a spare row that is not in the memory map, either from never being in the memory map, or from an sPPR undo need not be refreshed by the DRAM. If moving a spare row in and out of the memory map, the host controller is responsible for sending enough Activate commands to any mapped out row to assure any required data retention. The host controller is also responsible for any data copy operations between the original row and spare row.

The host controller should read MR23 OP2 to determine whether the sPPR undo and sPPR lock functions are supported. 0=unsupported, 1=supported.The two features are supported together.

4.29.2.1 sPPR Repair of a Fail Row Address

The following is the procedure of sPPR with WR command. Note that during the soft repair sequence, no refresh is allowed.

1. User should back up the data of the target row address for sPPR in the bank before sPPR execution. The backup data should be one row per bank. After sPPR has been completed, user restores the data in the repaired array.
2. sPPR resources are shared with hPPR. The hPPR resource designation registers (MR 54, 55, 56, 57) should be checked prior to sPPR. If the MRR of hPPR resource designation (MR 54, 55, 56, 57) shows that hPPR resources in the bank that is targeted for sPPR repair is not available, the host controller should not issue sPPR mode.
3. Before entering 'sPPR' mode, all banks shall be in a precharged and idle state. and CRC mode must be disabled.
4. Enable sPPR using MR23 bits "OP[2:1]=01" and wait tMRD.
5. Issue Guard Key as four consecutive MRW commands each with a unique address field OP[7:0] Each MRW command shall be separated by tMRD. The Guard Key sequence is the same as hPPR in Table 131.
6. Issue ACT command with the CID bits, Bank Group, Bank and Row Fail address, Write data is used to select the individual DRAM in the Rank for repair. For non-3DS DRAMs, the CID bits need only be Valid, and are ignored by the DRAM.
7. A WR command is issued after tRCD, with valid column address. The DRAM will ignore the column address given with the WR command.
8. After WL (WL=WL=RL-2), DQ[3:0] of the individual Target DRAM must be LOW for 8tCK. If more than one DRAM shares the same command bus, DRAMs that are not being repaired must have DQ[3:0] driven HIGH for 8tCK. If all of the DQ[3:0] data bits are neither all LOW nor all HIGH for 8tCK, then sPPR mode will be unknown. For x8 and x16 devices, data bits other than DQ[3:0] are don’t cares. Note that a previous versions of the spec required ALL DQs to be high or low, but this was changed to DQ[3:0] to accomodate ECC UDIMMs and SoDIMMs. Check with the DRAM vendor for their specific implementation.
9. Wait tPGM_sPPR(min) for the internal repair register to be written and then issue PRE to the Bank.
10. Wait tRP after PRE command to allow the DRAM to recognize repaired Row address.
11. Exit sPPR with setting MR23 bit "OP[2:1]=00" and wait tMRD.
12. sPPR can be performed without affecting the hPPR previously performed provided a row is available in that repair region. When more than one sPPR request is made to the same repair region, the most recently issued sPPR address would replace the early issued one associcated with given bank and row addresses. In the case of conducting soft repair address in a different repair region, repeat step 4 to 11. During a soft repair, refresh command is not allowed between sPPR MRS entry and exit.

4.29.2.1 sPPR Repair of a Fail Row Address (cont'd)

For a 3DS device, the target die for the sPPR is selected by the CID[3:0] bits in the ACT, WR, and PRE commands. The CID bits must match in all three commands.

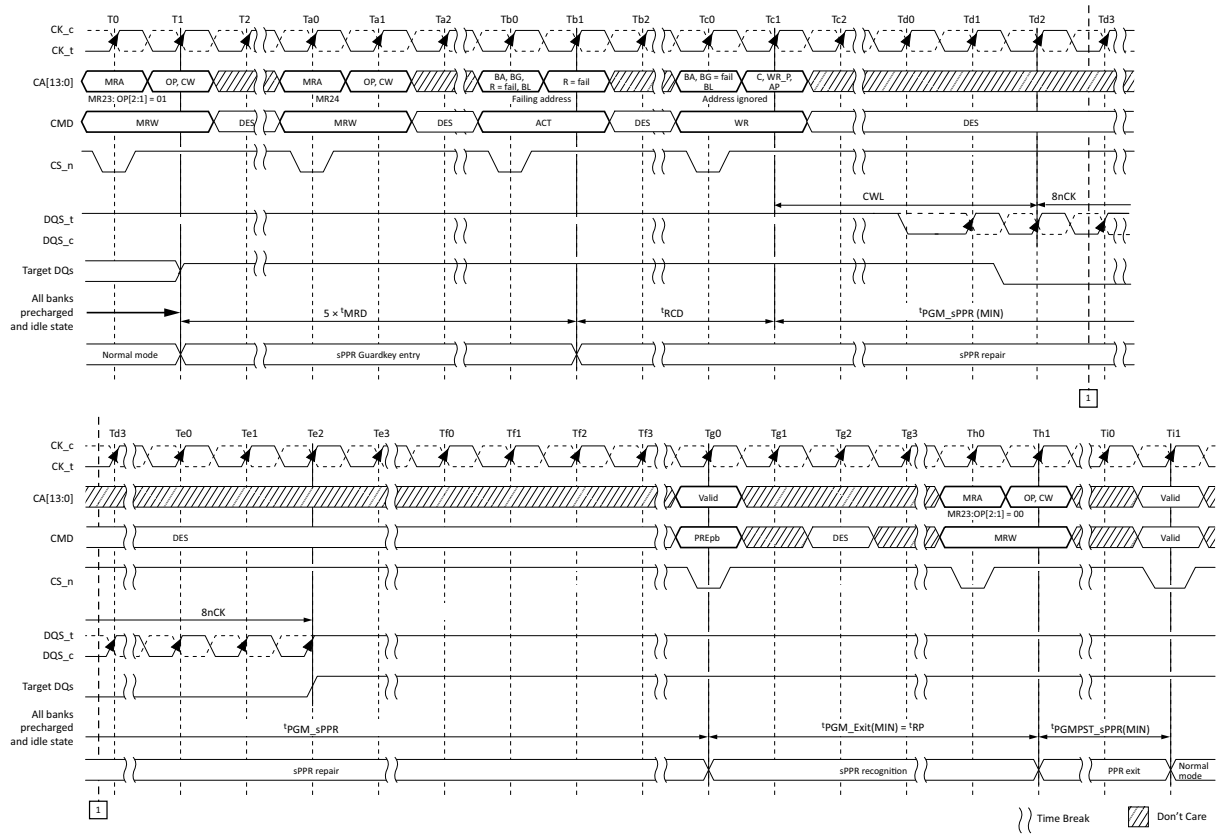


Figure 142 — sPPR Fail Row Repair

Table 134 — sPPR Timings

		DDR5-3200 to 9200		Unit	Note
Parameter	**Symbol**	**Min**	**Max**		
sPPR Programming Time: x4/x8, x16	tPGM_sPPR	WL+8tCK +tWR	-	tCK	
sPPR Exit Recognition Time	tPGM_Exit	tRP	-	ns	
sPPR Exit and New Address Setting time	tPGMPST _sPPR	tMRD	-	ns	

4.29.2.2 sPPR Undo

sPPR Undo is a method of setting the sPPR resource back to its unused state, as it was following Reset. It follows the exact same protocol as the sPPR sequence, but with MR23 OP[2:1] set to 10. The host controller must send the same CID bits, BG bits, Bank bits, and row address in the Activate command as it did for the most recent sPPR for this resource. The DRAM may ignore the bank and row address bits if it so chooses, as the CID and BG bits may be enough to uniquely identify the sPPR resource depending on number of repair elements. For non 3DS DRAMs the CID bits need only be Valid, and are ignored by the DRAM. Any cases where the CID bits, BG bits, Bank bits or row address do NOT match that of the most recent sPPR to this resource will result in sPPR undo operation not being guaranteed. Any required copying of data is the host controller's responsibility.

Following an sPPR Undo, a later sPPR may be done to assign the resource to a new or the same location. Data is retained in the sPPR resource, but it need not be refreshed by the DRAM. If the host controller requires the data to remain valid, it must send enough ACT commands to the row while it is mapped in to guarantee the data.

This feature is optional. The sPPR undo function should only be done to DRAMs in which MR23 bit 2 is read as a 1 upon an MRR.

4.29.2.3 sPPR Lock

sPPR Lock allows an sPPR resource to be locked in place. Locks are done to sPPR resources individually. Following an sPPR Lock any sPPR or sPPR undo is blocked to that spare resource. A hardware reset or power cycle must be done to undo the lock. The hardware reset or power cycle must also be done before any hPPR operation can be done if any sPPR resources are locked.

The sPPR Lock uses the same protocol as the sPPR function except that MR23 OP[2:1] is set to 11. The Activate command must contain the CID bits, BG bits, bank bits and row address of the most recent sPPR for that resource. The DRAM may ignore the bank and row address bits if it so chooses, as the CID and BG bits may be enough to uniquely identify the sPPR resource depending on number of repair elements. For non 3DS DRAMs the CID bits need only be Valid, and are ignored by the DRAM. Any cases where the CID bits, BG bits, Bank bits or row address do NOT match that of the most recent sPPR to this resource will result in sPPR Lock operation not being guaranteed.

This feature is optional. The sPPR lock function should only be done to DRAMs in which MR23 bit 2 is read as a 1 upon an MRR.

4.30 MBIST/mPPR

DDR5 devices can support optional Memory Built-In Self Test (MBIST) and Memory Built-In Self Test-Post Package Repair (mPPR) to help with hard failures such as single-bit or multi-bit failures in a single device so that weak cells can be scanned and repaired during the initialization phase. There are two distinct associated phases, MBIST (Self-test phase) and mPPR (Self-repair phase). During MBIST, the DRAM will use vendor specific patterns to test the memory array, detect hard failures. During mPPR, addresses of hard-failures will be automatically repaired out. MBIST and mPPR may only be entered from the All Banks Idle state. MBIST may be ran any time after the device has been properly initialized according to section “Power-up Initialization Sequence”, but must be run prior to mPPR. After MBIST completes, MR22 transparency must be read. If transparency says that fails remain and the controller chooses to run mPPR, it must perform mPPR immediately after the DRAM transparency is read.

mPPR resources are separated from normal hPPR/sPPR resources. mPPR resources will be used for initial scan and repair, and hPPR/sPPR resources still must satisfy the number of repair elements as specified in Table 127. Once MBIST is done, DRAM will update the MBIST/mPPR transparency status in MR22:OP[2:0]. Detailed transparency status is described in 3.5.24.

There are two timings associated with MBIST/mPPR, tSELFTEST and tSELFREPAIR. The time to test the array and detect failures is defined as tSELFTEST. The time to repair failures detected in the previous MBIST run using mPPR is defined as tSELFREPAIR. Multiple iterations of MBIST and mPPR may be required to repair all failures, and the transparency status will inform the host of this.

For 3DS devices, MBIST must be run on each logical rank in the 3DS package independently by configuring MR14:OP[3:0] prior to invoking MBIST. After MBIST is run on a single logical rank, MBIST/mPPR transparency in MR22 must subsequently be read to determine whether mPPR is needed on that logical rank. The controller may choose to run MBIST on all ranks before performing mPPR on all ranks sequentially, or it may perform MBIST on one rank followed by mPPR to the same rank, proceeding through each logical rank.

4.30.1 MBIST Sequence

The controller is required to issue an MRW command to enter the MBIST operation. Controller sets the MR23:OP[4] to HIGH, subsequently followed by the MR24 commands for the guard key, then the DRAM enters MBIST operation and the DRAM drives ALERT_n to LOW. Once the MBIST is completed, the DRAM drives ALERT_n to HIGH to notify the controller that this operation is completed. MBIST/mPPR transparency will be updated in MR22, and will signify to the host whether mPPR must be performed to repair any found fails. If mPPR is required, the controller will follow the mPPR sequence described in section 4.30.2, and transparency will be updated once mPPR is complete. DRAM data will not be guaranteed after MBIST PPR operation. During MBIST mode, only DESELECT command is allowed. The DQ/DQS may either float (Hi-Z) or perform RTT_PARK/DQS_RTT_PARK termination during tSELFTEST depending on vendor specific implementation, while CA/CS/CK ODT will remain unchanged from its programmed state prior to MBIST.

Table 135 — MBIST Timing Parameter

Parameter	Density			Min/Max	Unit	Notes
	8 Gb / 16 Gb	24 Gb	32 Gb			
tSELFTEST	9	14	19	Max	s	1
NOTE 1 tSELFTEST applies per logical-rank.						

MBIST procedure is detailed in Figure 143.

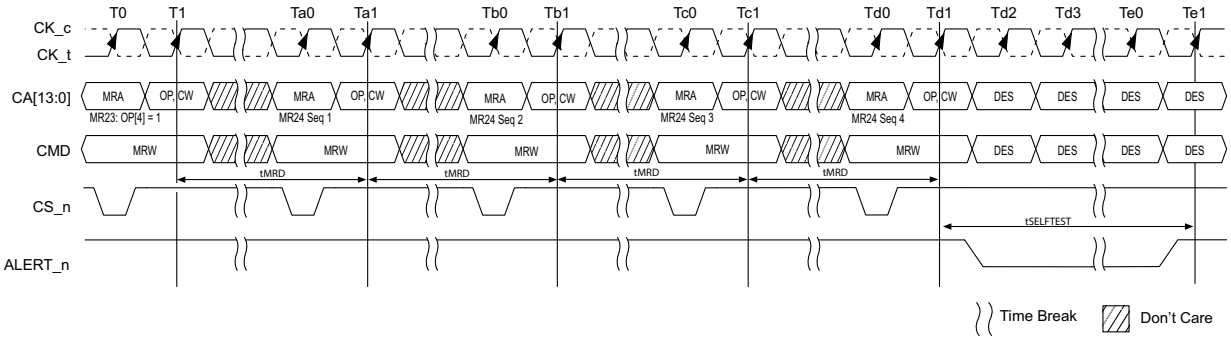


Figure 143 — MBIST Procedure

4.30.2 mPPR Sequence

MBIST-PPR (mPPR) may be used after MBIST in order to repair failures found during the self-test phase. mPPR may only be performed after MR22 MBIST/mPPR transparency is read, and MR22 MBIST/mPPR transparency must be read after mPPR completes in order to determine if an additional mPPR or MBIST is required. If fails remain after the read of MR22 transparency, the mPPR sequence is described as follows:

1. All banks shall be in a precharged and idle state, and CRC mode must be disabled prior to entering mPPR mode.
2. Enable mPPR using MR23:OP[3]=1 and wait tMRD.
3. Issue guard key sequence as four consecutive MR24:OP[7:0] MRW commands each with a unique address field OP[7:0]. Each MRW command must be spaced by tMRD.
4. Issue ACT command with valid address. The DRAM will ignore the address given with the ACT command. Write data is used to select the individual DRAM in the rank for repair. For 3DS devices, CID on the ACT must be set to the same value programmed in MR14:OP[3:0] which determined which logical rank MBIST was last run on.
5. After tRCD, issue WRA with a valid address. The DRAM will ignore the address given with the WRA command. For 3DS devices, CID on the WRA must be set to the same value programmed in MR14:OP[3:0] which determined which logical rank MBIST was last run on.
6. After WL (WL=RL-2), DQ[3:0] of the individual target DRAM must be LOW for 8tCK. Only DRAMs in which most recently have had an MR22 transparency result of 001_B may be considered “target DRAMs”. If more than one DRAM shares the same command bus, DRAMs that are not being repaired must have DQ[3:0] driven HIGH for 8tCK. If all of the DQ[3:0] data bits are neither all LOW or all HIGH for 8tCK, the mPPR mode execution is unknown. For x8 and x16 devices, data bits other than DQ[3:0] are don’t cares. Note that a previous versions of the spec required ALL DQs to be high or low, but this was changed to DQ[3:0] to accomodate ECC UDIMMs and SoDIMMs. Check with the DRAM vendor for their specific implementation.
7. Wait tSELFREPAIR to allow DRAM to self repair the address(es) identified internally by MBIST, and then issue a PREab command.
8. Wait tPGM_exit after PREab command to allow DRAM to update MR22 transparency status.
9. Exit mPPR by setting MR23:OP[3]=0. Wait tPGMPST.
10. Read MR22 transparency status.
11. If additional fails remain, the controller may repeat steps 2-10. If no fails remain or the controller chooses not to perform additional mPPR, the DRAM may continue to the next planned operation.

4.30.2 mPPR Sequence (cont'd)

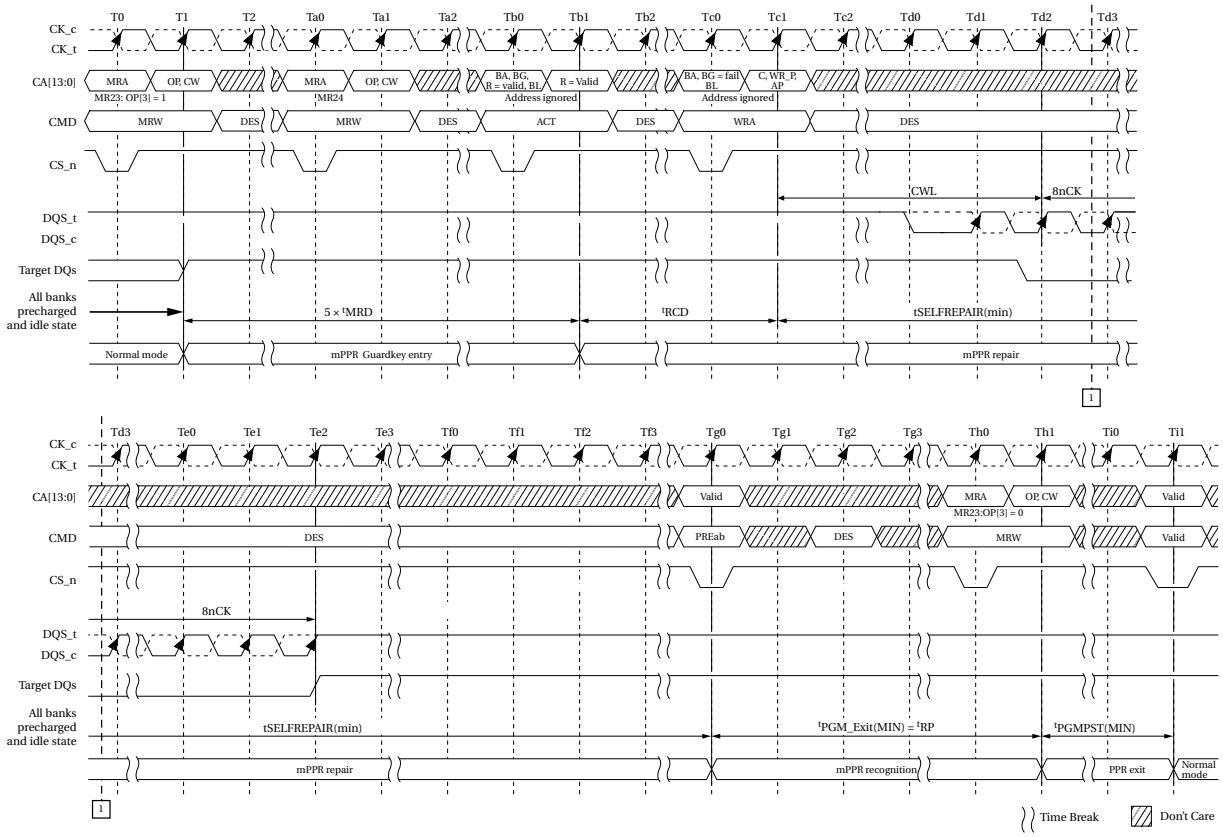
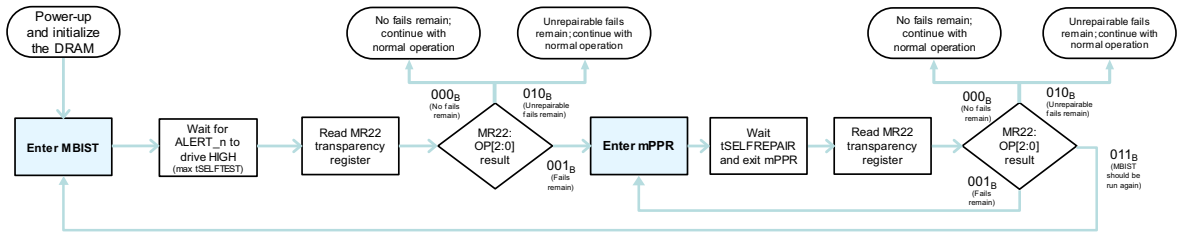


Figure 144 — mPPR Row Repair

Table 136 — mPPR Timings

Parameter		DDR5-3200 to 9200		Unit	Notes
	Symbol	Min	Max		
mPPR programming time: x4, x8, x16	tSELFREPAIR	1000	-	ms	

Figure 145 contains a detailed flow chart of the MBIST/mPPR procedure.



NOTE 1 mPPR may only be performed after an MR22 transparency result of 001_B.

NOTE 2 011_B = "MBIST should be run again" indicates that some fails were repaired with mPPR, but MBIST should be run again to load internal fail addresses for mPPR.

NOTE 3 010_B = "Unrepairable fails remain" indicates that there are not enough mPPR elements remaining to repair fail addresses latched during MBIST. It may be updated in MR22 after either MBIST or mPPR, depending on vendor implementation.

Figure 145 — MBIST/mPPR Flow Chart

4.31 Decision Feedback Equalization

4.31.1 Introduction

At data rates >= 2933 MT/s, signal degradation due to Inter Symbol Interference (ISI) is expected to increase and the data eye at the DRAM ball is expected to be closed. Since the memory channel is very reflective due to the many impedance mismatched points that exist along the memory subsystem, ISI due to reflections are expected to increase. Traditional methods of characterizing the Receiver using the input eye mask is no longer sufficient. DDR5 requires equalization to help improve (or open up) the data eyes after the data is latched by the receiver. A 4-tap DFE is chosen to help equalize the DQ signals without amplifying the noise due to insertion loss and reflections, which is a common side effect of other equalization techniques (example CTLE). For ISI correction to occur, the Global DFE Gain and Tap (MR111) and per-pin DFE Gain and Tap (MR112-MR252) bits shall be enabled and properly configured for data rates >= 2933 MT/s. When the DFE is enabled, the DQs shall be high for a minimum of 4UI prior to the first Write data bit to ensure proper DFE synchronization. Figure 146 shows an example of a memory subsystem with DFE circuit included on the DRAM.

For systems supporting data channel margins where the DFE is not required to improve signaling, the DFE can be disabled. Also at the 1980-2100 MT/s data rates, the DRAM's DFE shall be disabled. Setting either the Global DFE Gain and Tap 1-4 Enable bits to "Disable" or setting all DFE Gain and Tap 1-4 Bias bits to "Step 0" will disable the DFE.

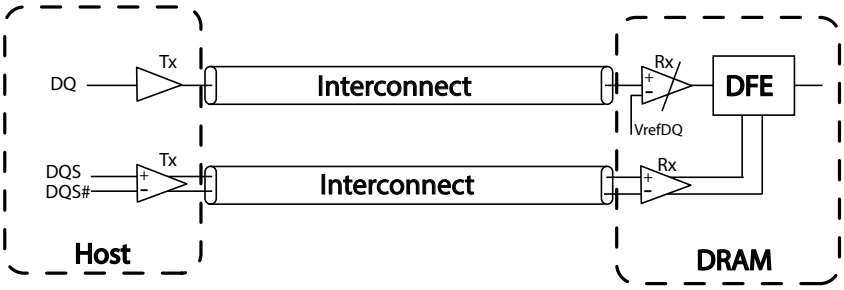
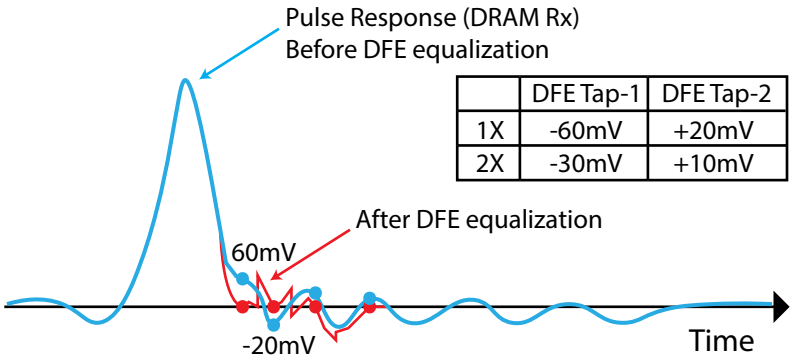


Figure 146 — Example of Memory Subsystem with DFE Circuit on the DRAM

4.31.2 Pulse Response of a Reflective Memory Channel

A reflection dominated channel such as those found in a memory subsystem is anticipated to have substantially reduced data eye at the DRAM ball due to the effects of insertion loss and reflections. Figure 147 represents how a pulse response of a very reflective channel might look like. The attenuation as well as the ringing of the signal can cause the data eye to close at the DRAM ball. Moreover, the ringing can impact future bits that are being sent into the channel, i.e., if the pulse response is for bit n, then the ringing from bit n can impact the signal integrity of future bits n+1, n+2, n+3, n+4, etc. Putting it another way, the signal integrity of any bit, for example bit n, can be impacted by the signals of the previous bits n-1, n-2, n-3, n-4, etc.



	DFE Tap-1	DFE Tap-2
1X	-60mV	+20mV
2X	-30mV	+10mV

Figure 147 — Example of Pulse Response of a Reflective Channel

4.31.3 Components of the DFE

The 4-tap DFE subsystem consists of a gain amplifier, a DFE summer, 4 DQ slicers (also called Taps) with outputs that loop back to the DFE summer, and a coefficient multiplier for each Tap (Figure 148). The gain control of the front end is used to ensure that the cursor or the current bit is in a congruent relationship with the ISI correction required for the channel. The taps T1, T2, T3, and T4 coefficients provide the corrections needed to the current bit by adding or subtracting the effects of ISI of the previous bits.

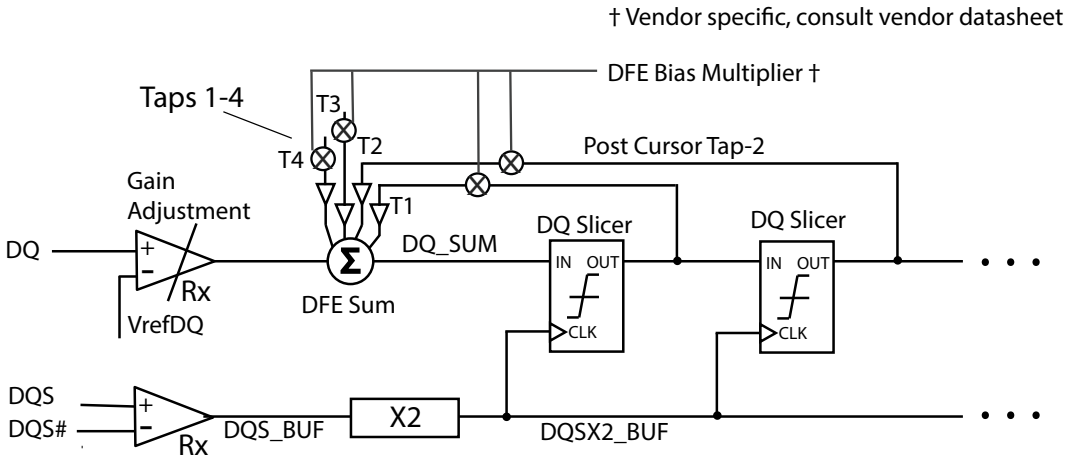


Figure 148 — 4-Tap DFE Example

The Mode Registers shown in Table 137 and Table 138 are used by the memory controller to set the strengths of the gain amplifier and the strengths of the correction of the Taps to adapt the ISI cancellation in accordance with the channel performance. Optimal values used for the strengths of the gain amplifier and of the Taps are system dependent, and are usually obtained through a combination of simulations, platform characterizations, and other methods.

4.31.3 Components of the DFE (cont'd)

Table 137 — Min/Max Ranges for the DFE Gain Adjustment

Description	DDR5 3200-9200			Unit	Notes
	Min	Typ	Max		
DFE Gain Bias Max	6	-	-	dB	1, 2, 3, 4
DFE Gain Bias Min	-	-	-6	dB	1, 2, 3, 4
DFE Gain Bias Average Step Size		2		dB	1, 2, 3, 4
DFE Gain Bias DNL	-1	-	1	dB	1, 2, 3, 4
DFE Gain Bias INL	-1	-	1	dB	1, 2, 3, 4
DFE Gain Bias Time	tDFE	-	-	ns	1, 2, 3, 4

NOTE 1 All parameters are defined over the Vref ranges from 0.5*VDDQ to 0.9*VDDQ
NOTE 2 DFE Gain Bias are for all voltage and temperature range
NOTE 3 These values are defined over the entire voltage and temperature range
NOTE 4 These parameters are suggested to evaluate relative ratio of DFE gain bias settings, and absolute values of all parameters are not subject to silicon validation nor production test.

Table 138 — Min/Max Ranges for the DFE Tap Coefficients

Description	DDR5 3200-9200			Unit	Notes
	Min	Typ	Max		
DFE Tap-1 Bias Max	50	-	-	mV	1, 2, 4, 5, 7
DFE Tap-1 Bias Min	-	-	-200	mV	1, 2, 4, 6, 7
DFE Tap-2 Bias Max	75	-	-	mV	2, 4, 5, 7
DFE Tap-2 Bias Min	-	-	-75	mV	2, 4, 6, 7
DFE Tap-3 Bias Max	60	-	-	mV	2, 4, 5, 7
DFE Tap-3 Bias Min	-	-	-60	mV	2, 4, 6, 7
DFE Tap-4 Bias Max	45	-	-	mV	2, 4, 5, 7
DFE Tap-4 Bias Min	-	-	-45	mV	2, 4, 6, 7
DFE Tap Bias Average Step Size	-	5	-	mV	2, 3, 4, 7
DFE Tap Bias DNL	-2.5	-	+2.5	mV	2, 3, 4, 7
DFE Tap Bias INL	-2.5	-	+2.5	mV	2, 3, 4, 7
DFE Tap Bias Step Time	tDFE			ns	2, 3, 4

NOTE 1 As speed increases, the impact of loss from the channel makes the bias range of the first cursor asymmetric
NOTE 2 Values are defined for the entire voltage, temperature and the Rx Vref range from 0.5*VDDQ to 0.9*VDDQ.
NOTE 3 Values are identical for Taps 1-4.
NOTE 4 These parameters are suggested to evaluate relative ratio of DFE Taps 1~4, and absolute values of all parameters are not subject to silicon validation nor production test.
NOTE 5 For the pulse response shown in Fig 118 (...000010000... pulse pattern), a positive value corrects a negative post-cursor by setting the DFE tab bias sign bit (MR113~116, OP[6]) to '0' to apply a positive correction.
NOTE 6 For the pulse response shown in Fig 118 (...000010000... pulse pattern), a negative value corrects a positive post-cursor by setting the DFE tab bias sign bit (MR113~116, OP[6]) to '1' to apply a negative correction. For example, in a memory channel where the ISI during the first post-cursor is dominated by bandwidth loss, the expected tap-1 bias sign bit will be set to '1'.
NOTE 7 Users refer to DRAM supplier's datasheet to check the multiplier which is applied to the DFE Tap Bias setting (MR113, MR114, MR115, etc.) for total DFE feedback swing implemented in hardware.

4.31.3 Components of the DFE (cont'd)

The method to measure INL and DNL for both DFE gain and DFE taps will be the subject of future ballots.

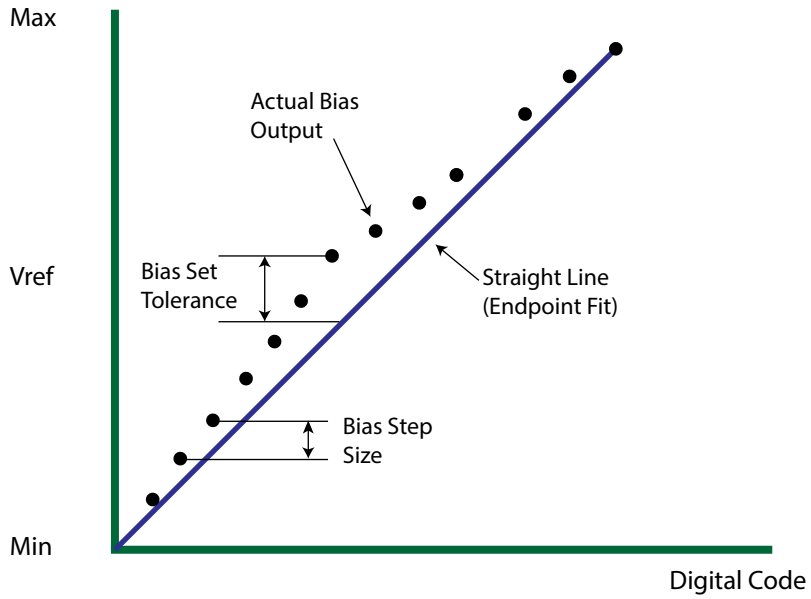


Figure 149 — Example to be Revised for INL/DNL

The DRAM may implement 1-way interleave, 2-way interleave, or 4-way interleave 4-tap DFE memory circuitry. The 1-way interleaved 4-tap DFE architecture (Figure 150) requires a strobe multiplier, which is at Nyquist rate, and the output of the DQ slicer runs at same speed as received data.

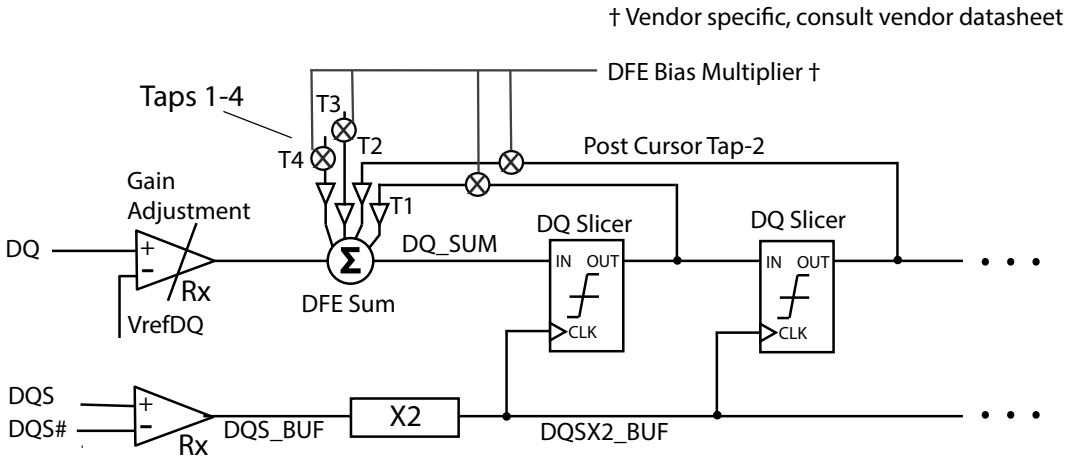


Figure 150 — 1-Way Interleave 4-Tap DFE Example

4.31.3 Components of the DFE (cont'd)

A 2-way interleaved 4-tap DFE architecture (Figure 151) can use the strobe as is. In this case, the output of the DQ slicer runs at half the speed as received data.

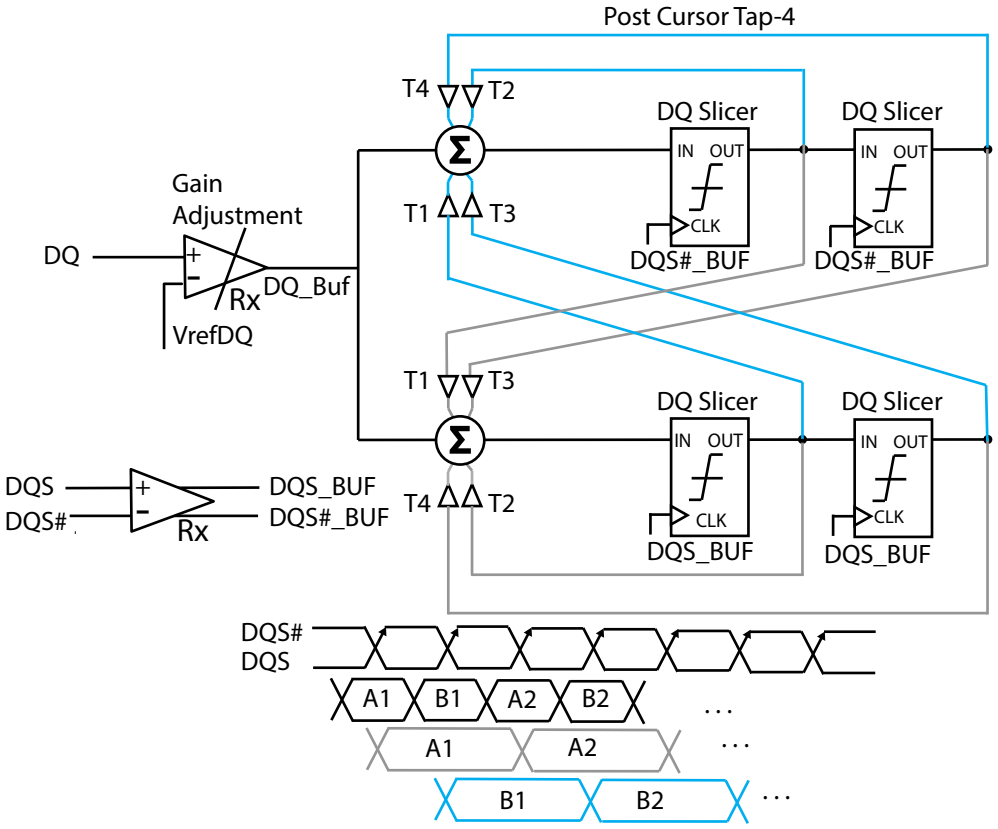


Figure 151 — 2-Way Interleave 4-Tap DFE Example

4.31.3 Components of the DFE (cont'd)

A 4-way interleaved 4-tap DFE architecture (Figure 152) requires a divided clock. In this case, the output of the DQ slicer runs at 1/4 the speed as received data.

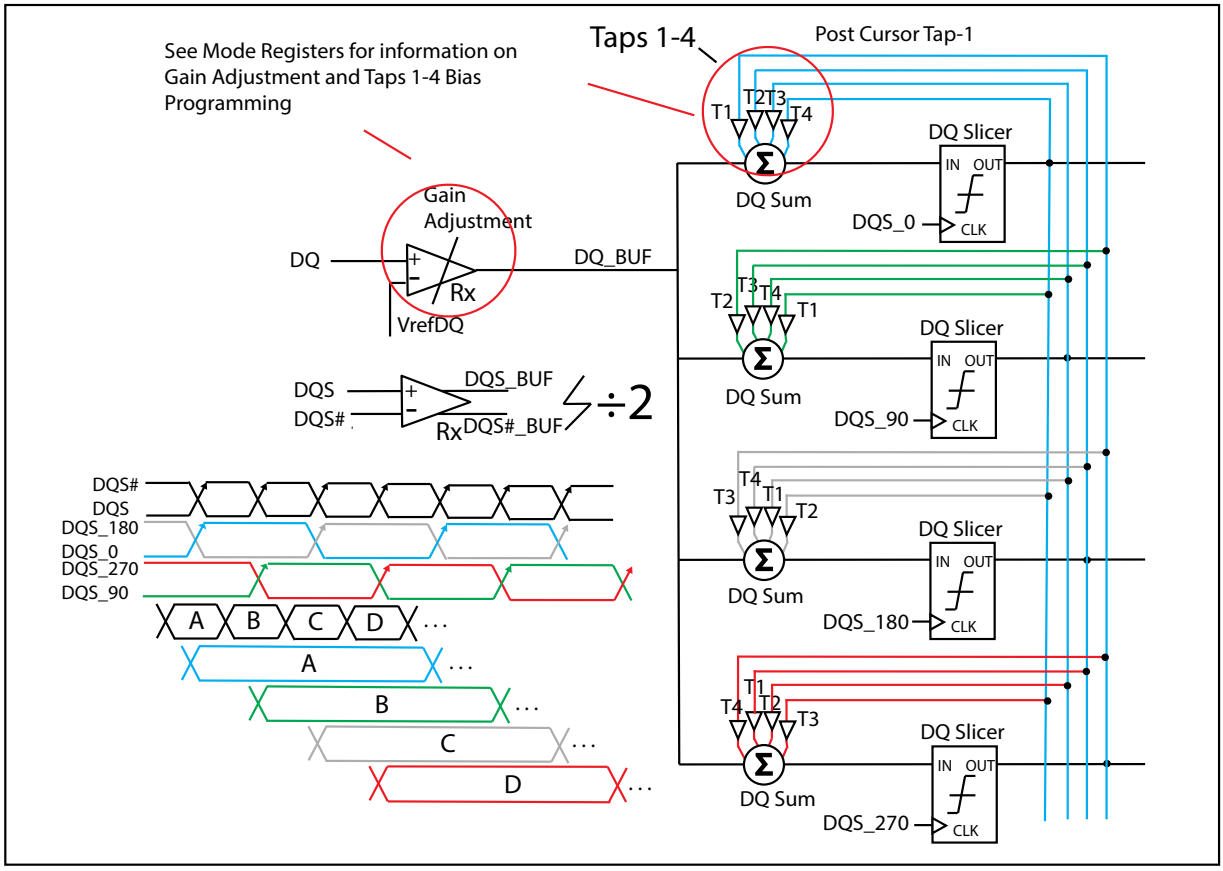


Figure 152 — 4-Way Interleave 4-Tap DFE Example

4.32 DQS Interval Oscillator

As voltage and temperature change on the SDRAM die, the DQS clock tree delay will shift and may require re-training. The DDR5-SDRAM includes an internal DQS clock-tree oscillator to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time. The DQS Oscillator will provide the controller with important information regarding the need to re-train, and the magnitude of potential error.

The DQS Interval Oscillator is started by issuing an MPC [Start DQS Osc] command with OP[0000 0111B] set as described in the MPC Operation section, which will start an internal ring oscillator that counts the number of times a signal propagates through a copy of the DQS clock tree.

The DQS Oscillator may be stopped by issuing an MPC [Stop DQS Osc] command with OP[0000 0110_B] set as described in the MPC Operation section, or the controller may instruct the SDRAM to count for a specific number of clocks and then stop automatically (See MR45,46, and 47 for more information). If MR45 is set to automatically stop the DQS Oscillator, then the MPC [Stop DQS Osc] command shall not be used. When the DQS Oscillator is stopped by either method, the result of the oscillator counter is automatically stored in MR46 and MR47 after the oscillator is stopped and within tOSCOA for the automatic mode and tOSCOM for the manual mode.

MRW commands to MR45 during an ongoing DQS Interval Oscillator operation are not permitted. MR45 may be reprogrammed tMRD after the oscillator is stopped by the automatic stop.

The DRAM shall respond in one of two ways if an MPC Start DQS Osc is issued during an ongoing DQS Interval Oscillator operation (automatic or manual). One option is the DRAM will ignore the concurrent start command, in which case the DQS Interval Oscillator operation will proceed as normal with all timing constraints referencing the original start command. The other option is for the DRAM to restart the DQS Interval Oscillator operation, in which case all timing constraints will reference the most recent (subsequent) start command. The host must account for the worst-case option in the event that a concurrent start command is issued. If issuing a concurrent MPC [Start DQS Osc] results in a loss of run time tracking, the results stored in MR46 and MR47 should be ignored and the full operation restarted.

Entering Self Refresh during an ongoing DQS Interval Oscillator operation is permitted. Upon exiting Self Refresh, an operation started in automatic mode shall be allowed to complete naturally based upon the specified number of clocks (cumulative before and after Self Refresh). If a manual operation started prior to entering Self Refresh is not stopped prior as well, the operation shall be manually stopped upon Self Refresh exit. The results stored in MR46 and MR47 for a DQS Interval Oscillator operation that spans Self Refresh entry/exit should be ignored and the full operation restarted.

The controller may adjust the accuracy of the result by running the DQS Interval Oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the result for a given temperature and voltage is determined by the following equation:

$$\textit{DQS Oscillator Granularity Error} = \frac{\textit{2 * (DQS delay)}}{\textit{Run Time}}$$

Where:
Run Time = total time between start and stop commands
DQS delay = the value of the DQS clock tree delay (tRX_DQS2DQ min/max)

Additional matching error must be included, which is the difference between DQS training circuit and the actual DQS clock tree across voltage and temperature. The matching error is vendor specific.

Therefore, the total accuracy of the DQS Oscillator counter is given by:

$$\textit{DQS Oscillator Accuracy = 1 - Granularity Error - Matching Error}$$

4.32 DQS Interval Oscillator (cont'd)

Example: If the total time between start and stop commands is 100 ns, and the maximum DQS clock tree delay is 400 ps (tRX_DQS2DQ max), then the DQS Oscillator Granularity Error is:

$$\textit{DQS Oscillator Granularity Error} = \frac{2 * (0.4\ ns)}{100ns} = 0.8\%$$

This equates to a granularity timing error of 3.2ps.

Assuming a circuit Matching Error of 5.5 ps across voltage and temperature, then the accuracy is:

$$\textit{DQS Oscillator Accuracy} = 1 - \frac{3.2 + 5.5}{400} = 97.8\%$$

Example: Running the DQS Oscillator for a longer period improves the accuracy. If the total time between start and stop commands is 250 ns, and the maximum DQS clock tree delay is 400 ps (tRX_DQS2DQ max), then the DQS Oscillator Granularity Error is:

$$\textit{DQS Oscillator Granularity Error} = \frac{2 * (0.4\ ns)}{250ns} = 0.32\%$$

This equates to a granularity timing error or 1.28 ps.

Assuming a circuit Matching Error of 5.5 ps across voltage and temperature, then the accuracy is:

$$\textit{DQS Oscillator Accuracy} = 1 - \frac{1.28 + 5.5}{400} = 98.3\%$$

The result of the DQS Interval Oscillator is defined as the number of DQS Clock Tree Delays that can be counted within the "run time," determined by the controller. The result is stored in MR46 and MR47. MR46 contains the least significant bits (LSB) of the result, and MR47 contains the most significant bits (MSB) of the result. MR46 and MR47 are overwritten by the SDRAM when an MPC-1 [Stop DQS Osc] command is received. The SDRAM counter will count to its maximum value (=2^16) and stop. If the maximum value is read from the mode registers, then the memory controller must assume that the counter overflowed the register and discard the result. The longest "run time" for the oscillator that will not overflow the counter registers can be calculated as follows:

$$\textit{Longest Run Time Interval} = 2^{16} * tRX_DQS2DQ(min)$$

The interval oscillator matching error is defined as the difference between the DQS training circuit (interval oscillator) and the actual DQS clock tree across voltage and temperature.

- Parameters:
  - tRX_DQS2DQ: Actual DQS clock tree delay
  - tDQSOSC: Training circuit (interval oscillator) delay
  - OSCOffset: Average delay difference over voltage and temp
  - OSCMatch: DQS oscillator matching error

4.32 DQS Interval Oscillator (cont'd)

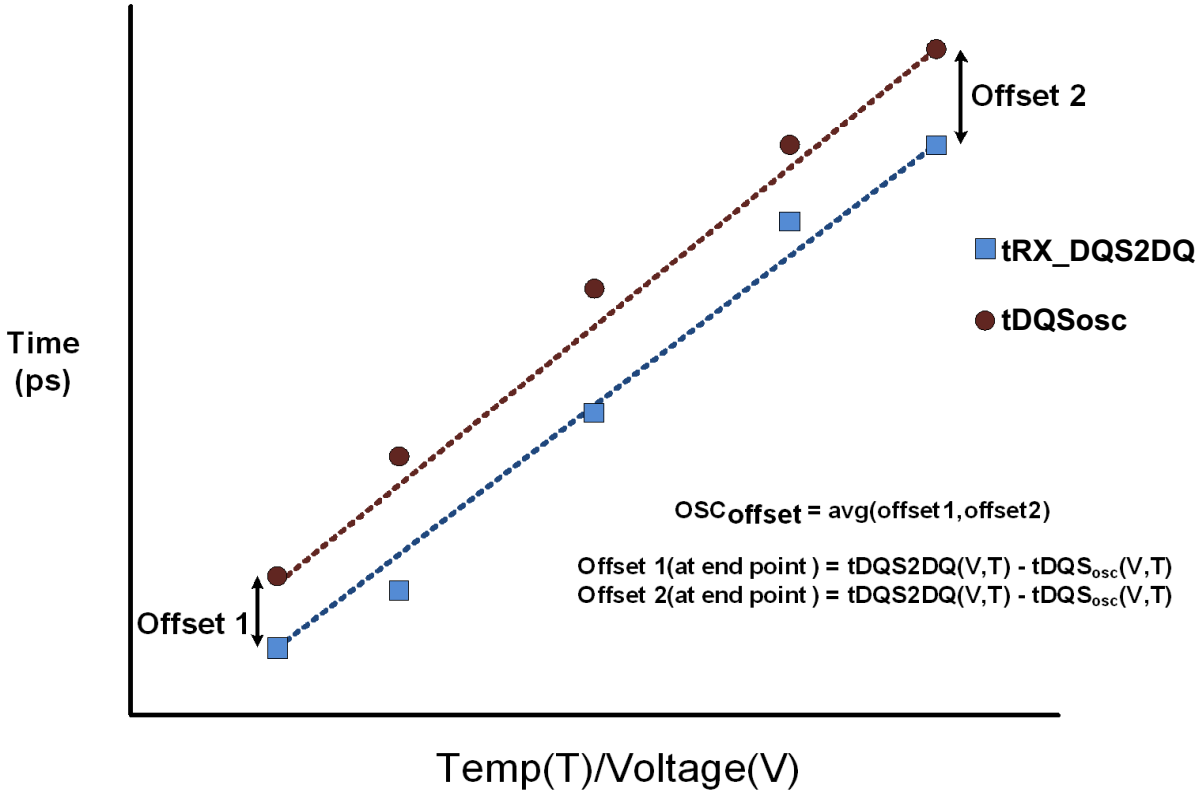


Figure 153 — Interval Oscillator Offset (OSC_{offset})

- OSC_{Match}:

$$OSC_{Match} = [tRX_DQS2DQ_{(V,T)} - tDQS_{OSC(V,T)} - OSC_{offset}]$$

- $tDQS_{OSC}$:

$$tDQS_{OSC(V,T)} = \frac{Runtime}{2 * Count}$$

4.32 DQS Interval Oscillator (cont'd)

Table 139 — DQS Oscillator Matching Error Specification

Parameter	Symbol	Min	Max	Units	Notes
DQS Oscillator Matching Error	OSCMatch	-10	+10	ps	1, 2, 3, 4, 5, 6, 7, 8
DQS Oscillator Offset	OSC_{offset}	-150	150	ps	2, 4, 6, 7

NOTE 1 The OSC_{Match} is the matching error per between the actual DQS and DQS interval oscillator over voltage and temp.

NOTE 2 This parameter will be characterized or guaranteed by design.

NOTE 3 The OSC_{Match} is defined as the following:

$$OSC_{Match} = [tRX_DQS2DQ_{(V,T)} - tDQS_{OSC(V,T)} - OSC_{offset}]$$

Where $tRX_DQS2DQ_{(V,T)}$, $tDQS_{OSC(V,T)}$ and $OSC_{offset(V,T)}$ are determined over the same voltage and temp conditions.

NOTE 4 The runtime of the oscillator must be at least 200ns for determining $tDQS_{OSC(V,T)}$

$$tDQS_{OSC(V,T)} = \frac{Runtime}{2 * Count}$$

NOTE 5 The input stimulus for tRX_DQS2DQ will be consistent over voltage and temp conditions.

NOTE 6 The OSCoffset is the average difference of the endpoints across voltage and temp.

NOTE 7 These parameters are defined per channel.

NOTE 8 tRX_DQS2DQ(V,T) delay will be the average of DQS to DQ delay over the runtime period.

NOTE 9 The matching error and offset of OSC came from DQS2DQ interval oscillator.

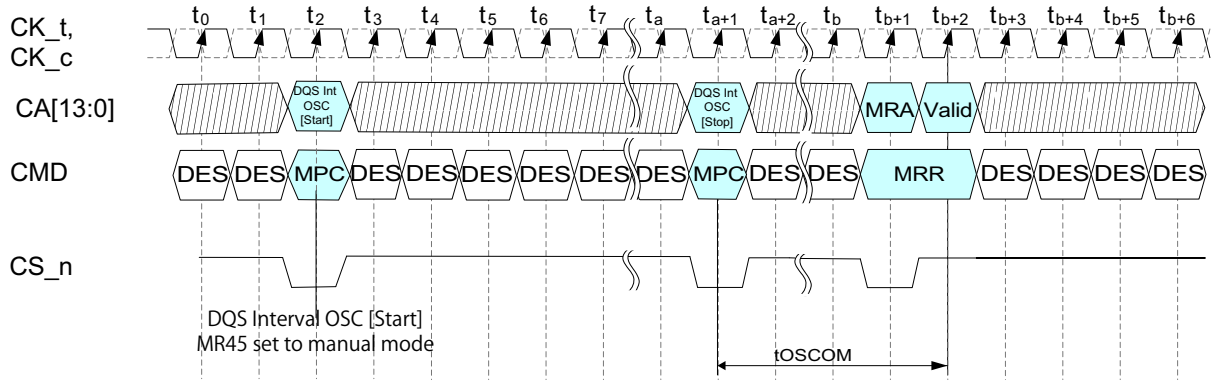
The interval oscillator count read out timing.

Table 140 — DQS Interval Oscillator Readout AC Timing

Parameter [1]	Symbol	DDR5-3200 to 9200		Unit	Notes
		Min	Max		
Delay time from DQS Interval Oscillator stop to Mode Register Readout in manual mode	tOSCOM	tMPC_Delay	-	nCK	
Delay time from DQS Interval Oscillator automatic mode timer expiration to Mode Register Readout	tOSCOA	tMRD	-	nCK	
DQS Interval Oscillator start gap in automatic stop mode	tOSCS	tMPC_Delay + DQS Interval Timer Run Time		nCK	

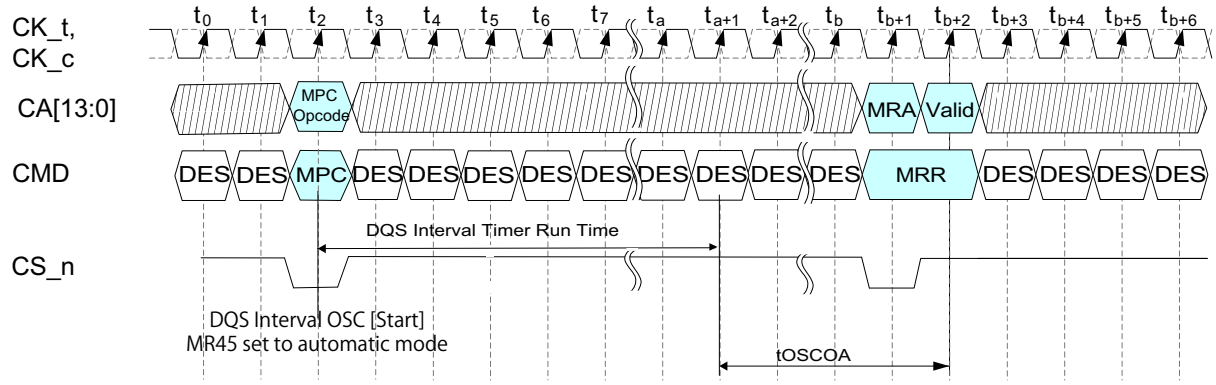
NOTE 1 In manual stop mode, DQS osc start command should be followed by DQS osc stop command (MPC). Otherwise, DQS osc result value (MR46 and MR47) cannot be guaranteed.

4.32 DQS Interval Oscillator (cont'd)



NOTES:
1. DES commands are shown for erase of illustrator; other commands may be valid at these times.

Figure 154 — DQS Interval Oscillator Manual Mode Timing Diagram



NOTES:
1. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 155 — DQS Interval Oscillator Automatic Mode Timing Diagram

4.33 tRX_DQS2DQ Offset Due to Temperature and Voltage Variation

As temperature and voltage change on the SDRAM die, the DQS clock tree will shift and may require retraining. The oscillator is usually used to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time. The tRX_DQS2DQ offset due to temperature and voltage variation specification can be used for instances when the oscillator cannot be used to control the tRX_DQS2DQ.

Table 141 — tRX_DQS2DQ Offset Due to Temperature and Voltage Variation for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS to DQ offset temperature variation	tRX_DQS2DQ_temp	-	12.75	-	11.34	-	10.20	-	9.28	-	8.50	ps / 10 ℃	1, 3
DQS to DQ offset voltage variation	tRX_DQS2DQ_volt	-	45.00	-	43.00	-	41.00	-	39.00	-	32.00	ps / 50 mV	2, 3

NOTE 1 tRX_DQS2DQ max delay variation as a function of temperature

NOTE 2 tRX_DQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD. It includes the VDDQ and VDD AC noise impact for frequencies >20 MHz and max voltage of 45 mVpk-pk from DC -20 MHz at a fixed temperature on the package. For tester measurement VDDQ=VDD is assumed

NOTE 3 Absolute value of DQS to DQ offset.

Table 142 — tRX_DQS2DQ Offset Due to Temperature and Voltage Variation for DDR5-5200 to 6800

Parameter	Symbol	DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		DDR5-6800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS to DQ offset temperature variation	tRX_DQS2DQ_temp	-	7.85	-	7.29	-	6.80	-	6.38	-	6.000	ps / 10 ℃	1, 3
DQS to DQ offset voltage variation	tRX_DQS2DQ_volt	-	30.00	-	28.00	-	26.25	-	25.00	-	23.75	ps / 50 mV	2, 3

NOTE 1 tRX_DQS2DQ max delay variation as a function of temperature

NOTE 2 tRX_DQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD. It includes the VDDQ and VDD AC noise impact for frequencies >20 MHz and max voltage of 45 mVpk-pk from DC -20 MHz at a fixed temperature on the package. For tester measurement VDDQ=VDD is assumed

NOTE 3 Absolute value of DQS to DQ offset.

Table 143 — tRX_DQS2DQ Offset Due to Temperature and Voltage Variation for DDR5-7200 to 9200

Parameter	Symbol	DDR5-7200		DDR5-7600		DDR5-8000		DDR5-8400		DDR5-8800		DDR5-9200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS to DQ offset temperature variation	tRX_DQS2DQ_temp	-	5.67	-	5.37	-	5.10	-	4.86	-	4.64	-	4.44	ps / 10 ℃	1, 3
DQS to DQ offset voltage variation	tRX_DQS2DQ_volt	-	22.50	-	21.25	-	20.00	-	19.00	-	18.00	-	17.00	ps / 50 mV	2, 3

NOTE 1 tRX_DQS2DQ max delay variation as a function of temperature

NOTE 2 tRX_DQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD. It includes the VDDQ and VDD AC noise impact for frequencies >20 MHz and max voltage of 45 mVpk-pk from DC -20 MHz at a fixed temperature on the package. For tester measurement VDDQ=VDD is assumed

NOTE 3 Absolute value of DQS to DQ offset.

4.34 2N Mode

2N mode allows the system to provide more setup and hold time on the CA bus. 2N mode is enabled by default on the DDR5 SDRAM, and an MPC is used to change between 2N and 1N modes. MR2:OP[2] allows the state of the 2N Mode to be read.

DDR5 has defined two cycle commands, which requires the DRAM to capture the command differently between 1N and 2N modes. In both modes, the first half of the command is sampled on the clock that the chip select is active. In 1N mode, the second half of the command is sampled on the next clock edge. In 2N mode, the second half of the command is sampled 2 clocks after the first half. Non-target ODT signaling (on the chip select) is also delayed by a clock in 2N mode.

To the DRAM, one clock commands operate the same in 1N and 2N mode, with the command sampled on the same clock as the chip select active.

A 2-cycle or 1-cycle command can start on any clock (unlike geardown mode). Figure 156 below shows the differences between standard 1N mode with a 2-cycle read command, followed by a 1-cycle precharge command, and what it looks like when operated in 2N mode with the same commands. While in 2N mode, the host will never send two consecutive Chip Selects except during explicit cases such as exiting CATM mode.

Table 144 — MR2 Functional Modes (for Reference Only) [1]

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Internal Write Timing	Reserved	Device 15 MPSM	CS Assertion Duration (MPC)	Max Power Savings Mode (MPSM)	2N Mode	Write Leveling Training	Read Preamble Training
NOTE 1 OP(0-7) can be programed with either “0” or “1”.							

Table 145 — 2N Mode Register Config

Function	Register Type	Operand	Data	Notes
2N Mode	R	OP[2]	0B: 2N Mode (Default) 1B: 1N Mode	1, 2
NOTE 1 To ensure training modes can be enabled and run appropriately, the default (power-on) mode for DDR5 is 2N mode. Post CA Training, the user can configure this bit to put the device into either 1N mode or 2N mode. Both 1N and 2N modes are valid operating conditions for DDR5.				
NOTE 2 Since 2N Mode setting is an MPC based command, it can only be programmed via that command and its mode register is therefore read only.				

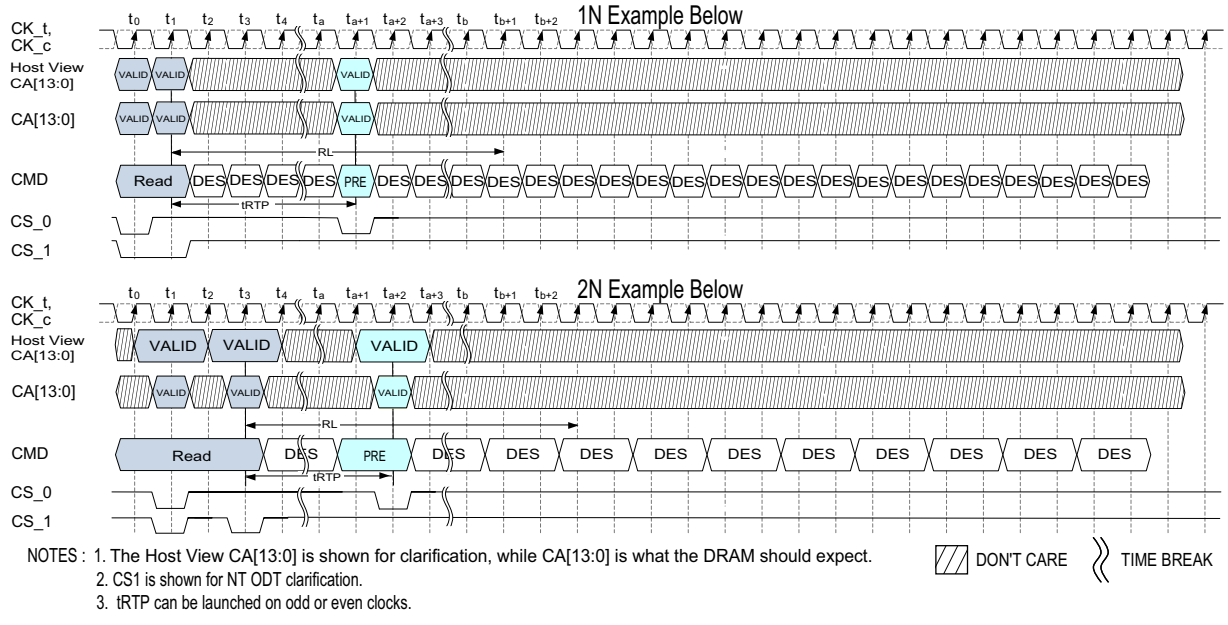


Figure 156 — Example of 1N vs 2N Mode - for Reference Only

4.34.1 1N / 2N Mode Clarifications

Several DDR5 SDRAM features require specific CS_n and CA bus behavior to function correctly in 1N and 2N mode. Table 146 describes the various behaviors (additional details in the respective sections of the spec).

Table 146 — CS_n and CA Bus Required Behaviors

Item	CS Assertion Duration	CS_n Required Behavior for 1N	CS_n Required Behavior for 2N	CA Bus Required Behavior for Multi-Cycle CS Assertion / 2N
Cold or Warm Reset Exit	Multi (default)	NA	Static low for 3+ nCK	Static NOP for 3+ nCK
MPC (includes CSTM Exit)	Single	Single low pulse	Single low pulse	Single MPC
	Multi	Static Multi-Cycle low	Static Multi-Cycle low	Static MPC surrounding CS_n low by tMC_MPC_*
VREFCS / VREFCA	Single	Single low pulse	Single low pulse	Single VREFCS / VREFCA
	Multi	Static Multi-Cycle low	Static Multi-Cycle low	Static VREFCS / VREFCA surrounding CS_n low by tMC_VREFCS_* / tMC_VREFCA_*
CATM exit (NOP Command)	Don't care	Static low for 2+ nCK	Static low for 2+ nCK	Static NOP for the duration of tCATM_CS_Exit
PDX	Don't care	Single low pulse	Single low pulse	Single NOP
SRX (3 NOPs)	Don't care	Static low for 3+ nCK	Static low for 3+ nCK	Static NOP for 3+ nCK if CS_n held static low
		Pulsing low 3+ cycles (...0, 1, 0, 1, 0...)	Pulsing low 3+ cycles (...0, 1, 0, 1, 0...)	Static NOP for 5+ nCK if CS_n is pulsed low
NOTE 1 MR2:OP[4], CS Assertion Duration, setting only applies to the MPC, VREFCS and VREFCA commands				

4.35 Write Pattern Command

Due to the significant percentage of writes that contain all zeros, this new mode is being proposed for inclusion into the DDR5 standard as a new WRITE Pattern command. When used effectively, the command can save power by not actually sending the data across the bus.

This new mode is operated very similar to a standard write command with the notable exceptions that it has its own encoded WRITE Pattern command, no data is sent on the DQ bus, no toggling of DQS is needed, and the DRAM does not turn on any internal ODT. ECC parity is based on the Write Pattern Mode data in MR48.

Upon receiving the command, the DRAM device will source the input for the memory array from the Write Pattern Mode Registers instead of from the DQ bits themselves. The DQ mapping across the burst is shown below in DQ output mapping table. The host will not send any data during this time. All timing constraints are still measured from the clocks where the write command data would have been transferred. e.g. tWR is measured from end of write burst to PRE as shown below in Figure . The pattern used for this mode is provided by the contents of MR48:OP[7:0]. That pattern can be all zeros, all ones, or something else, and can be changed with an MRW command to MR48. The power on default for this mode register is all zeros.

The DQ output mapping table below describes how the pattern stored in MR48 above will be mapped into the DRAM array across the DQ bits and Burst. The pattern is described as follows:

In the case of a x4 SDRAM device, only OP[3:0] will used, with each bit of the pattern corresponding to DQ[3:0] respectively. The same OP value will be repeated over the entire burst for that bit (i.e. DQ0 store OP0 on every UI of the burst). Although OP[7:4] are not used for the x4, the original programmed MRW values will still be read during an MRR. OP[7:4] will not revert back to the default of zero.

In the case of a x8 SDRAM device, the whole pattern OP[7:0] will be used, with each bit of the pattern corresponding to DQ[7:0] respectively. The same OP value will be repeated over the entire burst for that bit. (i.e. DQ0 store OP0 on every UI of the burst)

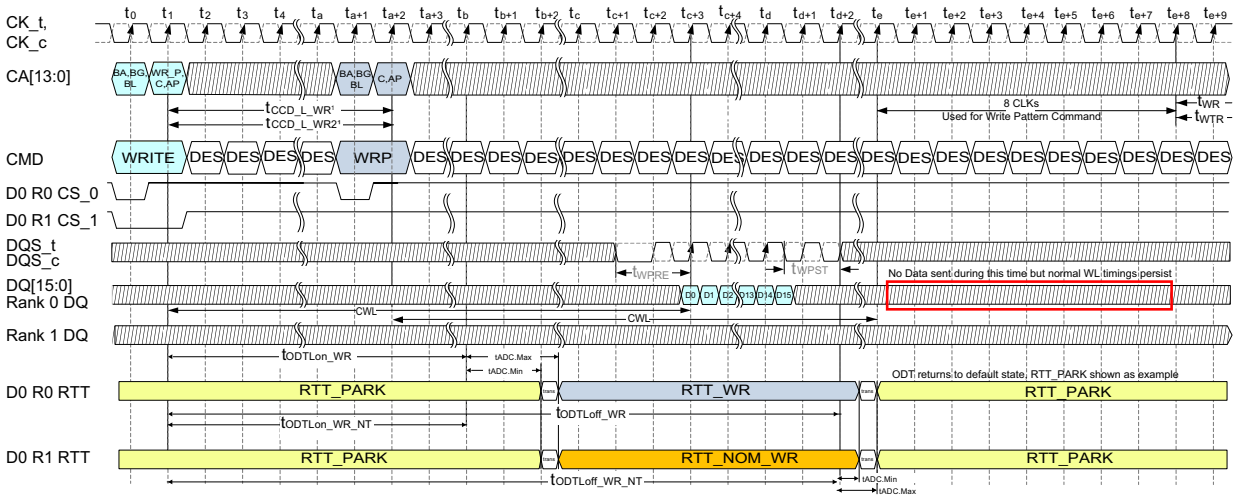
In the case of a x16 SDRAM device, the whole pattern OP[7:0] will be used, with each bit of the pattern corresponding to DQL[7:0] respectively and then that pattern will be repeated for DQU[7:0]. The same OP value will be repeated over the entire burst for that bit. (i.e., DQ0 store OP0 on every UI of the burst)

The Burst Length (BL) supported in Write Pattern Mode is based on MR0 OP[1:0]. The Write Pattern Command (WRP) does not support On-The-Fly (OTF), resulting in the output values being either a fixed BL16 or BL32.

4.35 Write Pattern Command (cont'd)

Table 147 — Write Pattern DQ Output Mapping

SDRAM CONFIG	BL16 x16	BL16 x8	BL16 x4	BL32 x4
UI	0-15	0-15	0-15	0-31
DQL0 / DQ0	OP0	OP0	OP0	OP0
DQL1 / DQ1	OP1	OP1	OP1	OP1
DQL2 / DQ2	OP2	OP2	OP2	OP2
DQL3 / DQ3	OP3	OP3	OP3	OP3
DQL4 / DQ4	OP4	OP4	-	
DQL5 / DQ5	OP5	OP5	-	
DQL6 / DQ6	OP6	OP6	-	
DQL7 / DQ7	OP7	OP7	-	
DQU0	OP0	-	-	
DQU1	OP1	-	-	
DQU2	OP2	-	-	
DQU3	OP3	-	-	
DQU4	OP4	-	-	
DQU0	OP5	-	-	
DQU6	OP6	-	-	
DQU7	OP7	-	-	
DML_n / DM_n	INVALID	INVALID	-	
DMU_n	INVALID	-	-	



NOTES:

1. Refer to Table 51, Table 52, and Table 54 to determine if the timing parameter definition for WRITE to WRP is tCCD_L_WR or tCCD_L_WR2.
2. The DQ signal is shown as "Don't Care" before the first Write data bit indicating DFE is disabled. When DFE is enabled, the DQ signal shall be high for a minimum of 4UI prior to the first Write data bit for proper DFE synchronization.

Figure 157 — Example of Write Pattern Command

4.36 On-Die ECC

DDR5 devices shall implement internal Single Error Correction (SEC) ECC to improve the data integrity within the DRAM. The DRAM shall use 128 data bits to compute the ECC code of 8 ECC Check Bits.

For a x4 DDR5 device, internal prefetch for on-die ECC is 128 bits even though a x4 is a 64-bit prefetch device. For each read or write transaction in a x4 device, an additional section of the DRAM array is accessed internally to provide the required additional 64 bits used in the 128-bit ECC computation. In other words, in a x4 device, each 8-bit ECC Check Bit word is tied to two 64-bit sections of the DRAM. In the case of a x8 device, no extra prefetch is required, as the prefetch is the same as the external transfer size. For a x16 device, two 128-bit data words and their corresponding 8 check bits are fetched from different internal banks(same external bank address). Each 128 Data bits and the corresponding 8 check bits are checked separately and in parallel.

On reads, the DRAM corrects any single-bit errors before returning the data to the memory controller. The DRAM shall not write the corrected data back to the array during a read cycle.

On writes, the DRAM computes ECC and writes data and ECC bits to the array. If the external data transfer size is smaller than the 128 data bits code word (x4 devices), then DRAM will have to perform an internal 'read-modify-write' operation. The DRAM will correct any single-bit errors that result from the internal read before merging the incoming write data and then re-compute 8 ECC Check bits before writing data and ECC bits to the array. In the case of a x8 and x16 DDR5, no internal read is required.

For a x16 device, two 136-bit code words are read from two internal banks(same external bank address), one code word is mapped to DQ[0:7] and the other code word is mapped to DQ[8:15].

4.36.1 SEC Overview

The ECC blocks shown in Figure 158 are the ECC Check Bit Generator, Syndrome Generator, Syndrome Decode, and Error Correction. The Check Bit Generator and Syndrome Generator blocks are fully specified by the H matrix.

The Syndrome Decode block executes the following function:

Zero Syndrome => No Error

Non-Zero Syndrome matches one of the columns of the H matrix => Flip Corresponding bit

Non-Zero Syndrome that does not match any of the columns in the H matrix => DUE

DUE: Detected Uncorrected

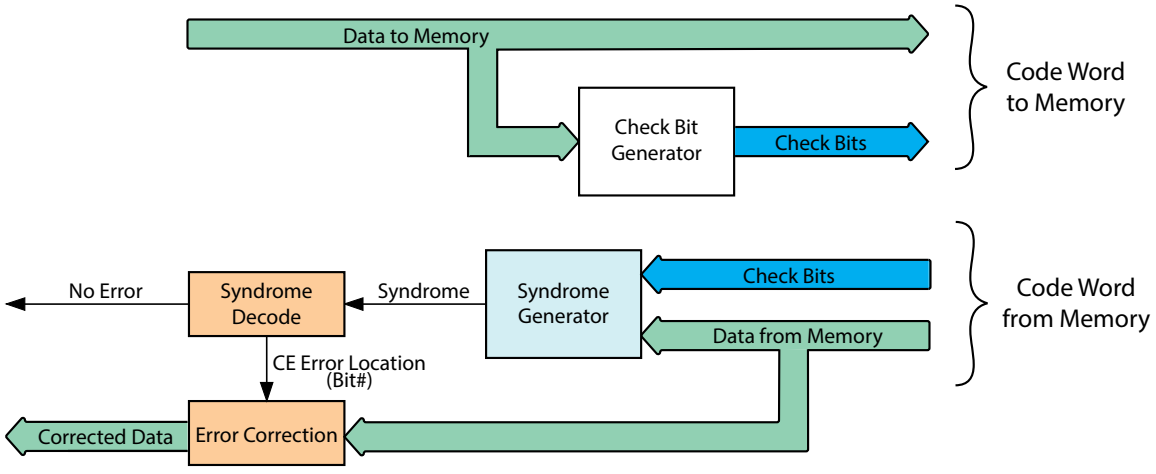


Figure 158 — On Die ECC Block Diagram

4.37 DDR5 ECC Transparency and Error Scrub

DDR5 ECC Transparency and Error Scrub incorporates an ECC Error Check and Scrub (ECS) mode with an error counting scheme for transparency. The ECS mode allows the DRAM to internally read, correct single bit errors, and write back corrected data bits to the array (scrub errors) while providing transparency to error counts. It is recommended that a full error scrub of the DRAM is performed a minimum of once every 24 hours.

There are two options for ECS mode, set via Mode Register. The Manual ECS mode (MR14:OP[7] = 1_B) allows for ECS operations via the Multi-Purpose Command. The Automatic ECS mode (MR14:OP[7] = 0_B, default setting) allows for the ECS to run internal to the DRAM.

The ECS feature is available on all device configurations.

ECS mode implements two counters to track ECC code word errors detected during operation: Error Counter (EC) and Errors per Row Counter (EpRC). The EC defaults to counting rows with errors; however, it may also be configured to count code words with errors. In row mode (default), the EC tracks the number of rows that have at least one code word error detected subject to a threshold filter. In the code word mode, the EC tracks the total number of code word errors, also subject to the threshold filter. The second counter, EpRC, tracks the error count of the row with the largest number of code word errors along with the address of that row. EpRC error reporting is also subject to a separate threshold filter. A general functional block diagram example of the ECS Mode operation is shown in Figure 159 while the ECC Error Checking and Scrub mode, Mode Register (MR14), is shown in Table 148.

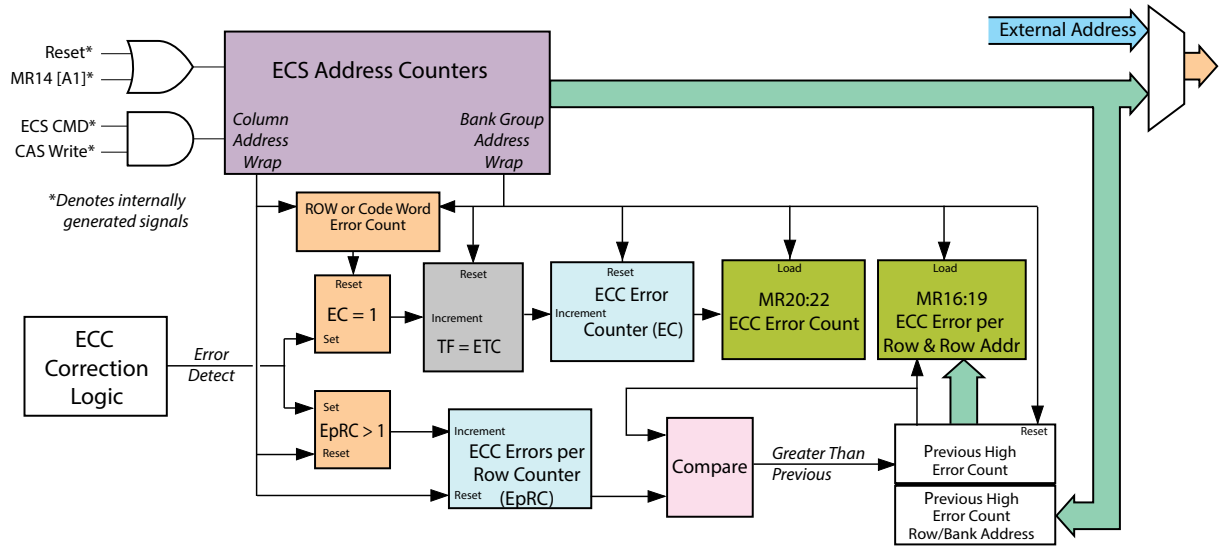


Figure 159 — Example of an ECC Transparency and Error Scrub Functional Block Diagram

Table 148 — MR14 ECC Transparency and Error Scrub Mode Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
ECS Mode	Reset ECS Counter	Row Mode/Code Word Mode	RFU	CID3	CID2	CID1	CID0

4.37.1 Mode Register and DRAM Initialization Prior to ECS Mode Operation

The ECC Transparency and Error Scrub counters are set to zero and the internal ECS Address Counters are initialized either by a RESET or by manually writing MR14 OP[6]=1_B. While MR14:OP[6]=1_B, ECS counters are reset and no additional ECS operations shall occur. If manual reset via mode register is utilized, mode register bit MR14 OP[6] shall be written back to a 0 before any subsequent ECS operations will continue or a subsequent reset can be applied.

4.37.1 Mode Register and DRAM Initialization Prior to ECS Mode Operation (cont'd)

ECS mode register selections Automatic ECS in Self-Refresh (MR15:OP[3]), ECS Threshold Filter (MR15:OP{2:0]), Manual / Automatic ECS Mode (MR14:OP[7]), and Row/Code Word Mode (MR14:OP[5]) shall be programmed during DRAM initialization and shall not be changed once the first ECS operation occurs unless followed by issuing a RESET or ECS Reset Counters, otherwise an unknown operation could result during subsequent ECS operations.

An ECS Reset Counters operation requires setting MR14:OP[6]=1_B to reset MR16 - MR20. Setting MR14:OP[6]=0_B is then required to re-enable Manual or Automatic ECS operations.

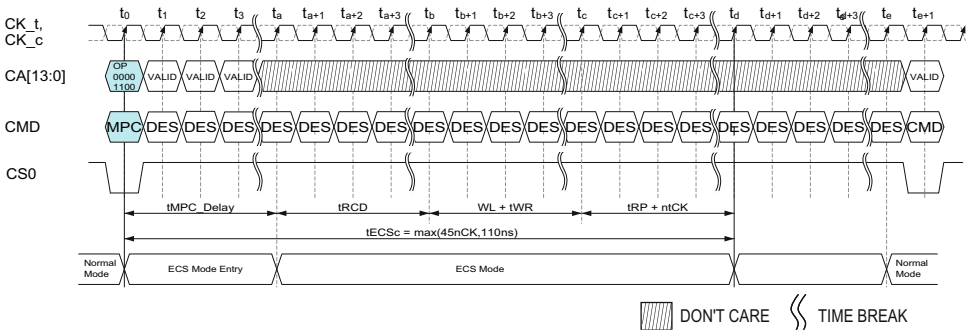
Manual ECS mode is enabled by MR14 OP[7] = 1_B. A manual ECS operation requires an MPC command with OP[7:0]=0000 1100_B.

The DRAM must have all array bits written to prior to executing ECS operations to avoid generating false failures.

4.37.2 ECS Operation

All banks shall be precharged and in an idle state prior to executing a manual ECS operation.

Executing a manual ECS operation, MPC command with OP[7:0]=0000 1100_B, generates the following internally self-timed command sequence: ACT→RD→WR→PRE. ECS operation timing is shown in Figure 160.



ECS Mode Timing Diagram

Figure 160 — ECS Operation Timing Diagram

The minimum time for the ECS operation to execute is t_{ECSc} (t_{MPC_Delay} + t_{RCD} + WL + t_{WR} + t_{RP} + nt_{CK}). nt_{CK} is required to satisfy t_{ECSc}.

Table 149 — ECS Operation Timing Parameter

Parameter	Symbol	Min	Max	Unit	NOTE
ECS Operation time	t_{ECSc}	Max(176nCK, 110ns)	-	ns	

Upon executing a manual ECS operation. DQ's will remain in RTT_PARK and DQS in DQS_RTT_PARK. The only commands allowed other than DES during t_{ECSc} for a manual ECS operation are ODT NT commands, which may change the DQ and DQS termination state.

Any illegal usage of manual ECS mode (e.g. refresh or temperature violations) will result in operation not being guaranteed.

Executing a manual ECS operation by an MPC command with OP[7:0]=0000 1100_B will issue an internally timed ACT command row activation based on the internal ECS Address Counters' row address, t_{MPC_Delay} after the MPC command. The ACT command is to be followed by a WR command t_{RCD} later. The WR command will perform an internal Read-Modify-Write cycle on the code word determined by the internal ECS Address Counters' column address.

4.37.2 ECS Operation (cont'd)

The internal Read-Modify-Write cycle will:

3. Read the entire code word (128 data bits and 8 check bits) from the array
4. Correct a single bit error in the code word or check bits, if an error is detected
5. Write the resultant code word back to the DRAM array

The WR command is followed by a PRE command WL + t_{WR} later. The PRE command will automatically re-enable the DRAM's I/Os and address inputs, and it will return the DRAM to idle mode t_{RP} + nt_{CK} later, after t_{ECSc} is satisfied.

For each ECS operation, ECS Address Counters increment the column address after each internal ECS WR command such that the next code word and check bits are selected. Once the column counter wraps (all code words and check bits on the row have been accessed), the row counter will increment until all code words on each of the rows within a bank are accessed. When the row counter wraps (all rows within the bank have been accessed), the bank counter will increment and the next bank within a bank group will repeat the process of accessing each code word. When the bank counter wraps, the bank group counter will increment and the next bank group will repeat the process of accessing each code word, until all bank groups within the DRAM have been accessed.

After all the code words within the DRAM are read, corrected, and written once, the bank group counter will wrap and the process begins again with the next manual ECS operation. The total number of manual ECS operations required to complete one cycle of Error Check and Scrub is density and configuration dependent, as listed in Table 150. The DRAM controller shall track the number of manual ECS operations to complete a full scrub of that device.

Table 150 — Number of Code Words per DRAM

Configuration	8 Gb	16 Gb	24 Gb	32 Gb	64 Gb
x4, x8, x16	2^26	2^27	2^27 * 1.5	2^28	2^29

In order to complete a full Error Check and Scrub within the recommended 24 hours, the average periodic interval per ECS operation (t_{ECSint}) is 86,400 seconds divided by the total number of manual ECS operations to complete one full cycle of ECS. t_{ECSint} is included in Table 151.

Table 151 — Average Periodic ECS Interval (tECSint)

Configuration	8 Gb	16 Gb	24 Gb	32 Gb	64 Gb
x4, x8, x16	1.287 mS	0.644 mS	0.429 mS	0.322 mS	0.161 mS

In order for the DDR5 SDRAM to perform automatic ECS operations when in Automatic ECS Mode, the host needs to issue periodic REFab commands or periodically enter Self Refresh mode. The maximum spacing between REFab commands or Self Refresh entry for the DRAM to complete the automatic scrub within the recommended 24 hours is t_{ECSint}. Meeting this REFab/Self-Refresh requirement allows the DRAM to perform the automatic ECS operations without placing additional restrictions on refresh mode usage, i.e. all bank/same bank refresh or normal/FGR mode refresh, while in Automatic ECS mode. REFab commands issued in excess of required by the DRAM for automatic ECS operations (one per t_{ECSint}) may be used by the DRAM for normal refresh operation. Issuing multiple REF commands shall not exceed the total number allowed within a 1 x t_{REFI} window, as described in the Refresh Operation Scheduling Flexibility section of the spec.

When in Automatic ECS mode, the ECS commands and timing are generated and satisfied internal to the DRAM, following the Average Periodic ECS Interval timings to ensure that the Error Check and Scrub is completed and the transparency registers (MR16 -20) are updated within the recommended 24-hour period.

The DRAM is required to perform automatic ECS operations while in Self Refresh mode if Automatic ECS is enabled by MR14 OP[7]=0_B or Automatic ECS in Self-Refresh is enabled by MR15 OP[3]=1_B, to meet the Average Periodic ECS Interval timings. However, some variation in the DRAM scrubbing rate may be encountered while in Self Refresh since the DRAM will need to sync the internal operations to an internal oscillator fre-quency. Entering and exiting Self Refresh will not reset the ECS transparency counters/registers. Interval timing for the maximum spacing between REFab commands or another Self Refresh entry is allowed to restart upon Self Refresh exit.

4.37.3 ECS Threshold Filter

The ECC Transparency and Error Scrub scheme incorporates a user programmable ECS Threshold Filter that masks error counts less than the programmed filter value. The value is set using MR15 as listed in Table 152. The default MR15 setting is 256 fails per Gb of memory cells (OP[2:0] = 011B).

Table 152 — MR15 Transparency ECC Error Threshold Count per Gb of Memory Cells and Automatic ECS in Self-Refresh

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU				Automatic ECS in Self-Refresh	OP[2:0]: 000_B = 4 OP[2:0]: 001_B = 16 OP[2:0]: 010_B = 64 OP[2:0]: 011B = 256 (Default) OP[2:0]: 100B = 1024 OP[2:0]: 101B = 4096 OP[2:0]: 110B = RFU OP[2:0]: 111B = RFU		

4.37.4 ECS Error Tracking

The type of error tracking provided by the ECC Transparency and Error Scrub is selectable using MR14 OP[5], which can track either the number of rows (default) or code words with errors using the Error Counter. The row or code word error count will be tracked and written to MR20 register. MR14 OP[5] is programmed during DRAM initialization and should not be changed once the first ECS command has been issued, otherwise an unknown operation could result. If MR14 OP[5] is changed without powering down, a MR14 OP[6] reset shall be issued prior to subsequent ECS commands to reinitialize the counters.

When the ECC row count mode is selected, the Error Counter (EC) increments each time a row with check bit errors is detected. After all rows, in all banks, in all bank groups have ECS operations performed, the result of the Error Counter is loaded into MR20, subject to error threshold reporting. The EC is reset after the value has been transferred to the mode register.

MR20 is shown in Table 153. EC[7:0] indicate error counts within a range. EC0 is set to "1" if $EC0_{min}$ (the ETC set by MR15) has been reached, but the fail count is less than or equal to $EC0_{max}$ = 2 * ETC * Density(Gb) - 1. Likewise, the min values of EC[7:1] are defined as $EC[x]_{min}$ = ETC * Density(Gb) * 2^x, and max values are defined as $EC[x]_{max}$ = 2 * (ETC * Density(Gb) * 2^x) - 1. The exception is $EC7_{max}$, which is unlimited. The corresponding bit will be set if the error count is within the required range.

Table 153 — MR20 Number of Rows or Code Word Errors per DRAM Die

	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
MR20	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

When the ECC code word error count mode is selected, the Error Counter (EC) increments each time a code word with check bit errors is detected. After all code words, on all rows, in all banks, in all bank groups had ECS commands performed, the result of the Error Counter is loaded into MR20, subject to error threshold reporting. The EC is reset after the value has been transferred to the mode register.

The ECC Errors per Row Counter increments the number of code words errors on a given row, after more than one error on a given row is detected. The EpRC counter is reset with each column address wrap. Each row's code word error count is compared to the previous code word error count to determine the row address with the highest error count within the DRAM die. After reading all code words on a row, the number of errors counted is compared to the number of errors from the previous row. If the previous row error count is less than the present row error count, the present larger error count is saved to the Previous High Error Count register, its associated address is saved to the Previous High Error Count Row/Bank Address/Bank Group register, and the present row error counter is cleared. If the previous row error count is greater than the present row error count, the previous row error count and register value remains unchanged, however the present row error counter is cleared.

After all rows, in all banks, in all bank groups have executed ECS operations, the result of the Previous High Error Count (address and error count) are latched into MR16:19 when the bank group counter wraps, if the Errors per Row Count(EpRC) meets or exceeds the Row Error Threshold Count(RETC) in Table 155. MR16:18 shown in Table 154 contains the information for the row with the highest number of code word errors and is allocated as A[17:0] Row Address, BA[1:0] Bank Address, BG[2:0] Bank Group Address. MR19 shown in Table 154 contains the information for the Errors per Row Count (EpRC) for the number of code word errors on the highest failing row. REC[5:0] indicates error counts within a range. REC0 is set to "1" if REC0min (the RETC defined in Table 155) has been reached, but the fail count is less than or equal to REC0max = 2 * RETC - 1. Likewise, the min values of REC[5:1] are defined as REC[*x*]min = RETC * 2^x, and max values are defined as REC[*x*]max = 2 * (RETC * 2^x) - 1. The exception is $REC5_{max}$, which is unlimited. The corresponding bit will be set if the error count is within the required range.

4.37.4 ECS Error Tracking (cont'd)

Table 154 — MR16-MR19 Address of Row with Max Errors and Error Count

	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
MR16	R7	R6	R5	R4	R3	R2	R1	R0
MR17	R15	R14	R13	R12	R11	R10	R9	R8
MR18	RFU	BG2	BG1	BG0	BA1	BA0	R17	R16
MR19	RFU	RFU	REC5	REC4	REC3	REC2	REC1	REC0

Table 155 — Row Error Threshold Count (RETC)

	Error Count
Row Error Threshold Count (RETC)	4

The error counters (ECC Error Counter and ECC Errors per Row Counter) reset each time the bank group counter wraps. This process will occur on the ECS operation following the ECS operation that processed the last row in the last bank in the last bank group. The MR16:20 are not cleared after being read from, they will retain the most recent written data until they are rewritten during a subsequent bank group wrap or reset by either issuing a RESET or ECS Reset Counters.

4.37.5 3DS Operation

The ECS feature supports 3DS stacking where the Chip ID, MR14 OP[3:0] (CID3:0 respectively), command bits steer the ECS command to the proper mode registers MR14-MR20 within the die stack. The CID[3:0] bits will be ignored for MRW commands to MR14 or MR15, resulting in identical transparency settings for all die in a 3DS stack. The CID[3:0] bits must be set for MRR commands to MR14-MR20 to read out the data from the target die in the 3DS stack. The CID[3:0] bits will also be used by the Manual ECS MPC command. For single die packages, the CID[3:0] bits should all be set to '0'.

Mode register configuration and readout of mode register data requires per DRAM addressing mode.

Broadcasting the Manual ECS MPC command to all die in the stack is not supported. The Manual ECS MPC command to command spacing requires waiting tECSc, even to different die in the stack. The only commands allowed during t_{ECSc} for a manual ECS operation are ODT NT commands.

4.37.6 ECS Operation with PASR Support

PASR has been deprecated starting with spec working revision 1.90, JESD79-5C-v1.30. All MR60 bits will behave as RFU on devices that do not support PASR.

Segments which are masked are not guaranteed to retain their data if Self Refresh is entered. If Automatic ECS (MR14:OP[7]=0B) or Automatic ECS in Self Refresh (MR15:OP[3]=1B) is enabled, ECS scrubbing will still occur in unmasked segments while in Self Refresh, but the DRAM is not required to execute the ECS on the masked segments. ECS Transparency may not produce accurate results if any mak bit is set. Additionally, upon exit of Self Refresh with masked segments, the masked segments will need to be initialized with known data and the ECS counters will need to be reset, if accurate ECS data is required during the next scrub through the full array.

4.38 CRC

4.38.1 CRC Polynomial and Logic Equation

DDR5 supports CRC for write and read operations. Write and read CRC can be enabled by separate mode register bits. Write CRC and data mask functions are not supported at the same time and cannot be enabled together.

The CRC polynomial used by DDR5 is the ATM-8 HEC, X^8+X^2+X^1+1 that is same as used on DDR4. A combinatorial logic block implementation of this 8-bit CRC for 64-bits of data contains 242 two-input XOR gates contained in eight 6 XOR gate deep trees.

Table 156 shows error detection coverage of DDR5 CRC.

4.38.1 CRC Polynomial and Logic Equation (cont'd)

Table 156 — Error Detection Details

Error Type	Detection Capability
Random Single Bit Error	100%
Random Double Bit Error	100%
Random Odd Count Error	100%
Random Multi-Bit Error within Two adjacent Transfers	100%

CRC COMBINATORIAL LOGIC EQUATIONS

```
module CRC8_D64;
// polynomial: (0 1 2 8)
// data width: 64
// convention: the first serial data bit is D[63]
// initial condition all 0 implied
function [7:0]
nextCRC8_D64;
input [63:0] Data;
reg [63:0] D;
reg [7:0] NewCRC;
begin
D = Data
;
NewCRC[0] = D[63] ^ D[60] ^
D[56] ^ D[54] ^ D[53] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^
D[45] ^ D[43] ^ D[40] ^ D[39] ^ D[35] ^ D[34] ^ D[31] ^
D[30] ^ D[28] ^ D[23] ^ D[21] ^ D[19] ^ D[18] ^ D[16] ^
D[14] ^ D[12] ^ D[8] ^ D[7] ^ D[6] ^ D[0] ;
NewCRC[1] = D[63] ^ D[61] ^ D[60] ^ D[57] ^
D[56] ^ D[55] ^ D[52] ^ D[51] ^ D[48] ^ D[46] ^ D[45] ^
D[44] ^ D[43] ^ D[41] ^ D[39] ^ D[36] ^ D[34] ^ D[32] ^
D[30] ^ D[29] ^ D[28] ^ D[24] ^ D[23] ^ D[22] ^ D[21] ^
D[20] ^ D[18] ^ D[17] ^ D[16] ^ D[15] ^ D[14] ^ D[13] ^
D[12] ^ D[9] ^ D[6] ^ D[1] ^ D[0];
NewCRC[2] = D[63] ^ D[62] ^ D[61] ^ D[60] ^
D[58] ^ D[57] ^ D[54] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
D[44] ^ D[43] ^ D[42] ^ D[39] ^ D[37] ^ D[34] ^ D[33] ^
D[29] ^ D[28] ^ D[25] ^ D[24] ^ D[22] ^ D[17] ^ D[15] ^
D[13] ^ D[12] ^ D[10] ^ D[8] ^ D[6] ^ D[2] ^ D[1] ^ D[0];
NewCRC[3] = D[63] ^ D[62] ^ D[61] ^ D[59] ^
D[58] ^ D[55] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^ D[45] ^
D[44] ^ D[43] ^ D[40] ^ D[38] ^ D[35] ^ D[34] ^ D[30] ^
D[29] ^ D[26] ^ D[25] ^ D[23] ^ D[18] ^ D[16] ^ D[14] ^
D[13] ^ D[11] ^ D[9] ^ D[7] ^ D[3] ^ D[2] ^ D[1];
NewCRC[4] = D[63] ^ D[62] ^ D[60] ^
D[59] ^ D[56] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[46] ^
D[45] ^ D[44] ^ D[41] ^ D[39] ^ D[36] ^ D[35] ^ D[31] ^
D[30] ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15] ^
D[14] ^ D[12] ^ D[10] ^ D[8] ^ D[4] ^ D[3] ^ D[2];
NewCRC[5] = D[63] ^ D[61] ^ D[60] ^
D[57] ^ D[53] ^ D[51] ^ D[50] ^ D[49] ^ D[47] ^ D[46] ^
D[45] ^ D[42] ^ D[40] ^ D[37] ^ D[36] ^ D[32] ^ D[31] ^
D[28] ^ D[27] ^ D[25] ^ D[20] ^ D[18] ^ D[16] ^ D[15] ^
D[13] ^ D[11] ^ D[9] ^ D[5] ^ D[4] ^ D[3];
NewCRC[6] = D[62] ^ D[61] ^ D[58] ^
D[54] ^ D[52] ^ D[51] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
D[43] ^ D[41] ^ D[38] ^ D[37] ^ D[33] ^ D[32] ^ D[29] ^
D[28] ^ D[26] ^ D[21] ^ D[19] ^ D[17] ^ D[16] ^ D[14] ^
D[12] ^ D[10] ^ D[6] ^ D[5] ^ D[4];
NewCRC[7] = D[63] ^ D[62] ^ D[59] ^
D[55] ^ D[53] ^ D[52] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^
D[44] ^ D[42] ^ D[39] ^ D[38] ^ D[34] ^ D[33] ^ D[30] ^
D[29] ^ D[27] ^ D[22] ^ D[20] ^ D[18] ^ D[17] ^ D[15] ^
D[13] ^ D[11] ^ D[7] ^ D[6] ^ D[5];
nextCRC8_D64 = NewCRC;
```

4.38.2 CRC Data Bit Mapping for x4 Devices

Figure 161 shows detailed bit mapping for a x4 device. This bit mapping is common between write and read CRC operations.

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7

Figure 161 — CRC Bit Mapping for x4 Device

4.38.3 CRC Data Bit Mapping for x8 Devices

Figure 162 shows detailed bit mapping for a x8 device. This bit mapping is common between write and read CRC operations. x8 devices have two DQ nibbles and each DQ nibble has its own eight CRC bits to protect 64 data bits. Therefore, a x8 device will have two identical CRC trees implemented.

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7

Figure 162 — CRC Bit Mapping for x8 Device

4.38.4 CRC Data Bit Mapping for x16 Devices

Figure 163 shows detailed bit mapping for a x16 device. This bit mapping is common between write and read CRC operations. x16 devices have four DQ nibbles and each DQ nibble has its own eight CRC bits to protect 64 data bits. Therefore, a x16 device will have four identical CRC trees implemented.

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ8	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ9	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ10	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ11	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ12	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ13	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ14	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ15	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7

Figure 163 — CRC Bit Mapping for x16 Device

4.38.5 Write CRC for x4, x8, and x16 Devices

The controller generates the CRC checksum and forms the write data frames as shown in Clause 4.38.2 to Clause 4.38.4.

Write CRC function can be enabled or disabled per each nibble independently in x8 device. There are two separate write CRC enable MR bits (for upper and lower nibbles) defined for x8. When at least one of two write CRC enable bits is set to '1' in x8, the timings of write CRC enable mode is applied to the entire device (i.e. both nibbles). When write CRC is enable in one nibble and disabled in the other nibble in x8, then the DRAM does not check CRC errors on the disabled nibble, and hence the ALERT_n signal and any internal status bit related to CRC error is not impacted by the disabled nibble.

In case of x4 or x16, only one of two write CRC enable bit is used as defined in the MR50 table and notes. The unused write CRC enable bit is don't care in x4 and x16, i.e., MR50 OP[2] is set to low for x4 and x16 devices.

The DRAM checks for an error in received code words per each write CRC enabled nibble by comparing the received checksum against the computed checksum and reports errors using the ALERT_n signal if there is a mismatch in any of the nibbles.

DRAM can write data to the DRAM core without waiting for CRC check for full writes. If bad data is written to the DRAM core then controller will retry the transaction and overwrite the bad data. Controller is responsible for data coherency.

There is no write latency adder when write CRC is enabled.

4.38.6 Write CRC Auto-disable

Write CRC auto-disable mode is enabled by programming the Write CRC auto-disable mode enable bit MR50:OP[4] to '1'. When this mode is enabled, the DDR5 SDRAM counts the number of Write CRC error occurrences per device, regardless of configuration (x4, x8, or x16). When the number of Write CRC errors exceeds the Write CRC Auto-Disable Threshold (between 0 and 127) as programmed in MR51:OP[6:0], the DDR5 SDRAM disables Write CRC error checking of all nibbles and sets the Write CRC auto-disable status bit MR50:OP[5] to '1'. To exceed the Write CRC Auto-Disable Threshold, the number of Write CRC errors must occur within the Write CRC Auto-Disable Window described below.

Once the CRC auto-disable threshold is reached, the DRAM does not drive ALERT_n low on subsequent Write CRC errors until Write CRC error checking is re-enabled. However, due to DRAM internal timing constraints, the DRAM may drive ALERT_n low on the first CRC error that exceeds the CRC auto-disable threshold.Additionally, if the CRC auto-disable threshold is reached and the DDR5 SDRAM was already driving ALERT_n to low due to the current or a previous Write CRC error, then ALERT_n may be released upon satisfying CRC_ALERT_PW_min.

Unless the Write CRC auto-disable status bit is set, the Write CRC error counter is reset after the predetermined number of writes between 0 and 127, where 0 means an infinite window, as programmed in MR52:OP[6:0], so that the Write CRC error count will accumulate during each Write CRC Auto-Disable Window. Once the Write CRC auto-disable status bit is set, the write CRC error checking is not re-enabled at the end of the Write CRC Auto-Disable Window, even though the Write CRC error counter is reset below the threshold value.

Write CRC error checking can be re-enabled by resetting the Write CRC auto-disable status bit MR50:OP[5] to '0'. This will reset the Write CRC error counter and restart the Write CRC Auto-Disable Window.

Prior to changing the Write CRC Auto-Disable Threshold as programmed in MR51:OP[6:0] or the Write CRC Auto-Disable Window as programmed in MR52:OP[6:0], the host shall disable the Write CRC Auto-Disable mode, MR50:OP[4]=0. Once the updated values have been programmed in MR51 and/or MR52, Write CRC Auto-Disable mode can be (re)enabled, MR50:OP[4]=1. Disabling the Write CRC Auto-Disable mode, if enabled, will reset the DRAM's Write CRC error counter and restart the Write CRC Auto-Disable Window. However, if the Write CRC auto-disable status bit had previously been set to '1', MR50:OP[5]=1, the host is required to set MR50:OP[5]=0 to resume error counting.

Changes to the Write CRC auto-disable threshold (MR51) and window (MR52) settings are only allowed when the CRC Write auto-disable mode is disabled (MR50[4]=0).

When Write CRC auto-disable mode is disabled, MR50:OP[4] = 0, Write CRC error counters may remain at reset values even if Write CRC errors occur.

4.38.7 Read CRC for x4, x8, and x16 Devices

The DDR5 SDRAM generates the CRC checksum and forms the read data frames as shown in Clause 4.38.2 to Clause 4.38.4. The controller can check for an error in received code words per nibble by comparing the received checksum against the computed checksum and if there is a mismatch in any of nibbles then controller may retry the transaction.

Read latency adder when read CRC is enabled depends on data rate as shown in Table 157.

Table 157 — Read CRC Latency Adder

Data Rate (MT/s)	Read CRC Latency Adder (nCK)
1980 MT/s ≤ Data Rate ≤ 2100 MT/s	0
2933 MT/s ≤ Data Rate ≤ 6000 MT/s	0
6000 MT/s < Data Rate ≤ 9200 MT/s	2

The host shall accordingly update MR0:OP[7:2] with the Read CRC Latency Adder when Read CRC is enabled.

4.38.8 CRC Burst Order

When Write CRC is enabled, the CRC bits are calculated based on the sequential burst address order of the write data for the Write command. This sequential order is '0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F' in BL16, and '0,1,2,3,4,5,6,7,T,T,T,T,T,T,T,T' or '8,9,A,B,C,D,E,F,T,T,T,T,T,T,T,T' in BC8 OTF.

When Read CRC is enabled, the DDR5 SDRAM's CRC generator overrides the CA burst order bits C3 and C2 to '00', and CRC bits are calculated based on the sequential burst address order of the read data for the Read command. This sequential order is '0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F' in BL16, and '0,1,2,3,4,5,6,7,T,T,T,T,T,T,T,T' or 'T,T,T,T,T,T,T,T,8,9,A,B,C,D,E,F' in BC8 OTF. The override values do not modify the actual data burst ordering, and are only used for the CRC calculations. Actual data burst follows the burst order as indicated by C3 and C2 in the Read command.

4.38.9 Write CRC Error Handling

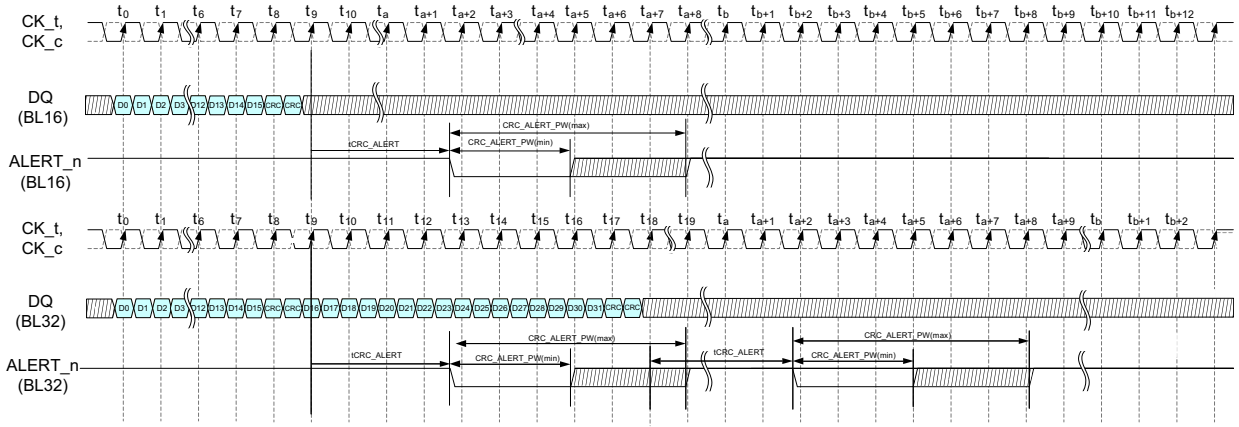
When DRAM detects CRC error on received code words in any of nibbles, then it drives ALERT_n signal to ‘0’ for 12-20 clocks.

The latency to ALERT_n signal is defined as tCRC_ALERT in Figure 164.

DRAM will set Write CRC Error Status bit in A[3] of MR50 to '1' upon detecting a CRC error. The Write CRC Error Status bit remains Group At '1' until the host clears it explicitly using an MRW command.

The controller upon seeing an error as a pulse width will retry the write transactions. The controller understands the worst-case delay for ALERT_n (during initialization) and can back up the transactions accordingly or the controller can be made more intelligent and try to correlate the write CRC error to a specific rank or a transaction. The controller is also responsible for opening any pages and ensuring that retrying of writes is done in a coherent fashion.

The pulse width may be seen longer than 12-20 clocks at the controller if there are multiple CRC errors as the ALERT_n is a daisy chain bus.



NOTES:

1. CRC_ALERT_PW is specified from the point where the DRAM starts to drive the signal low to the point where the DRAM driver releases and the controller starts to pull the signal up.
2. Timing diagram applies to x4, x8 and x16 devices.

Figure 164 — CRC Error Reporting Timing Diagram

Table 158 — CRC Error Handling Timing Parameters

Symbol	Description	Min	Max	Unit
tCRC_ALERT	CRC Alert Delay Time	3	13	ns
CRC_ALERT_PW	CRC Alert Pulse Width	12	20	nCK

4.38.10 CRC Bit Mapping in BC8 Mode

CRC bits are always transferred on 17th and 18th UI, in BC8 mode. When read CRC is enabled during BC8 read, DQ bits are driven high and DQS is toggled by DRAM during the chopped data bursts. When write CRC is enabled during BC8 write, DQ bits must be driven high and DQS must be toggled by controller during the chopped data bursts. In BC8 mode, read CRC and write CRC bits are calculated with the inputs to the CRC engine for the chopped data bursts replaced by all '1's.

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7

Figure 165 — CRC Bit Mapping in BC8 Modes for x4 Device

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7

Figure 166 — CRC Bit Mapping in BC8 Modes for x8 Device

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ8	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ9	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ10	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ11	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ12	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ13	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ14	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ15	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7

Figure 167 — CRC Bit Mapping in BC8 Modes for x16 Device

4.38.11 CRC Bit Mapping in BL32 Mode

In BL32 mode, CRC bits are separately calculated for the first half and the second half of the data. CRC bits for the first half of the data are transferred on 17th and 18th UI, and CRC bits for the second half of the data are transferred on 35th and 36th UI.

4.39 Loopback

With Loopback, DDR5 can feed a received signal or data back out to an external receiver for multiple purposes. Loopback allows the host (memory controller or test instrument) to monitor data sent to the DRAM. Loopback Normal Output Mode requires that the data be sent to the Loopback path before sending it to the core so no READ/WRITE commands are required for Loopback to be operational (no data is stored in the array nor retrieved from the array). Alternatively, Loopback Write Burst Output Mode only generates Loopback data on Write commands during normal operation, where data is written to the array. There are also inherent limitations when characterizing the receiver using statistical analysis methods such as Bit Error Rate (BER) analysis. At BER=1E-16, for example, (1) there is not enough memory depth in the DRAM to store all the 1E+16 data; (2) the amount of time to perform multiple WRITE/READ commands to/from the memory is prohibitively long; (3) since the amount of time involved performing these operations is much longer than the DRAM refresh rate interval, the host or memory controller must also manage Refreshes during testing to ensure data retention; and (4) limited pattern depth means limited Inter Symbol Interference (ISI) and limited Random Jitter (Rj), and, therefore, limited errors at the receiver. Use of the Loopback feature is a necessity for characterizing the receiver without the limitations and complexities of other traditional validation methods. Loopback can also be used during “normal” operation, i.e., during training and when an operating system is loaded.

4.39.1 Loopback Output Definition

The Loopback requires two output pins (one single-ended Loopback strobe LBDQS and one single-ended Loopback data LBDQ).

The default RTT state for Loopback is RTT_OFF, designated by MR36:OP[2:0] = 000B. In this state, both the LBDQS and LBDQ outputs are disabled. If the Loopback pins of several DDR5 SDRAM devices are connected together and the “end” device needs termination, there is an RZQ/5 (48 ohms) option available by setting MR36:OP[2:0] = 101B.

Selecting a Loopback Select Phase A(MR53:OP[6:5]=00B) and Output value via MR53:OP[4:0] other than the default, Loopback Disabled(MR53:OP[4:0]=00000B), will result in the LBDQS and LBDQ pins to transition from the RTT_OFF to a DRAM Drive State.

Before changing the Loopback Output Select from upper byte to lower byte or vice versa, host shall set Loopback Output Select to MR53:OP[4:0]=00000B to make Loopback mode be Disabled.

The LBDQS output will transition with the differential input crossing point of DQS_t/DQS_c for x4 and x8 device configurations, plus latency. LBDQS will transition with DQSL_t/DQSL_c for x16 devices if DML or a DQL is selected for output, or with DQSU_t/DQSU_c for x16 devices if DMU or a DQU is selected for output. If an RFU output is selected, or if DMU or a DQU is selected on a x4 or x8 device where DQSU_t/DQSU_c are not valid, LBDQS will remain in a DRAM Drive State.

The LBDQ output will transition with the receiver data state of the DM or DQ pin selected by MR53:OP[4:0]. If an RFU output is selected, or if an invalid output for device configuration is selected, the LBDQ output will remain in a DRAM Drive State.

Table 159 — Loopback Output Definition

Condition	LBDQS	LBDQ	NOTE
Loopback Disabled	RTT_Loopback	RTT_Loopback	
Loopback Enabled	Selected Phase	Selected Phase and Selected DQ	1
NOTE 1 Selection of an unsupported DM/DQ for the device configuration may result in LBDQS toggling and the LBDQ in a driven state.			

4.39.2 Loopback Phase

Due to the high data rates of the DDR5 SDRAM, Loopback may be implemented with 2-way or 4-way interleaved outputs. With a 2-way implementation, the DQS and selected DM/DQ will be sampled and output every 1 CK or 2 UI. Similarly, with a 4-way implementation, the DQS and selected DM/DQ will be sampled and output every 2 CK or 4 UI.

To be able to sample all bits with a 2-way or 4-way interleave implementation, the Loopback Select Phase programmed in MR53:OP[6:5] allow selection of the DQS/DM/DQ phase to be output. In 2-way mode, Phase A and Phase B are valid options. In 4-way mode, Phase A, Phase B, Phase C and Phase D, are valid options.

Figure 168 shows an example of a Loopback implementation for 4-way interleave x4 DRAM. This example requires a divided clock to produce DQS_0, DQS_90, DQS_180 and DQS_270. Phase A through D refers to the 4-bit naturally aligned bits in a data stream. The output of the DQ slicer runs at 1/4 the speed as received data. In a 4-way interleave design, the data is received at full speed, but internally the data is latched only at quarter speed. For example, if the input bit stream consists of A, B, C, D, then the multiplexer input “A” receives data bit A and strobe DQS_0; multiplexer input “B” receives data bit B and strobe DQS_90; multiplexer input “C” receives data bit C and strobe DQS_180; and multiplexer input “D” receives data bit D and DQS_270.

4.39.2 Loopback Phase (cont'd)

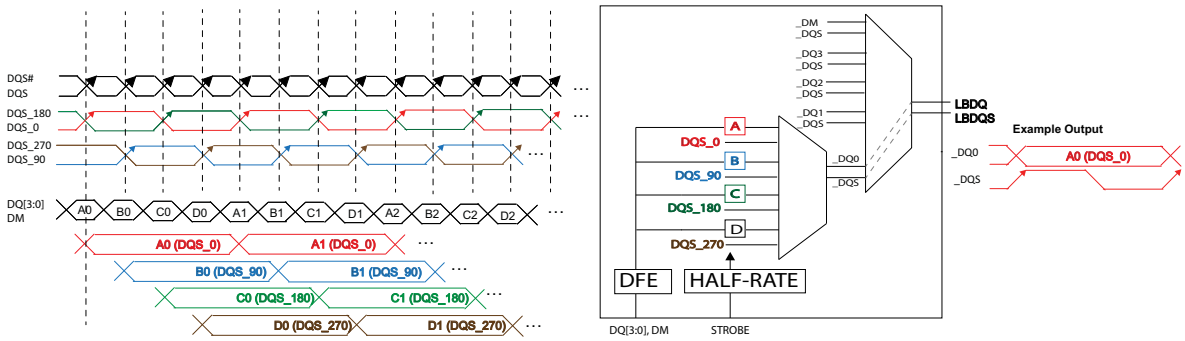


Figure 168 — Example of 4-Way Interleave Loopback Circuit on an x4 SDRAM

4.39.3 Loopback Output Mode

Loopback Output Mode selects whether to output LBDQS and LBDQ in Normal Output Mode or Write Burst Output Mode, based on MR53:OP[7]. In the default Normal Output Mode (MR53:OP[7] = 0B), the selected DM/DQ state is captured with every DQS_t/DQS_c toggle for the selected Loopback Phase. In Write Burst Output Mode (MR53:OP[7] = 1B), the selected DM/DQ state will be output on LBDQ when qualified by the write enable, which means data is only captured during the write burst and not during the preamble or postamble.

4.39.3.1 Loopback Normal Output Mode (Default)

In Normal Output Mode (MR53:OP[7] = 0B), the selected DM/DQ state is captured with every DQS_t/DQS_c toggle for the selected Loopback Phase and output on LBDQ. The LBDQS output will be delayed by *t*LBDLY from the selected DQS_t/DQS_c Loopback Phase. Phase C and D are inverted from Phase A and B, respectively. Since no Write commands are required in Normal Output Mode, MR settings pertaining to preamble, postamble, CWL are ignored by the Loopback function.

Additional requirements for Normal Output Mode:

- Loopback in Normal Output mode is not supported after completing Write Leveling training with Internal Write Timing mode set MR2:OP[7]=1.
- DQS must be driven differentially low (DQS_t low, DQS_c high) prior to entry into Normal Output Mode.
- DQS_t/DQS_c must be continuously driven during Loopback operation. (HiZ state not allowed.)
- Only DSEL and MRW commands applied at command pins during Normal Output Mode.
- RESET is required to exit Loopback Normal Output Mode.

No DFE Reset is assumed after first rising edge of DQS_t. DDR5 SDRAM array data is not guaranteed after entering Normal Output Mode.

4.39.3.2 Loopback Normal Output Mode Timing Diagrams

Loopback Normal Output Mode entry and output example timing diagrams are shown in Figure 169 through Figure 173.

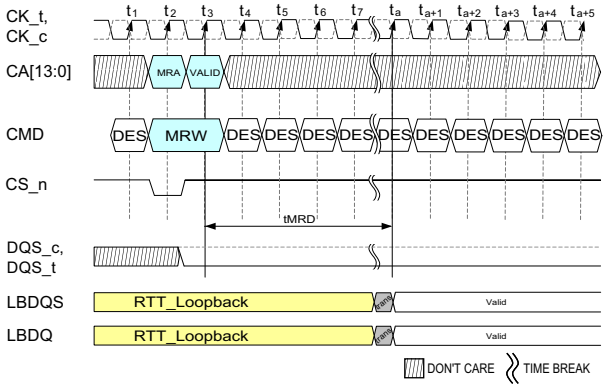


Figure 169 — Loopback Normal Output Mode Entry

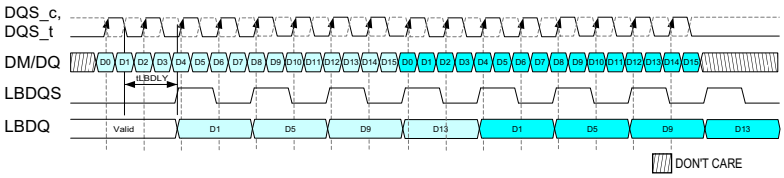


Figure 170 — Loopback Normal Output 4-Way Mode PhaseB Example

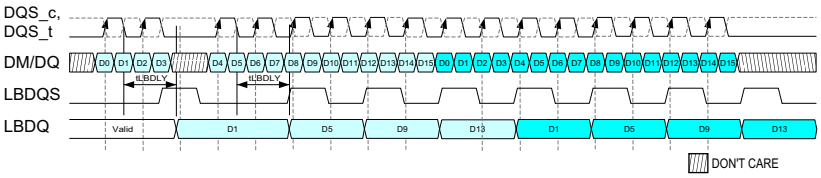


Figure 171 — Loopback Normal Output Mode 4-Way PhaseB 1CK Mid Gap Example

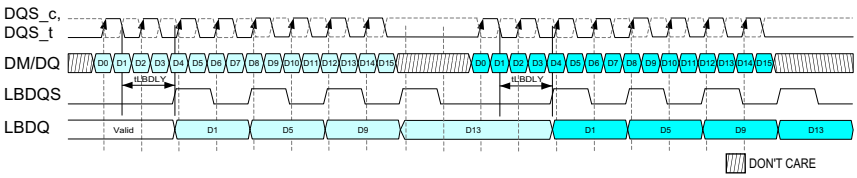


Figure 172 — Loopback Normal Output Mode 4-Way PhaseB 2CK Gap Example

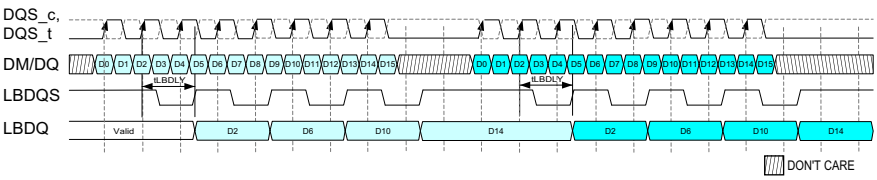


Figure 173 — Loopback Normal Output Mode 4-Way PhaseC 2CK Gap Example

4.39.3.3 Loopback Normal Mode with CRC Output Timings

Loopback Normal Output Mode with CRC, timing diagram examples are shown in Figure 174 through Figure 176.

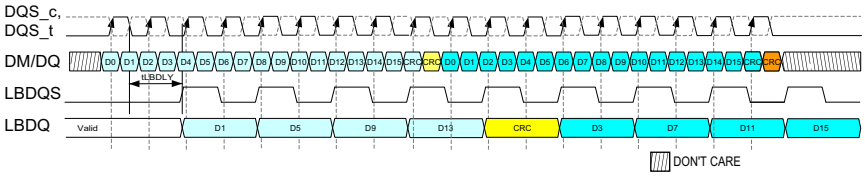


Figure 174 — Loopback Normal Output Mode 4-Way PhaseB with CRC, no Gap Example

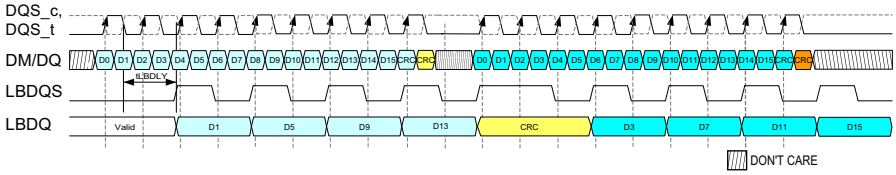


Figure 175 — Loopback Normal Output Mode 4-Way PhaseB with CRC,1CK Gap Example

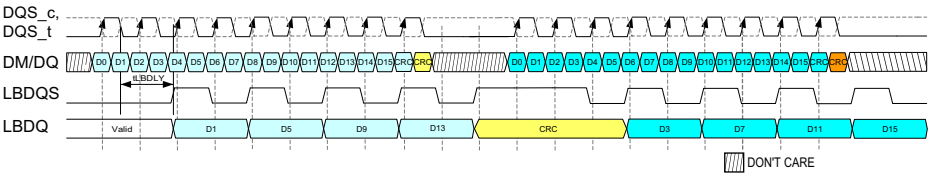


Figure 176 — Loopback Normal Output Mode 4-Way PhaseB with CRC, 2CK Gap Example

4.39.3.4 Loopback Write Burst Output Mode

In Write Burst Output Mode (MR53:OP[7] = 1B), Loopback data is only generated during the write burst, so it is effectively masked for the DQS toggles during the preamble or postamble. Normal Write operation for the Command, DQS and DM/DQ is assumed. MR settings pertaining to preamble, postamble, CWL apply, as they do for any Write command.

To prevent Loopback interference on the DRAM within the normal data path, the DRAM optionally may output the 2nd preamble pulse for the special case of WPRE=4CK and selection of Phase C or D for Data Burst Bit phase alignment or Phase A or B for Strobe phase alignment. With this behavior, all phases are inverted from normal behavior.

Implementation of 2-way or 4-way interleave Loopback introduces complexity in Write Burst Mode when the DQS toggle is not continuous. If the DQS toggle is continuously generated by Write commands spaced BL/2, Loopback will align the LBDQS/LBDQ output with the selected phase for all write bursts. In cases where gaps in Write commands are greater than BL/2, the phase shall be determined by the analysis of the conditions.

Table 160 — Loopback Output Phase

Write to Write Separation	Phase	NOTE
X = BL/2	Selected	
X >= BL/2	Determined via analysis of specific conditions	1

NOTE 1 Specific conditions include 2-way/4-way interleave implementation, selected phase, data rate, preamble, postamble and write burst gap duration.

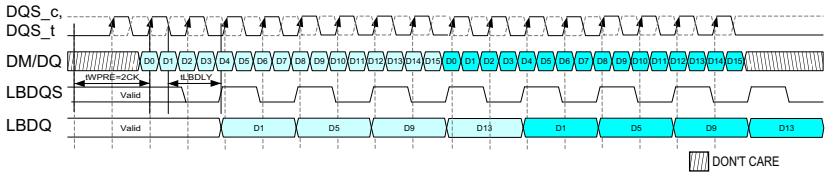
In the case where continuous bursts are not issued in Loopback Write Burst Output Mode, selection of Phase C or D for Data Burst Bit phase alignment or Phase A or B for Strobe phase alignment may result in the last tLBQSH width of a burst that does not comply with spec.

Additional requirements for Write Burst Output Mode:

- Write Leveling training is required prior to Write Burst Loopback operation.
- All Write timing and voltage requirements must be followed. Failure to meet this requirement results in unknown data written to DRAM, and the Loopback pins may not output the captured input data as expected.

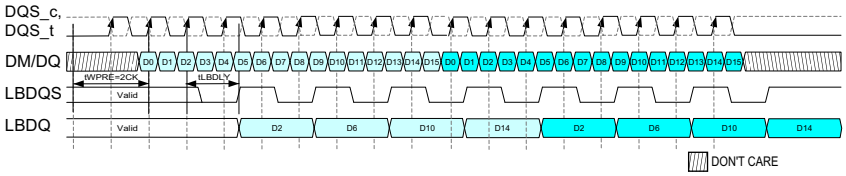
4.39.3.5 Loopback Write Burst Output Mode Timing Diagrams

Loopback Write Burst Output Mode timing diagram examples are shown in Figure 177 through Figure 180. The DM/DQ signal is shown as “Don’t Care” before the first Write data bit indicating DFE is disabled. When DFE is enabled, the DM/DQ signal shall be high for a minimum of 4UI prior to the first Write data bit for proper DFE synchronization.



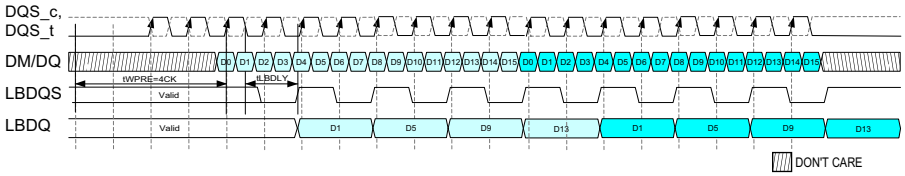
NOTES:
1. The DM/DQ signal is shown as “Don’t Care” before the first Write data bit indicating DFE is disabled. When DFE is enabled, the DM/DQ signal shall be high for a minimum of 4UI prior to the first Write data bit for proper DFE synchronization.

Figure 177 — Loopback Write Burst Output Mode 4-Way PhaseB WPRE=2CK Example



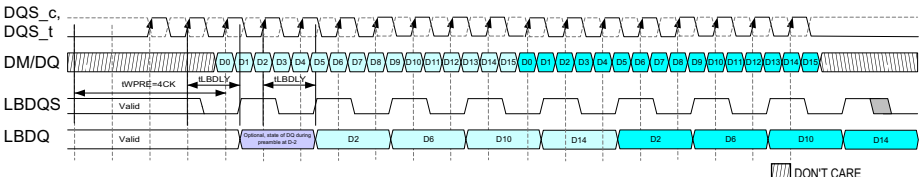
NOTES:
1. The DM/DQ signal is shown as “Don’t Care” before the first Write data bit indicating DFE is disabled. When DFE is enabled, the DM/DQ signal shall be high for a minimum of 4UI prior to the first Write data bit for proper DFE synchronization.

Figure 178 — Loopback Write Burst Output Mode 4-Way PhaseC WPRE=2CK Example



NOTES:
1. The DM/DQ signal is shown as “Don’t Care” before the first Write data bit indicating DFE is disabled. When DFE is enabled, the DM/DQ signal shall be high for a minimum of 4UI prior to the first Write data bit for proper DFE synchronization.

Figure 179 — Loopback Write Burst Output Mode 4-Way PhaseB Data Burst Bit and PhaseD Strobe Alignment WPRE=4CK Optional Example

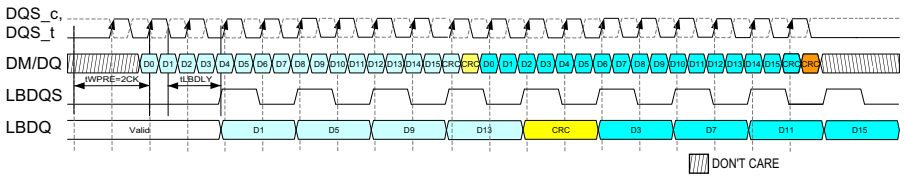


NOTES:
1. The DM/DQ signal is shown as “Don’t Care” before the first Write data bit indicating DFE is disabled. When DFE is enabled, the DM/DQ signal shall be high for a minimum of 4UI prior to the first Write data bit for proper DFE synchronization.

Figure 180 — Loopback Write Burst Output Mode 4-Way PhaseC Data Burst Bit and PhaseA Strobe Alignment WPRE=4CK Optional Example

4.39.3.6 Loopback Write Burst with CRC Output Mode Timing Diagrams

Loopback Write Burst Output Mode with CRC, timing diagram example is shown in Figure 181.



NOTES:
1. The DM/DQ signal is shown as “Don’t Care” before the first Write data bit indicating DFE is disabled. When DFE is enabled, the DM/DQ signal shall be high for a minimum of 4UI prior to the first Write data bit for proper DFE synchronization.

Figure 181 — Loopback Write Burst with CRC Output Mode 4-Way PhaseB with CRC, No Gap Example

4.39.4 Loopback Timing and Levels

The LBDQS output will be delayed from the selected DQS_t/DQS_c Loopback Phase. The timing parameter, *t*LBDLY, is shown in Table 161.

Table 161 — Loopback LBDQS Output Timing

Speed		DDR5-3200 to 9200		Units	NOTE
Parameter	Symbol	Min	Max		
Loopback Timing					
LBDQS Delay from Selected DQS Loopback Phase	tLBDLY	-	20	ns	

The interaction between LBDQS and LBDQ is described in section 9.10 Loopback Output Timing.

ODT for Loopback is described in Section 5.5 On-Die Termination for Loopback Signals. Output driver electrical characteristics for Loopback is described in Section 9.2 Output Driver DC Electrical Characteristics for Loopback Signals LBDQS, LBDQ.

4.40 CA_ODT Strap Operation

With the introduction of on-die termination for CA/CS/CK on DDR5 DRAMs, the setting of the termination values per DRAM will be different depending on the configuration of DRAMs on the DIMM or system board. The CA_ODT pin enables the distinction of two “sets” of CA/CS/CK ODT settings. When the CA_ODT pin is strapped to a constant VSS setting on the DIMM or board, the CA/CS/CK ODT settings will be referred to as “Group A”. When the CA_ODT pin is strapped to a constant VDD setting on the DIMM or system board, the CA/CS/CK ODT settings will be referred to as “Group B”. Typical usage would be to apply a weak termination setting to Group A devices and a stronger termination setting to Group B devices, which would be at the end of the fly-by routing on the DIMM. To support these different settings, two sets of MPC opcodes will be used to target either Group A or Group B devices. In addition to these separate “Groups” of devices based on the CA_ODT pin, the PDA commands will also be supported. However, the correct combination of the PDA Select ID and MPC opcode must be used according to the CA_ODT pin value.

For DDP device, CA_ODT package pin ties to both top die and bottom die CA_ODT bond pads. CS_n and CS1_n being defined in DDP package ballout. CS is not shared between dies, and each die terminated individually. CK is shared between both dies and both dies terminated. CA is shared between both dies and both dies terminated. host can program optimal ODT value after initialization.

4.40 CA_ODT Strap Operation (cont'd)

The CA_ODT pin is defined in the pinlist as follows:

Table 162 — CA_ODT Pinlist

Pin Name	Input/ Output	Description
CA_ODT	Input	ODT for Command and Address. Apply Group A settings if the pin is connected to VSS and apply Group B settings if the pin is connected to VDDQ

MR32 is defined as follows to reflect the need to be able to read the CA_ODT strap value:

Table 163 — MR32 Definition

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	CA_ODT Strap Value	CS ODT			CK ODT		

MR33 is defined as follows:

Table 164 — MR33 Definition

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		DQS_RTT_PARK			CA ODT		

If the CA_ODT Strap Value for the DRAM is 0, the CK ODT, CS ODT, and CA ODT values will reflect the default settings for "Group A" ODT values, or will reflect what has been written to these mode registers via the MPC opcodes for Group A CK/CS/CA ODT settings.

If the CA_ODT Strap Value for the DRAM is 1, the CK ODT, CS ODT, and CA ODT values will reflect the default settings for "Group B" ODT values, or will reflect what has been written to these mode registers via the MPC opcodes for Group B CK/CS/CA ODT settings.

4.40.1 CA/CS/CK ODT Settings

The MPC opcodes in Table 165 will be used to set the "Group A" and "Group B" RTT_CA, RTT_CS, and RTT_CK values (to be included in the MPC section)

Table 165 — MPC Opcodes

Function	Operand	Data	Notes
Initialization and Training Modes	OP[7:0]	... 0010 0xxxB: Group A RTT_CK = xxx (See MR32:OP[2:0] for encoding) 0010 1xxxB: Group B RTT_CK = xxx (See MR32:OP[2:0] for encoding) 0011 0xxxB: Group A RTT_CS = xxx (See MR32:OP[5:3] for encoding) 0011 1xxxB: Group B RTT_CS = xxx (See MR32:OP[5:3] for encoding) 0100 0xxxB: Group A RTT_CA = xxx (See MR33:OP[2:0] for encoding) 0100 1xxxB: Group B RTT_CA = xxx (See MR33:OP[2:0] for encoding) ...	

4.41 Duty Cycle Adjuster (DCA)

DDR5 SDRAM supports a mode register adjustable DCA to allow the memory controller to adjust the DRAM internally generated DQS clock tree and DQ duty cycle to compensate for systemic duty cycle error of all DQS and DQs.

The DQS DCA is located before the DQS clock tree or equivalent place. The DCA requires a locked DLL state and will affect DQS and DQ duty cycle during the following operations.

- Read
- Read Preamble Training
- Read Training Pattern
- Mode Register Read

The controller can adjust the duty cycle through all the DCA mode registers and can determine the optimal Mode Register setting for DCA in multiple different ways.

In case of 4-phase internal clocks, for example, since QCLK(90˚)/IBCLK(180˚)/QBCLK(270˚) are adjusted based on ICLK(0˚), the controller can first confirm that the first BL is synchronized with ICLK(0˚), and then perform the full DCA training operation which needs to have an even number of MRR(or Read) - MRR(or Read) timing to avoid confusion whether the first BL is synchronized with ICLK(0˚) or IBCLK(180˚).

4.41.1 Duty Cycle Adjuster Range

The global DCA step range is from -7 to +7, as defined in MR43 and MR44. The actual step size cannot be defined since the variation of duty cycle by changing DCA code is not linear.

Table 166 — DCA Range

Parameter	Min/Avg./Max	Value	Unit	Note
Duty Cycle Adjuster Range	Min	28	ps	1
	Max	56		
NOTE 1 These values are guaranteed by design.				

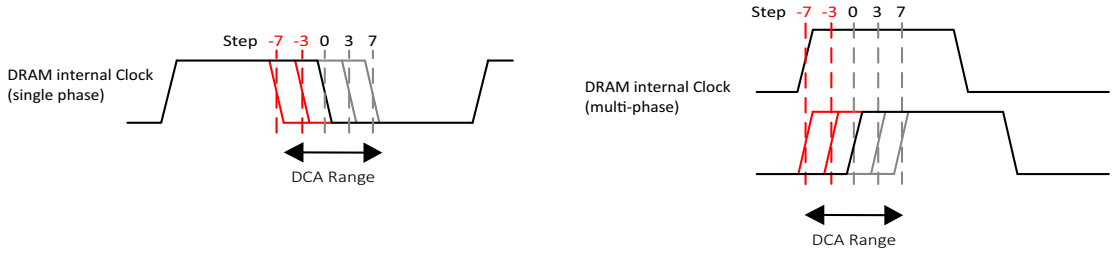


Figure 182 — Duty Cycle Adjuster Range

4.41.2 Relationship between DCA Code Change and Single/Two-phase Internal Clock(s)/DQS Timing

In case of the DQS clock tree used single/two-phase clock(s) scheme, the duty-cycle ratio of all DQS per device can be adjusted directly according to the internal clock(s) controlled by the DCA code. Note that tDQSCK is not changed by DCA code change.

Using a 2-phase clock scheme, the rising edge of the 0° clock is the reference edge, while the 180° clock is adjusted based on 0° clock. The rising edge of 0° clock is for even burst bit data, and the rising edge of 180° clock is for odd burst bit data.

The global DCA adjustment uses the “DCA for single/two-phase clock(s)” mode register bits, MR43:OP[3:0]. A positive DCA adjustment results in a larger duty cycle ratio, while a negative DCA adjustment results in a smaller duty cycle ratio.

4.41.2 Relationship between DCA Code Change and Single/Two-phase Internal Clock(s)/DQS Timing (cont'd)

In addition to the global DCA adjustment, a per-pin DCA adjustment allows an additional step range of -3 to +3, per DQS/DQ. The 2-phase clock per-pin DCA adjustment uses the OP bits [3,1:0] of MR103 (DQSL_t), MR105 (DQSL_c), MR107 (DQSU_t), MR109 (DQSU_c), MR133 (DQL0), MR141 (DQL1), ...,MR253 (DQU7). The per-pin DCA adjustment is additive to the global DCA adjustment, as shown in Table 167.

Table 167 — DCA Range Examples (not All Possible Combinations)

Global DCA Adjustment	Per-Pin DCA Adjustment	Total DCA Adjustment at Pin
DCA Step -3	DCA Step -2	DCA Step -5
DCA Step -2	DCA Step +2	DCA Step 0
DCA Step 0	DCA Step +1	DCA Step +1
DCA Step +2	DCA Step -3	DCA Step -1
DCA Step +4	DCA Step +3	DCA Step +7
DCA Step +7	DCA Step +2	DCA Step +9

Like the global DCA adjustment, the actual step size for the per-pin DCA adjustment cannot be defined since the variation of duty cycle by changing DCA code is not linear, however the per-pin DCA adjustment will be approximately the same as the global DCA adjustment.

Mode register OP bits associated with the IBCLK and QBCLK may not be supported on the DRAM with a 2-phase clock scheme.

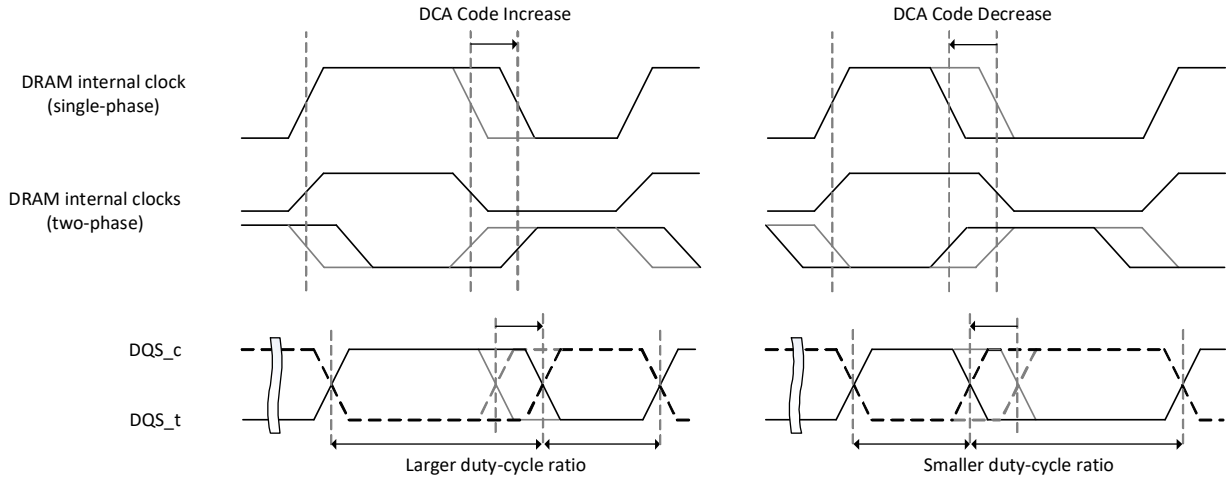


Figure 183 — Relationship between DCA Code Change and the Single/Two-phase Internal Clock(s)/DQS Waveform (Example)

4.41.3 Relationship between DCA Code Change and 4-phase Internal Clock(s)/DQS Timing

In case of the DQS clock tree used 4-phase clocks scheme, the even and odd duty-cycle ratio of all DQS per device can be respectively adjusted since the internal 4-phase clocks can be independently controlled by the DCA code.

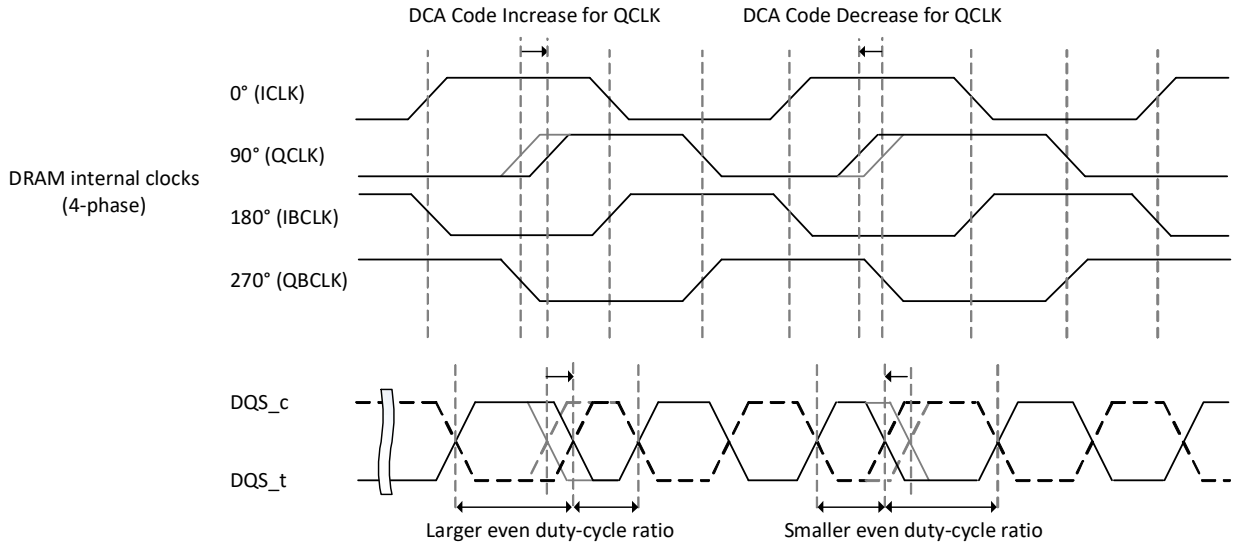


Figure 184 — Relationship between DCA Code Change for QCLK and the 4-phase Internal Clocks/DQS Waveform (Example)

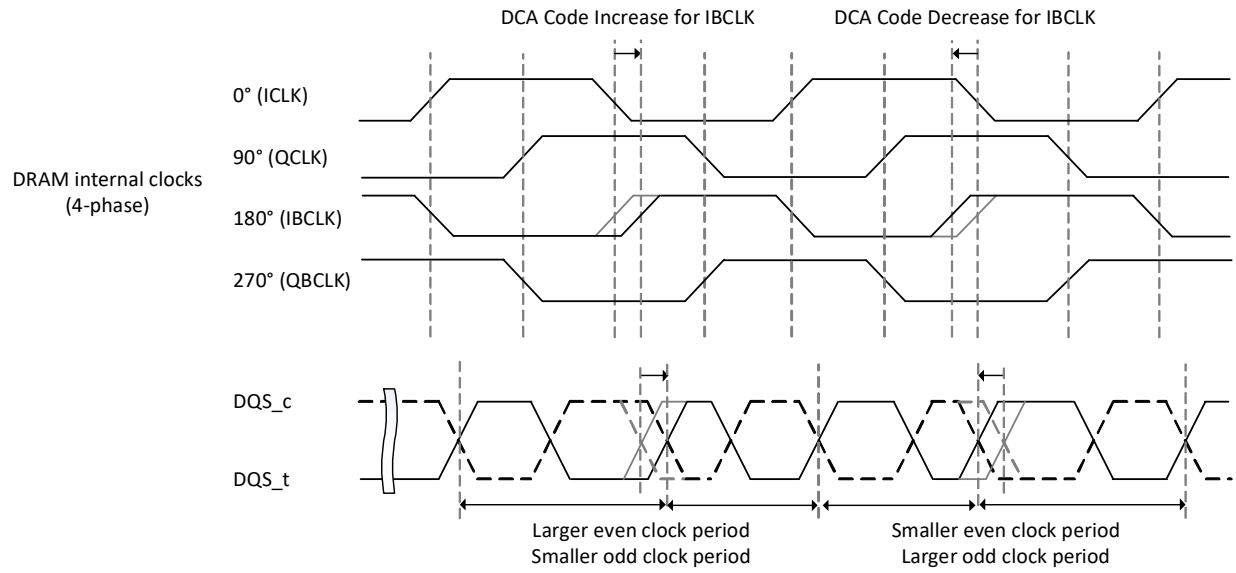


Figure 185 — Relationship between DCA Code Change for IBCLK and the 4-phase Internal Clocks/DQS Waveform (Example)

4.41.3 Relationship between DCA Code Change and 4-phase Internal Clock(s)/DQS Timing (cont'd)

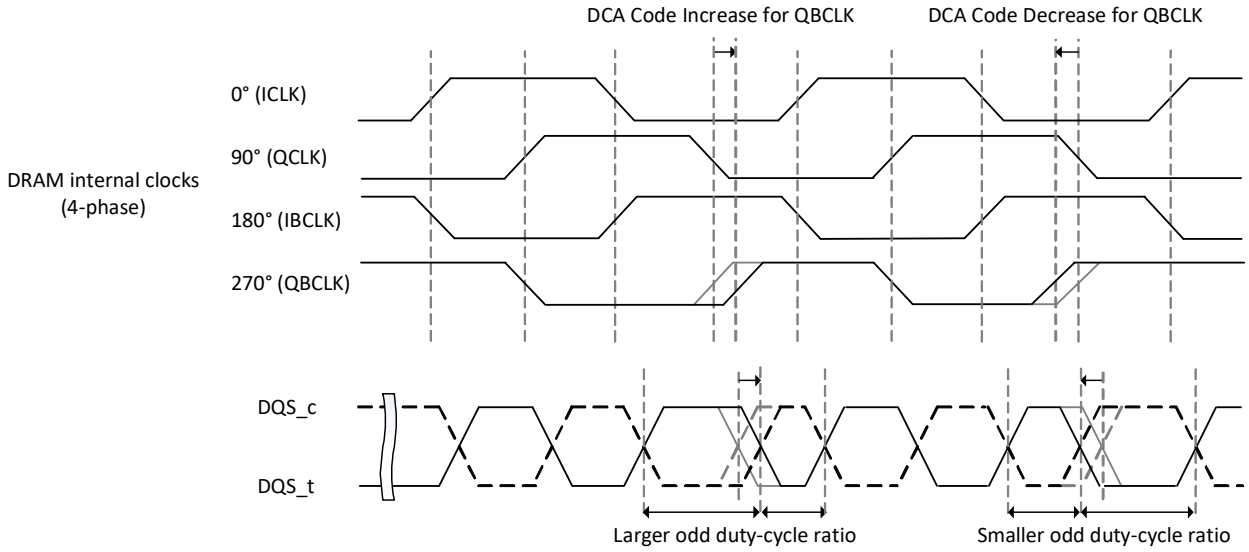


Figure 186 — Relationship between DCA Code Change for QBCLK and the 4-phase Internal Clocks/DQS Waveform (Example)

4.41.4 Relationship between DCA Code Change and DQs Output/DQS Timing

The DQS DCA code change effect to DQ Output as follows. The rising edge of DQS_t affects the even data output. The falling edge of DQS_t affects to the falling edge of the odd data output.

4.42 Refresh Management (RFM)

Periods of high DDR5 DRAM activity may require additional refresh commands to protect the integrity of the DRAM data. The DRAM will indicate the requirement for additional Refresh Management (RFM) by setting read only MR58 opcode bit 0 (Table 168). OP[0]=0 indicates no additional refresh is needed beyond the refresh required in the Refresh Operation section of the specification. OP[0]=1 indicates additional DRAM refresh management is required.

Table 168 — Mode Register Definition for Refresh Management

MR58 OP[0]	Refresh Management (RFM) Requirement
0	Refresh Management (RFM) not required
1	Refresh Management (RFM) required

A suggested implementation of Refresh Management by the controller monitors ACT commands issued per bank to the DRAM. This activity can be monitored as a Rolling Accumulated ACT (RAA) count. Each ACT command will increment the RAA count by 1 for the individual bank receiving the ACT command.

When the RAA counter reaches a DRAM vendor specified Initial Management Threshold (RAAIMT), which is set by the DRAM vendor in the read only MR58 opcode bits 4:1 (Table 169), additional DRAM refresh management is needed. Executing the Refresh Management (RFM) command allows additional time for the DRAM to manage refresh internally. The RFM operation can be initiated to all banks on the DRAM with the RFMab command, or to a single bank address (BA[1:0]) in all bank groups with the RFMsb command. A DRAM with MR58 OP[0]=0 will treat the RFM command as a REF command.

4.42 Refresh Management (RFM) (cont'd)

Table 169 — Mode Register Definition for the RAA Initial Management Threshold (RAAIMT)

MR58 OP[4:1]	RAAIMT Value Normal Refresh Mode	RAAIMT Value FGR Refresh Mode
0000_B-0011_B	RFU	RFU
0100_B	32	16
0101_B	40	20
...	...	...
1001_B	72	36
1010_B	80	40
1011_B-1111_B	RFU	RFU

The RFM command bits are the same as the REF command, except for CA9. If the Refresh Management Required bit is "0", (MR58 OP[0]=0), CA9 is only required to be valid ("V") for a REF command, and the DRAM will treat a RFM command as a REF command. If the Refresh Management Required bit is "1", (MR58 OP[0]=1), CA9="H" executes the REF command and CA9="L" executes either an RFMab command if CA10="L" or an RFMsb command if CA10="H".

The duration of the RFMab commands is dependent upon the DRAM being in Normal or FGR refresh mode, while the RFMsb command is only allowed in FGR refresh mode. *t*RFM,min is equivalent to *t*RFC,min. See Table 170.

Table 170 — t_{RFM} parameters

Refresh Operation	Symbol	Value	Notes
Normal Refresh Management (RFMab)	$t_{RFM1,min}$	$t_{RFC1,min}$	
Fine Granularity Refresh Management (RFMab)	$t_{RFM2,min}$	$t_{RFC2,min}$	
Same Bank Refresh Management (RFMsb)	$t_{RFMsb,min}$	$t_{RFCsb,min}$	

When an RFM command is issued to the DRAM, the RAA counter in any bank receiving the command can be decremented by the RAAIMT value, down to a minimum RAA value of 0 (no negative or "pull-in" of RFM commands is allowed). Issuing an RFMab command allows the RAA count in all banks to be decremented by the RAAIMT value. Issuing an RFMsb command with BA[1:0] allows the RAA count only with that bank address across all bank groups to be decremented by the RAAIMT value

RFM commands are allowed to accumulate or "postpone", but the RAA counter shall never exceed a vendor specified RAA Maximum Management Threshold (RAAMMT), which is set by the DRAM vendor in the read only MR58 opcode bits 7:5 (Table 171). If the RAA counter reaches RAAMMT, no additional ACT commands are allowed to the DRAM bank until one or more REF or RFM commands have been issued to reduce the RAA counter below the maximum value.

Table 171 — Mode Register Definition for RAA Maximum Management Threshold (RAAMMT)

MR58 OP[7:5]	RAAMMT Value Normal Refresh Mode	RAAMMT Value FGR Refresh Mode
000_B-010_B	RFU	RFU
011_B	3x RAAIMT	6x RAAIMT
100_B	4x RAAIMT	8x RAAIMT
101_B	5x RAAIMT	10x RAAIMT
110_B	6x RAAIMT	12x RAAIMT
111_B	RFU	RFU

RFM command scheduling shall meet the same minimum separation requirements as those for the REF command (for example, see Table 69 in the Refresh Operation section).

4.42 Refresh Management (RFM) (cont'd)

An RFM command does not replace the requirement for the controller to issue periodic REF commands to the DRAM, nor does a RFM command affect internal refresh counters and internal bank counters (RFMsb). The RFM commands are bonus time for the DRAM to manage refresh internally. However, issuing a REF command also allows decrementing the RAA counter by the value set by MR59 OP[7:6], as shown in Table 172. Hence, any periodic REF command issued to the DRAM allows the RAA counter of the banks being refreshed to be decremented by the MR59 OP[7:6] setting. Issuing a REFab command allows the RAA count in all banks to be decremented. Issuing a REFsb command with BA[1:0] allows the RAA count only with that bank address in all bank groups to be decremented.

Table 172 — Mode Register Definition for RAA Counter Decrement per REF Command

MR59 OP[7:6]	RAA Counter Decrement per REF Command
00b	RAAIMT
01b	RAAIMT * 0.5
10b	RFU
11b	RFU

No decrement to the RAA count values is allowed for entering/exiting Self Refresh. The per bank count values before Self Refresh is entered remain unchanged upon Self Refresh exit.

4.42.1 Adaptive Refresh Management (ARFM)

DDR5 supports an optional Refresh Management mode called Adaptive RFM (ARFM). Since Refresh Management settings are read only, the Adaptive RFM allows the controller flexibility to choose additional RFM threshold settings, called "RFM Levels". The RFM Levels permit alignment of the controller-issued RFM commands with the in-DRAM management of these commands. MR59:OP[5:4} allows selection of the Adaptive RFM Level, as shown in Table 173.

Table 173 — Mode Register Definition for Adaptive RFM Levels

MR59:OP[5:4]	RFM Level	RFM Requirement	RAAIMT Normal Refresh	RAAMMT Normal Refresh	RAA Decrement per REF Command	Notes
00_B	Default	Default	Default	Default	Default	1, 2
01_B	Level A	RFM Required	RAAIMT-A	RAAMMT-A	RAADEC-A	1, 2, 3
10_B	Level B	RFM Required	RAAIMT-B	RAAMMT-B	RAADEC-B	
11_B	Level C	RFM Required	RAAIMT-C	RAAMMT-C	RAADEC-C	

NOTE 1 RAAIMT values for FGR are half of the normal refresh mode
NOTE 2 RAAMMT values for FGR are double that of the normal refresh mode
NOTE 3 RAAIMT, RAAMMT and RAADEC values for RFM Levels A-C are set by DRAM vendor

The Adaptive RFM mode inherits the RAA counting and decrement attributes of the standard RFM mode, while using the alternate RAAIMT, RAAMMT, and RAADEC for the selected RFM Level. Increasing the RFM Level results in increased need for RFM commands. Level C is highest RFM Level.

Setting the MR59:OP[5:4] bits to something other than the default "00" case will enable the alternative RFM Level for the Adaptive RFM mode. The host shall decrement the Rolling Accumulated ACT (RAA) count to 0, either with RFM or pending REF commands, prior to making a change to the RFM Level.

To inform the host of the RFM settings required as the RFM Level is changed by MR59:OP[5:4], the DRAM modifies the corresponding mode register values for RFM required, RAAIMT, RAAMMT and RAADEC (MR58:OP[0], MR58:OP[4:1], MR58:OP[7:5], MR59:OP[7:6], respectively) for subsequent MRR commands. Mode register values that remain the same as the default setting indicate the default RFM threshold levels are supported at the selected ARFM level.

Adaptive RFM also allows a DRAM shipped with 'RFM not required' (MR58:OP[0]=0) to override that initial setting and enable RFM by programming a non-default RFM Level. The DRAM internally manages the change to treat the RFM command as an RFM command in this special override case, as shown in Table . A DRAM that supports ARFM, even if the device is shipped with 'RFM not required' (MR58:OP[0]=0), will set MR58:OP[0]=1 to indicate the chosen ARFM level is supported.

4.42.1 Adaptive Refresh Management (ARFM) (cont'd)

Table 174 — RFM Commands Perceived by DRAM

Command	MR58:OP[0]	MR59:OP[5:4]	Command Perceived by DRAM	Notes
RFM	0_B	00_B	REF	
RFM	0_B	01_B - 11_B	REF	1
RFM	1_B	00_B	RFM	
RFM	1_B	01_B - 11_B	RFM	1, 2

NOTE 1 If the optional ARFM (MR59:OP[5:4]=01B-11B) is not supported on the DRAM, the command perceived by the DRAM is determined by MR58:OP[0].

NOTE 2 Adaptive RFM enables a DRAM shipped with MR58:OP[0]=0 to override the initial setting and enable RFM by programming a non-default RFM Level. The DRAM will change MR58:OP[0]=1 to indicate the chosen ARFM level is supported.

NOTE 3 If the DRAM requires RFM (MR58:OP[0]=1B) but the optional ARFM is not supported, the DRAM does not change the programmed value in MR58:OP[0] when the host changes ARFM level settings (MR59:OP[5:4]).

NOTE 4 If the DRAM is shipped with MR58:OP[0]=0 (RFM not required), then any time RFM level is default (MR59:OP[5:4]=00), then MR58:OP[0]=0. For non-default RFM levels (MR59:OP[5:4]=01,10,11), MR58:OP[0]=1when ARFM is supported on the DRAM.

4.42.2 Directed Refresh Management (DRFM)

Directed Refresh Management (DRFM) is an optional feature on DDR5 that gives the controller additional flexibility for maintaining data integrity within the DRAM.

The DRFM feature allows the DRAM to capture a host-requested row address, which then is followed by a host-directed RFM command allowing the DRAM to refresh physically adjacent neighboring rows of the requested row address.

When DRFM Enable (DRFE), MR59:OP[0], is set High, DRFM mode is enabled. DDR5 supports two method to sample DRFM address:

1) PREpb - when DRFM is enabled, CA5 becomes a control bit to select between "CA5=H Precharge per Bank" or "CA5=L Precharge per bank plus sampling DRFM address". Executing the PREpb with CA5=L tells the DRAM to sample the currently activated address for DRFM. When DRFM is disabled, CA5 retains CID3 functionality.

2) WRPA/WRA/RDA - when DRFM mode is enabled, CA9 on the second cycle of these two-cycle commands becomes a control bit to select between "CA9=H Auto Precharge" or "CA9=L Auto Precharge plus sampling DRFM address". Executing a Write Pattern, Write or Read command with Auto Precharge and CA9=L on the second cycle samples the currently activated address for DRFM. When DRFM is disabled, CA9 is required to be "V" during the second cycle of there two-cycle commands.

Each DRAM bank has an independent DRFM address register for the DRFM address sample. This DRFM address register is updated with each DRFM address sample to the bank, resulting in the last (most recent) address sample being retained for the hostdirected DRFM command.

Although a PREpb is allowed to a closed bank or a bank that is already in the process of precharging, issuing a PREpb plus DRFM address sample to a closed or precharging bank may result in an unknown address sample, potentially overwriting a prior valid address sample.

Table 175 — Command Truth Table with DRFM Address Sample Commands

Function	Abbreviation	CS_n	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Write Pattern with Auto Precharge	WRPA	L	H	L	L	H	L	H	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	11, 15, 18, 19, 20
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V or DRFM=L	AP=L	H	V	CID3	
Write with Auto Precharge	WRA	L	H	L	H	H	L	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8, 12, 15, 19, 20
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V or DRFM=L	AP=L	WR_ Par-tial=L	V	CID3	
Read with Auto Precharge	RDA	L	H	L	H	H	H	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8, 15, 19, 20
		H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V or DRFM=L	AP=L	V	V	CID3	
Precharge	PREpb	L	H	H	L	H	H	CID3 or DRFM=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	7, 20

4.42.2 Directed Refresh Management (DRFM) (cont'd)

After the DRFM address sample, the host can then issue a DRFM command to service the sampled DRFM address(es). This DRFM command is supplemental to DRAM RFM requirements.

When DRFM is enabled on DDR5, CA5 becomes a control bit to select between "CA5=H RFMab/RFMsb" or "CA5=L DRFMab/ DRFMsb". Executing the RFMab or RFMsb commands with CA5=L tells the DRAM to service the sampled DRFM address for all banks where a DRFM address sample occurred. Any banks without a DRFM address sample will use an address internally sampled by the DRAM. Banks with internally sampled addresses allow the host to decrement the RAA count for those banks. Since DRFM is supplemental, any banks with DRFM address samples do not allow RAA counts to be decremented.

RFMab or RFMsb commands with CA5=H will only use DRAM internally sampled addresses and do not interfere with any DRFM sampled addresses.

When DRFM is disabled, CA5 retains CID3 functionality for RFMab or RFMsb commands.

Table 176 — Command Truth Table with DRFM Commands

Function	Abbreviation	CS_n	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Refresh Management All	RFMab	L	H	H	L	L	H	CID3 or DRFM=L	V	V	V	L	L	CID0	CID1	CID2	3, 20
Refresh Same Bank	REFsb	L	H	H	L	L	H	CID3 or DRFM=L	BA0	BA1	V or RIR	V or H	H	CID0	CID1	CID2	4, 20, 23, 24

Following a DRFM command to the DRAM, any host-requested row address samples to banks that received the DRFM command will be cleared from further use.

RESET will clear DRFM sampled addresses. Any DRFM sampled addresses will be retained during Self Refresh, Power Down, MPSM modes, etc., requiring the host to resample prior to issuing a DRFM
command if the address retained in a bank is no longer relevant. Additionally, no RAA credit is given to banks with DRFM sampled addresses, regardless of relevancy.

Disabling DRFM (MRW to set MR59:OP[0]=0B) may result in a DRFM sampled address being cleared or overwirtten by the DRAM.

DRFM command scheduling shall meet the same minimum separation requirements as those for the REF command (see Table 69 in the Refresh Operation section).

On average, any row/bank address combination is allowed to be sampled once per DRFM command interval, tDRFMi. tDRFMI is 2*tREFI1, resulting in no more than 4,096 DRFM commands to the same row/bank address combination within tREF.

4.42.2.1 Bounded Refresh Configuration and tDRFM

The DRFM command refreshes physically adjacent neighboring rows to the DRFM sampled address, up to the distance specified by the Bounded Refresh Configuration (BRC) as defined by MR59:OP[2:1]. The DRAM is responsible for applying a refresh ratio to the outermost rows being refreshed to protect the DRAM from excessive refreshes on rows adjacent to the outermost rows.

For example, BRC2 will always refresh the +/-1 physically adjacent neighboring rows, and the +/-2 physically adjacent neighboring rows may be refreshed at a reduced rate as determine by the DRAM. Likewise if BRC4 is programmed, the DRAM will always refresh the +/-1, +/-2 and +/- 3 physically adjacent neighboring rows, while applying a ratio to +/-4 physically adjacent neighboring rows.

The corresponding DRFM command duration (tDRFM) is directly related to the time required to refresh the rows. Due to a single row being refreshed on multiple banks corresponding to the DRFMab or DRFMsb command being issued, the per row refresh duration is tRRF, as shown in Table 177.

Table 177 — tRRF by Device Density

Parameters	Symbol	8 Gb	16 Gb	24 Gb	32 Gb	Units	Notes
All bank per row refresh duration	tRRFab(min)	70	70	70	70	ns	
Same bank per row refresh duration	tRRFsb(min)	60	60	60	60	ns	

4.42.2.1 Bounded Refresh Configuration and tDRFM (cont'd)

The equation for tDRFM is (2*tRRF)*BRC. tDRFM is dependent on the DRFMab or DRFMsb command being issued. Table 178 shows the allowable BRC options and corresponding tDRFM durations:

Table 178 — tDRFM and Blast Radius Configuration (BRC)

MR59:OP[2:1]	Rows Refreshed	tDRFMab	tDRFMsb
BRC 2	Always +/-1, Ratio +/-2	280 ns	240 ns
BRC 3	Always +/-1, +/-2, Ratio +/-3	420 ns	360 ns
BRC 4	Always +/-1, +/-2, +/-3, Ratio +/-4	560 ns	480 ns
RFU	RFU	RFU	RFU

4.42.2.2 BRC Support Level

The BRC support level indicates how many BRC options the DRAM can support, which is set by the DRAM vendor in the read only MR59:OP[3]. A DRAM with MR59:OP[3]=0 will support all BRC options (BRC2, 3, 4). A DRAM with MR59:OP[3]=1 only supports BRC2. If the DRAM only supports BRC2, MR59:OP[3]=1, then the default support is BRC2 regardless of BRC setting in MR59:OP[2:1]. BRC2 only support is transitional option for earlier support with limited DRFM. DRAM vendors shall support all BRC options (BRC2, 3, 4) with future DRAM designs.

4.43 Package Output Driver Test Mode (Optional)

This optional mode allows for characterization of the DRAM package by allowing the host to individually turn on the output driver of a single bit of the DRAM, while all other bits remain terminated. To use this test mode, the host sets MR61:OP[4:0] to select the target DM or DQ Output Driver. The host also sets the target driver to use the Pull-up Output Driver Impedance of 34 ohms (MR5:OP[2:1] = 00_B), while the termination for all the other DMs and DQs in the DRAM are defined by MR34:[2:0] (RTT_PARK). Note that the supportability of DM termination is decided by MR5:OP[5]. However, when DM is selected as the target driver, DRAM should set DM impedance according to MR5:OP[2:1] regardless of MR5:OP[5].

This is only a test mode, no normal functionality is assumed while in this mode or after enabling this mode without a reset to the DRAM device. Entering into this mode is done by programming any value in MR61 other than 0. Since this is an optional function, the discovery bit is located in MR5:OP[3]. A reset of the DDR5 SDRAM is required after exiting the package output driver test mode.

Even though only 5 bits of the MR are needed, the entire MR61 is blocked out to isolate it from normal operating modes.

MR5 Register - for Reference only - See Mode Register Section for Details

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Pull-Down Output Driver Impedance		DM Enable	TDQS Enable	PODTM Support	Pull-up Output Driver Impedance		Data Output Disable

MR61 Register - for Reference only - See Mode Register Section for Details

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RSVD			Package Output Driver Test Mode				

4.44 CS Geardown Mode

DDR5 geardown mode for CS enables CS operation to 2N mode at conditions where 1N mode is not viable due to the system configuration and speed of operation. Geardown is enabled with an MPC command during power up. Upon exit from Self Refresh with Frequency Change, geardown mode is enabled or disabled based on the setting of MR13:OP[4].

Geardown mode is supported only on DRAMs that support max data rates of 7200 and faster, but these DRAMs support Geardown mode at all supported operating frequencies. The DRAM shall be capable of operating at 7200 and above with geardown mode disabled also. The commands shall not be issued at odd gap clocks from where clock sync occurred for proper functioning.

It is required that the system complete CSTM and CATM after any power on initialization.

Geardown INIT sequence:

1. PowerUp Initialization
2. CSTM (1N CS Pulse).
3. MPC (CS Geardown enable)
4. Sync Pulse(2N)
   a. Only DSEL commands are allowed during tSYNC_GEAR (between MPC and sync pulse)
   b. 2N sync pulse is 2 clocks wide. The falling edge of the pulse must meet 1N setup and hold timings. It must meet the hold time from the previous rising edge of the clock where it is sampled high, and meet the setup time of the next rising edge of the clock where it is sampled low.
5. CATM (in Geardown mode)

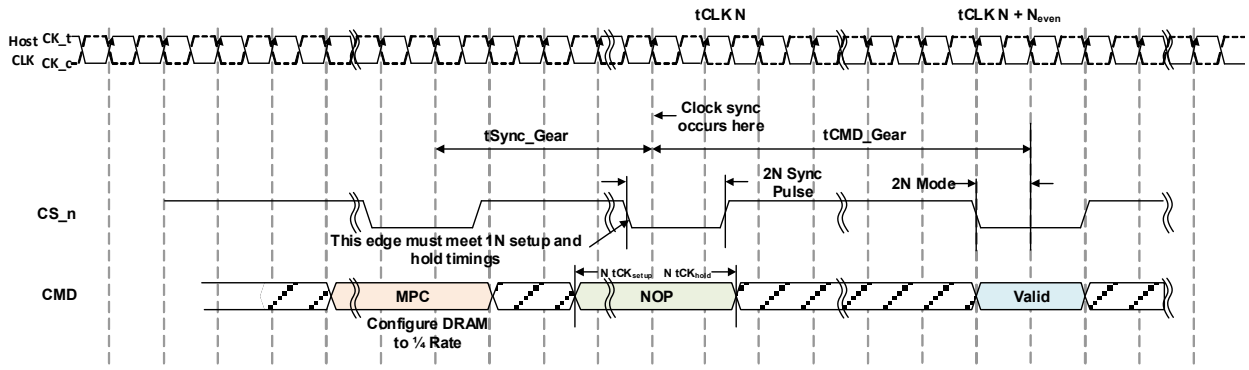
Note that in Geardown mode, the exit from CATM is achieved with two consecutive Geardown NOPs (CS sampled active on two consecutive Even numbered clocks).

For the CS geardown MPC, the following OP code in Table 179 should be applied.

Table 179 — MPC Function Definition for OP[7:0]

Functions	Operand	Data	Notes
Initialization and Training Modes	OP[7:0]	10010001: CS Geardown Enable	

The MPC command will not affect MR13:OP[4]. The host controller is expected to set this MR if geardown is to be used following self refresh.



NOTES:
1. During initialization, CSTM shall be run before entering Geardown Mode.
2. CSTM must be run in 1N mode in order to meet the 1N setup and hold window for the CS Geardown Sync, which is sent when the bus is quiet. Once in CS Geardown mode the CS is sampled only on even numbered clocks which provides the additional setup and hold times required for normal operation when other signals are toggling.
3. For the sync pulse, only the first falling edge of CS is used by the DRAM to determine the clock phase. The rising edge of the CS is not used for synchronization, and has no timing constraints.
4. The NOP encoding on the CA bus may be longer than the CS pulse used for synchronization

Figure 187 — Geardown during Initializations

4.44 CS Geardown Mode (cont'd)

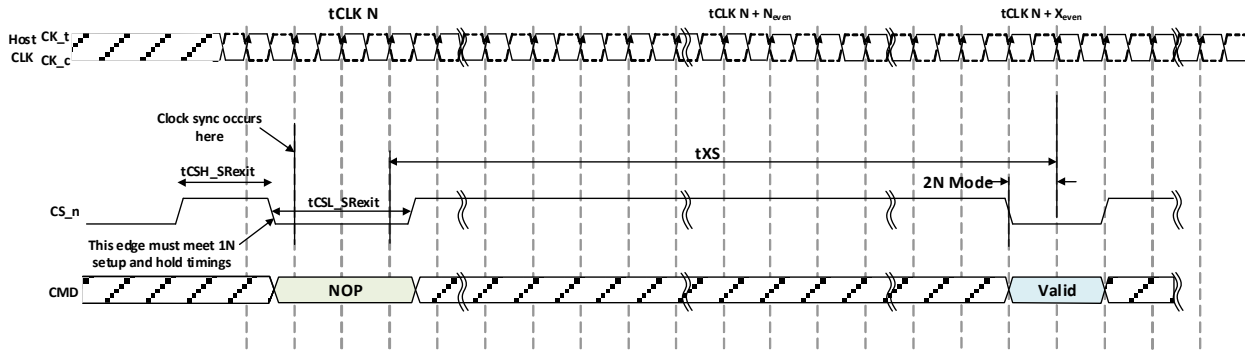
Table 180 — CS Geardown Parameters

Symbol	Value	Notes
*t*Sync_Gear	max (14ns, 16nCK)	
*t*CMD_Gear	max (14ns, 16nCK)	

On self refresh exit, the geardown clock phase must be re-established. Geardown may also be switched on or off upon self refresh exit due to a frequency change. MR13:OP[4] determines whether the DRAM will enable geardown mode or not upon the next exit of self refresh with frequency change. If switching between geardown on and off modes the host controller must write MR13:OP[4] to the appropriate value any time prior to the self refresh entry with frequency change command. The required MR13:OP[4] change is defined in Clause 3.5.15. Note that a SRE command (without frequency change) will remain in the previous mode and will NOT change based on a change in MR13:OP[4].

When Geardown is enabled, during a Self Refresh Exit the DRAM will sample the proper clock edge during the tCSL_SRexit. After tXS the host can then drive CS at 2N.

Geardown must be used only with the CA bus in 2N mode. It is the host controller's responsibility to have the CA bus in 2N mode with an explicit MPC command when operating in geardown mode before any 2-cycle commands are sent.



NOTES:
1. For the sync pulse, only the first falling edge of CS is used by the DRAM to determine the clock phase. The rising edge of the CS is not used for synchronization, and has no timing constraints.
2. The CS shall remain static low during tCSL_SRexit.
3. The NOP encoding on the CA bus may be longer than the CS pulse used for synchronization.

Figure 188 — Geardown Enabled during SRX

4.45 IO Features and Modes

4.45.1 Data Output Disable

The device outputs may be disabled by the Data Output Disable mode register, MR5:OP[0], as shown in the MR5 Register Definition table. For normal operation, set MR5:OP[0] = 0 (default). Setting MR5:OP[0] = 1 disables the device outputs. Disabling the data outputs also disables on-die termination (ODT) for those pins. Write and non-target (NT) commands to a devices with the data outputs disabled may not function correctly.

4.45.2 TDQS/DM

The DDR5 SDRAM x8 configuration has a package ball that is shared between TDQS_t and DM_n. The Write Data Mask (DM) function is dependent upon Termination Data Strobe (TDQS). If TDQS is enabled, DM is disabled. If TDQS is disabled, then DM may be enabled or disabled via mode register setting, as noted in Table 181.

4.45.2.1 TDQS

One pair of Termination Data Strobe (TDQS) pins, TDQS_t/TDQS_c, is supported for the x8 configuration DDR5 SDRAM. The TDQS function is programmable via Mode Register bit, MR5:OP[4]. The x8 is the only configuration which supports the TDQS function. The x4 and x16 DDR5 SDRAMs do not support this function thus, for these configurations, the TDQS MR setting must be disabled, MR5:OP[4] = 0 (default).

When TDQS is enabled, MR5:OP[4] = 1, the same termination resistance function is applied to the TDQS_t/TDQS_c pins that is applied to DQS_t/DQS_c pins., except during Read commands where TDQS does not output any data and will remain at RTT_DQS_PARK.

4.45.2.2 DM

(Reference section “4.8.1 Write Data Mask” for data mask functionality.)

4.45.2.3 TDQS/DM Disable

When the TDQS is disabled, MR5:OP[4] = 0, the MR5:OP[5] bit may be used to enable or disable the DM_n pin function.

When both TDQS and DM functions are disabled, termination will be turned off and the pins will drive Hi-Z. The DM_n pin input receiver will be turned-off and does not expect any valid logic level.

Table 181 — x8 TDQS Function Matrix

TDQS (MR5:OP[4])	DM
0_B: Disabled (default)	MR5:OP[5]
1_B: Enabled	Disabled

5 On-Die Termination

5.1 On-Die Termination for DQ, DQS, DM, and TDQS

On-Die Termination (ODT) is a feature of the DDR5 SDRAM that allows the DRAM to change termination resistance for each DQ, DQS, DM and TDQS pin. Unlike previous DDR technologies, DDR5 no longer has a physical ODT pin and all ODT based control is now command & mode register based. For x4 and x8 configuration devices, ODT is applied to each DQ, DQS_t, DQS_c and DM_n, as well as TDQS_t, TDQS_c for the x8 configuration. For x16 configuration devices, ODT is applied to each DQU, DQL, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n and DML_n. ODT is enabled via non-target Read/Mode Register Read commands, Write and non-target Write commands, or is set to the default “PARK” value through settings in MR33-MR35.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently change termination resistance for any or all DRAM devices. In addition to the control capability of the DQ ODT, the DQS ODT will now be independently programmed via MR33:OP[5:3] and held static. All ODT control will be targeted for the DQs. This addition allows for adjusting the delay common in an unmatched architecture. DQS RTT offset control mode is enabled via MR40:OP[2:0].

The ODT feature is turned off and not supported in Self-Refresh mode, but does have an optional mode when in Power Down. A simple functional representation of the DRAM ODT feature is shown in Figure 189.

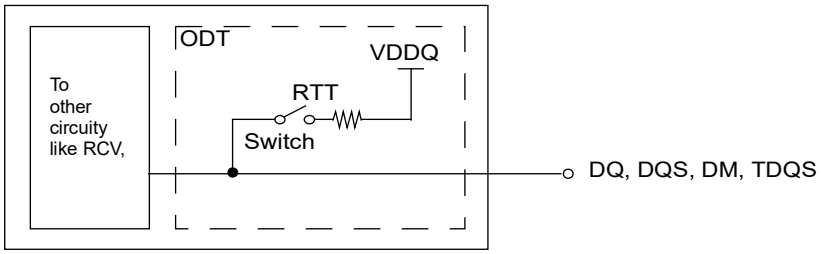


Figure 189 — Functional Representation of ODT

The switch is enabled by the internal ODT control logic, which uses command decode, Mode Register Settings and other control information, see below. The value of RTT is determined by the settings of Mode Register bits.

5.2 ODT Modes, Timing Diagrams, and State Table

The ODT Mode of DDR5 SDRAM has five states: Data/Strobe Termination Disable, RTT_WR, RTT_NOM_RD, RTT_NOM_WR and RTT_PARK/DQS_RTT_PARK. The ODT Mode is enabled based on Mode Registers for each RTT listed below. In this case, the value of RTT is determined by the settings of these mode register bits.

After entering Self-Refresh mode, DRAM automatically disables ODT termination and sets Hi-Z as termination state regardless of these settings.

Application: Controller can control each RTT condition with Write (WR), Read (RD) or Mode Register Read (MRR) commands and use of ODT Offset Control Mode Registers.

- **Data Termination Disable:** DRAM driving data upon receiving Read command disables the termination after CL-1 and re-enables the termination at CL + BL/2 (CL and BL defined in clock cycles).
- **Strobe Termination Disable:** DRAM driving strobe upon receiving Read command disables the termination after CL-1-tRPRE-(Read_DQS_Offset) and re-enables the termination at CL+BL/2-0.5+tRPST-(Read_DQS_Offset) (CL and BL defined in clock cycles).
- **RTT_WR:** The rank that is being written to provide termination and adjusts timing based on ODT Control Mode Register settings.
- **RTT_NOM_RD:** DRAM turns ON RTT_NOM_RD if it sees CS asserted during the second pulse of the Read command (except when ODT is disabled by MR35:OP[5:3]).
- **RTT_NOM_WR:** DRAM turns ON RTT_NOM_WR if it sees a CS asserted during the second pulse of the Write command (except when ODT is disabled by MR35:OP[2:0])
- **RTT_PARK:** Default parked value set via MR34:OP[2:0] and is to be enabled when a Read or Write is not active.
- **DQS_RTT_PARK:** Default parked value set for DQS via MR33:OP[5:3] and is to be enabled when a Read is not active

5.2 ODT Modes, Timing Diagrams, and State Table (cont'd)

Those RTT values have priority as follows:

1. Data Termination Disable and Strobe Termination Disable
2. RTT_WR
3. RTT_NOM_RD
4. RTT_NOM_WR
5. RTT_PARK and DQS_RTT_PARK

This means if there is a Write command, then the DRAM turns on RTT_WR, not RTT_NOM_RD or RTT_NOM_WR, and also if there is a Read command, then the DRAM disables data termination and goes into driving mode.

If during the second cycle of a Write, Read or Mode Register Read command, a CS enable is sent, then Non-Target ODT is enabled and the appropriate RTT_NOM_WR or RTT_NOM_RD is enabled for the non-target rank. This provides additional and potentially different termination options for the other ranks on the channel.

Table 182 — Termination State Table

Command	Mode Register Configuration Settings				Results		Note
	RTT_PARK	RTT_WR	RTT_NOM_WR	RTT_NOM_RD	Target DRAM Term	Non-Target DRAM Term	
ANY	Disabled				HI-Z (ODT OFF)		3
Any Non-Term CMD	Enabled	Don't Care			RTT_PARK	RTT_PARK	4
WR	Disabled			Don't Care	HI-Z (ODT OFF)	HI-Z (ODT OFF)	
	Disabled		Enabled		HI-Z (ODT OFF)	RTT_NOM_WR	
	Disabled	Enabled	Disabled		RTT_WR	HI-Z (ODT OFF)	
	Don't Care	Enabled			RTT_WR	RTT_NOM_WR	2
	Enabled		Disabled		RTT_WR	HI-Z (ODT OFF)	2, 5
	Enabled	Disabled	Enabled		RTT_PARK	RTT_NOM_WR	
	Enabled	Disabled			RTT_PARK	HI-Z (ODT OFF)	5
RD/MRR	Enabled	Don't Care		Disabled	HI-Z (ODT OFF)	HI-Z (ODT OFF)	1, 5
	Don't Care			Enabled	HI-Z (ODT OFF)	RTT_NOM_RD	1

NOTE 1 When a Read command is executed, the DRAM termination state of the target rank will be Hi-Z for a defined period independent of MR setting of RTT_PARK/RTT_NOM_RD/RTT_NOM_WR.

NOTE 2 If RTT_WR is enabled, RTT_WR will be activated by a Write command for a defined period of time independent of the MR setting of RTT_PARK /RTT_NOM.

NOTE 3 If all RTT configurations are disabled, ODT receiver power will be turned off to save power.

NOTE 4 If RTT_PARK is enabled, DRAM RTT_PARK termination will be enabled while WR/RD/MRR are not being executed.

NOTE 5 When a Non-Target ODT command is executed and the RTT_NOM_WR or RTT_NOM_RD is disabled, the DRAM termination state of the non-target rank will be Hi-Z for a defined period, independent of the MR setting of RTT_PARK.

5.2 ODT Modes, Timing Diagrams, and State Table (cont'd)

On-Die Termination effective resistance RTT is defined by MR bits. ODT is applied to the DQ, DQS_t/DQS_c, DM and TDQS_t/TDQS_c (x8 devices only) pins. A functional representation of the on-die termination is shown in Figure 190.

$$RTT = \frac{VDDQ - Vout}{|\ I\ out\ |}$$

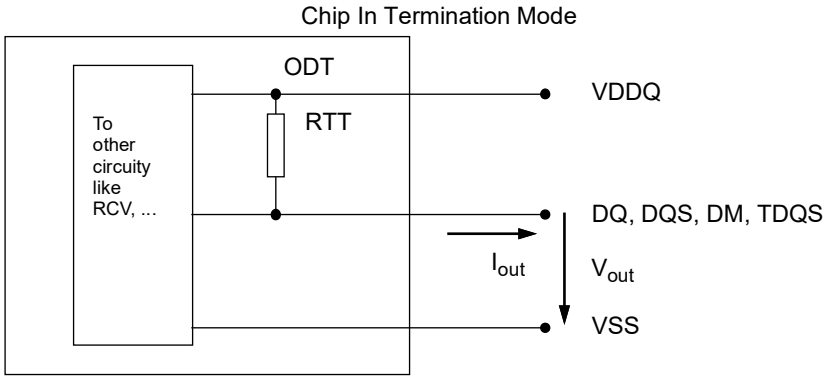


Figure 190 — On Die Termination

On-Die Termination effective RTT values supported are 240,120, 80, 60, 48, 40, and 34 ohms.

Table 183 — ODT Electrical Characteristics RZQ=240 Ω +/-1%
Entire Temperature Operation Range; after Proper ZQ Calibration

RTT	Vout	Min	Nom	Max	Unit	Notes
240 Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ	1, 2, 3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ	1, 2, 3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ	1, 2, 3
120 Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/2	1, 2, 3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/2	1, 2, 3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/2	1, 2, 3
80 Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/3	1, 2, 3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/3	1, 2, 3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/3	1, 2, 3
60 Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/4	1, 2, 3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/4	1, 2, 3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/4	1, 2, 3
48 Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1, 2, 3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1, 2, 3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/5	1, 2, 3
40 Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/6	1, 2, 3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/6	1, 2, 3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/6	1, 2, 3
34 Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1, 2, 3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1, 2, 3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/7	1, 2, 3
DQ-DQ Mismatch within byte	VOMdc = 0.8* VDDQ	0	-	8	%	1, 2, 4, 5, 6

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see "ZQ Calibration Commands" section.

NOTE 2 Pull-up ODT resistors are recommended to be calibrated at 0.8*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5*VDDQ and 0.95*VDDQ.

NOTE 3 The tolerance limits are specified under the condition that VDDQ=VDD.

NOTE 4 DQ to DQ mismatch within byte variation for a given component including DQS_T and DQS_C (characterized)

NOTE 5 RTT variance range ratio to RTT Nominal value in a given component, including DQS_t and DQS_c.

$$\text{DQ-DQ Mismatch in a Device} = \frac{RTTMax - RTTMin}{RTTNOM} * 100$$

NOTE 6 This parameter of x16 device is specified for Upper byte and Lower byte.

5.3 Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR5 SDRAM can be changed without issuing an MRW command. This requirement is supported by the “Dynamic ODT” feature as described as follows:

5.3.1 ODT Functional Description

The function is described as follows:

- Five RTT values are available: RTT_NOM_RD, RTT_NOM_WR, RTT_PARK, RTT_WR and DQS_RTT_PARK.
  - The value for RTT_NOM_RD is preselected via MR35:OP[5:3]
  - The value for RTT_NOM_WR is preselected via MR35:OP[2:0]
  - The value for RTT_WR is preselected via MR34:OP[5:3]
  - The value for RTT_PARK is preselected via MR34:OP[2:0] - Programmed via MPC
  - The value for DQS_RTT_PARK is preselected via MR33:OP[5:3] - Programmed via MPC

- During operation without commands, the termination is controlled as follows;
  - Nominal termination strength for all types (RTT_NOM_RD, RTT_NOM_WR, RTT_WR, RTT_PARK & DQS_RTT_PARK) are selected.
  - RTT_NOM_RD and RTT_NOM_WR on/off timings are controlled via the respective non-target Read/Mode Register Read and Write commands and latencies.
  - DQS_RTT_PARK is held static and is based on the value programmed in the MR listed above.

- When a Write command (WR) is registered, the termination is controlled as follows:
  - A latency ODTLon_WR after the Write command, termination strength RTT_WR is selected.
  - A latency ODTLoff_WR after the Write command, termination strength RTT_WR is de-selected.

- The termination, RTT_NOM_WR, for the non-target Write command is selected and de-selected by latencies ODTLon_WR_NT and ODTLoff_WR_NT, respectively.
- When a Read command (RD) is registered, the termination is controlled as follows:
  - A latency ODTLoff_RD after the Read command, data termination is disabled. Then, ODTLon_RD after the Read command, data termination is enabled.
  - A latency ODTLoff_RD_DQS after the Read command, strobe termination is disabled. ODTLon_RD_DQS after the Read command, strobe termination is enabled.

- The termination, RTT_NOM_RD, for the non-target Read command is selected and de-selected by latencies ODTLon_RD_NT and ODTLoff_RD_NT, respectively.

The duration of a Write or Read command is a full burst cycle, BL/2. The termination select ("ODTLon_...") and de-select ("ODTLoff_...") latency settings shall not result in an ODT pulse width which violates a burst cycle (BL/2) minimum duration. The equation "ODTLoff_*X* - ODTLon_*X* >= BL/2” must be met, where *X* is the termination latency setting associated with a particular command type (WR, WR_NT, RD_NT).

To achieve the minimum write burst duration, ODTLoff_*X* and ODTLon_*X* latencies contain independent programmable mode register offsets:

- The values for the Write command ODT control offsets are preselected via MR37.
  MR37:OP[2:0] preselects ODTLon_WR_Offset
  MR37:OP[5:3] preselects ODTLoff_WR_Offset
- The values for the non-target Write command ODT control offsets are preselected via MR38.
  MR38:OP[2:0] preselects ODTLon_WR_NT_Offset
  MR38:OP[5:3] preselects ODTLoff_WR_NT_Offset
- The values for the non-target Read command ODT control offsets are preselected via MR39.
  MR39:OP[2:0] preselects ODTLon_RD_NT_Offset
  MR39:OP[5:3] preselects ODTLoff_RD_NT_Offset

5.3.1 ODT Functional Description (cont'd)

Table 184 — Allowable Write ODTL Offset Combinations

		ODTLon_WR_OffsetSetting						
		-4	-3	-2	-1	0	1	2
ODTLoff_WR_Offset Setting	4	Valid	Valid	Valid	Valid	Valid	Valid	Valid
	3	Valid	Valid	Valid	Valid	Valid	Valid	Valid
	2	Valid	Valid	Valid	Valid	Valid	Valid	Valid
	1	Valid	Valid	Valid	Valid	Valid	Valid	Invalid
	0	Valid	Valid	Valid	Valid	Valid	Invalid	Invalid
	-1	Valid	Valid	Valid	Valid	Invalid	Invalid	Invalid
	-2	Valid	Valid	Valid	Invalid	Invalid	Invalid	Invalid
NOTE 1 The Write ODTLon -4 offset and ODTLoff +4 offset is not allowed for 1980-2100 data rates.								

Table 185 — Allowable Write NT ODTL Offset Combinations

		ODTLon_WR_NT_Offset Setting						
		-4	-3	-2	-1	0	1	2
ODTL-off_WR_NT_Offset Setting	4	Valid	Valid	Valid	Valid	Valid	Valid	Valid
	3	Valid	Valid	Valid	Valid	Valid	Valid	Valid
	2	Valid	Valid	Valid	Valid	Valid	Valid	Valid
	1	Valid	Valid	Valid	Valid	Valid	Valid	Invalid
	0	Valid	Valid	Valid	Valid	Valid	Invalid	Invalid
	-1	Valid	Valid	Valid	Valid	Invalid	Invalid	Invalid
	-2	Valid	Valid	Valid	Invalid	Invalid	Invalid	Invalid
NOTE 1 The Write NT ODTLon -4 offset and ODTLoff +4 offset is not allowed for 1980-2100 data rates.								

Table 186 — Allowable Read NT ODTL Offset Combinations

		ODTLon_RD_NT_OffsetSetting				
		-3	-2	-1	0	1
ODTLoff_RD_NT_Offset Setting	3	Valid	Valid	Valid	Valid	Valid
	2	Valid	Valid	Valid	Valid	Valid
	1	Valid	Valid	Valid	Valid	Valid
	0	Valid	Valid	Valid	Valid	Invalid
	-1	Valid	Valid	Valid	Invalid	Invalid

5.3.1 ODT Functional Description (cont'd)

See Table 187 for ODT latency and timing parameter details.

Table 187 — Latencies and Timing Parameters Relevant for Dynamic ODT and CRC Disabled

Name and Description	Abbre-viation	Defined from	Define to	DDR5 Speed Bins 3200 to 9200	Unit	Note
ODT Latency On from Write command to RTT Enable	tODTLon_WR	Registering external Write command	Change RTT strength from Previous State to RTT_WR	tODTLon_WR = CWL+ODTLon_WR_offset	nCK	1
ODT Latency On from NT Write command to RTT Enable	tODT-Lon_WR_NT	Registering external Write command	Change RTT strength from Previous State to RTT_NOM_WR	tODTLon_WR_NT = CWL+ODT-Lon_WR_NT_offset		1
ODT Latency Off from Write command to RTT Disable	tODTLoff_WR	Registering external Write command	Change RTT strength from RTT_WR to RTT_PARK/RTT_NOM_RD/RTT_NOM_WR/ Hi-Z	tODTLoff_WR = CWL+BL/2+ ODTLoff_WR_offset	nCK	1
ODT Latency Off from NT Write command to RTT Disable	tODTL-off_WR_NT	Registering external Write command	Change RTT strength from RTT_NOM_WR to RTT_PARK/RTT_NOM_RD/RTT_WR/ Hi-Z	tODTLoff_WR_NT = CWL+BL/2+ ODTLoff_WR_NT_offset		1
Data Termination Disable	tODTLoff_RD	Registering external Read command	Disables the termination upon driving data	Data Termination Disable = CL-1		2
Data Termination Enable	tODTLon_RD	Registering external Read command	Re-enables the termination after driving data	Data Termination Enable = CL+BL/2		2
Strobe Termination Disable	tODTLoff _RD_DQS	Registering external Read command	Disables the termination upon driving strobe	Strobe Termination Disable = CL-1-tRPRE-(Read DQS Offset)		2
Strobe Termination Enable	tODTLon _RD_DQS	Registering external Read command	Re-enables the termination after driving strobe	Strobe Termination Enable = CL+BL/2-0.5+tRPST-(ReadDQS Offset)		2
ODT Latency On from NT Read command to RTT Enable	tODT-Lon_RD_NT	Registering external Read command	Change RTT strength from Previous State to RTT_NOM_RD	tODTLon_RD_NT = CL+ODTLon_RD_NT_offset	nCK	1
ODT Latency Off from NT Read command to RTT Disable	tODTL-off_RD_NT	Registering external Read command	Change RTT strength from RTT_NOM_RD to RTT_PARK/RTT_NOM_WR/RTT_WR/ HI-Z	tODTLoff_RD_NT = CL+BL/2+ ODTLoff_RD_NT_offset		1

NOTE 1 All "_offset" parameters refer to the ODT Configuration Mode Registers settings in MR37 to MR39.

NOTE 2 For simplicity, Read commands are assigned the same type of timing parameter; however, unlike others, it is a fixed timing and does not have an offset mode register to control it. To indicate this, it was named Data (or Strobe) Termination Disable and Enable.

5.3.1 ODT Functional Description (cont'd)

Table 188 — RTT Change Skew for Dynamic ODT and CRC Disabled for DDR5-3200 thru 6400

Name and Description	Abbr.	Defined from	Define to	DDR5-3200 thru 5600	DDR5-6000	DDR5-6400	Unit	Note
RTT change skew	tADC	Transitioning from one RTT State to the next RTT State	RTT Valid	tADC(min)=0.20 tADC(max)=0.80	tADC(min)=0.18 tADC(max)=0.82	tADC(min)=0.16 tADC(max)=0.84	tCK(avg)	1, 2

NOTE 1 When transitioning from a value of RTT equal to RA, to a value of RTT equal to RB, the RTT termination resistance during the transition must be constrained for the minimum of (RA,RB) to the maximum of (RA, RB).
NOTE 2 The tADC spec follows the operating frequency (so that faster speed bins are backwards compatible to slower speed bins).

Table 189 — RTT Change Skew for Dynamic ODT and CRC Disabled for DDR5-6800 thru 7600

Name and Description	Abbr.	Defined from	Define to	DDR5-6800	DDR5-7200	DDR5-7600	Unit	Note
RTT change skew	tADC	Transitioning from one RTT State to the next RTT State	RTT Valid	tADC(min)=0.14 tADC(max)=0.86	tADC(min)=0.12 tADC(max)=0.88	tADC(min)=0.10 tADC(max)=0.90	tCK(avg)	1, 2

NOTE 1 When transitioning from a value of RTT equal to RA, to a value of RTT equal to RB, the RTT termination resistance during the transition must be constrained for the minimum of (RA,RB) to the maximum of (RA, RB).
NOTE 2 The tADC spec follows the operating frequency (so that faster speed bins are backwards compatible to slower speed bins)

Table 190 — RTT Change Skew for Dynamic ODT and CRC Disabled for DDR5-8000 thru 9200

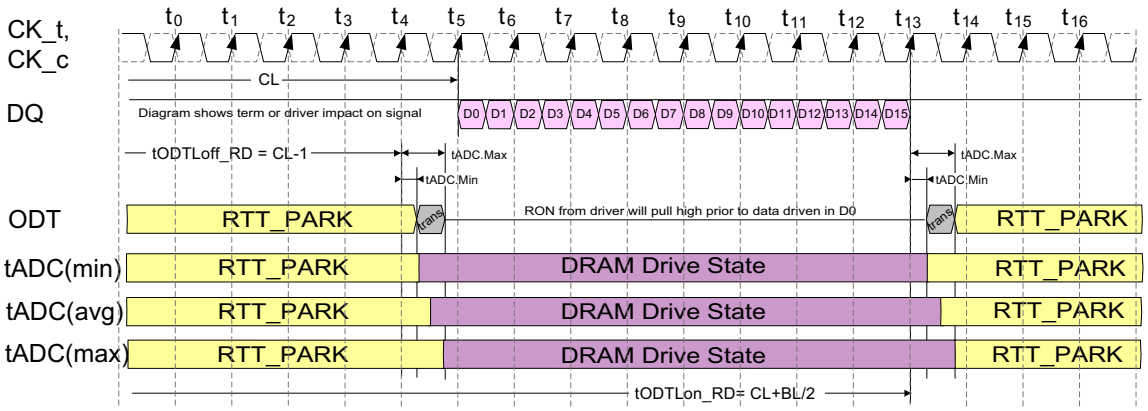
Name and Description	Abbr.	Defined from	Define to	DDR5-8000	DDR5-8400	DDR5-8800	DDR5-9200	Unit	Note
RTT change skew	tADC	Transitioning from one RTT State to the next RTT State	RTT Valid	tADC(min)=0.08 tADC(max)=0.92	tADC(min)=0.06 tADC(max)=0.94	tADC(min)=0.04 tADC(max)-0.96	tADC(min)=0.02 tADC(max)-0.98	tCK(avg)	1, 2

NOTE 1 When transitioning from a value of RTT equal to RA, to a value of RTT equal to RB, the RTT termination resistance during the transition must be constrained for the minimum of (RA,RB) to the maximum of (RA, RB).
NOTE 2 The tADC spec follows the operating frequency (so that faster speed bins are backwards compatible to slower speed bins)

5.3.2 ODT tADC Clarifications

tADC is defined as the time it takes for the DRAM to transition from one RTT state to the next RTT state, in case of the read, it is the time from the RTT state to the DRAM Drive state. Unless the RTT is specifically disabled, no High-Z state shall be allowed during tADC. During DRAM Drive state, the DRAM RON shall keep the DQ signal high prior to the first DQ transition. The DFE should assume that 4UI prior to D0 the signal is HIGH.

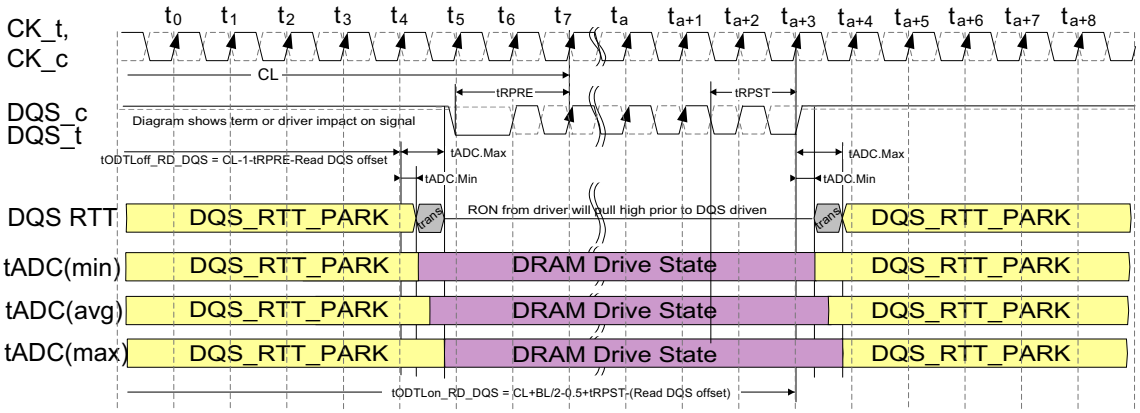
Figure 191 and Figure 192 are examples showing the tADC(min), tADC(avg) and tADC(max) with respect to the RTT status and effects on the DQ lines prior to the burst.



NOTES:
1. The follow diagram shows a transition from RTT_PARK to Read DRAM Drive state. When tADC transitions from RTT to Read Drive state, the DRAM RON from the driver will keep the DQ signal high prior to the data driven in D0. No High-Z time during tADC is allowed in this example.
2. In the case of Term to Write, the host will keep the DQ signal HIGH 4UI prior to the data driven in D0.
3. The DFE should assume that 4UI prior to D0 the signal is HIGH.

Figure 191 — tADC Clarification - Example 1 - DQ RTT Park to Read

Figure 192 is an example showing the tADC(min), tADC(avg) and tADC(max) with respect to the RTT status and effects on the DQS lines prior to the burst.



NOTES:
1. The follow diagram shows a transition from DQS_RTT_PARK to Read DRAM Drive state. When tADC transitions from RTT to Read Drive state, the DRAM RON from the driver will keep the DQS signal high prior to the DQS driven at t5. No High-Z time during tADC is allowed in this example.

Figure 192 — tADC Clarification - Example 2 - DQS RTT Park to Read

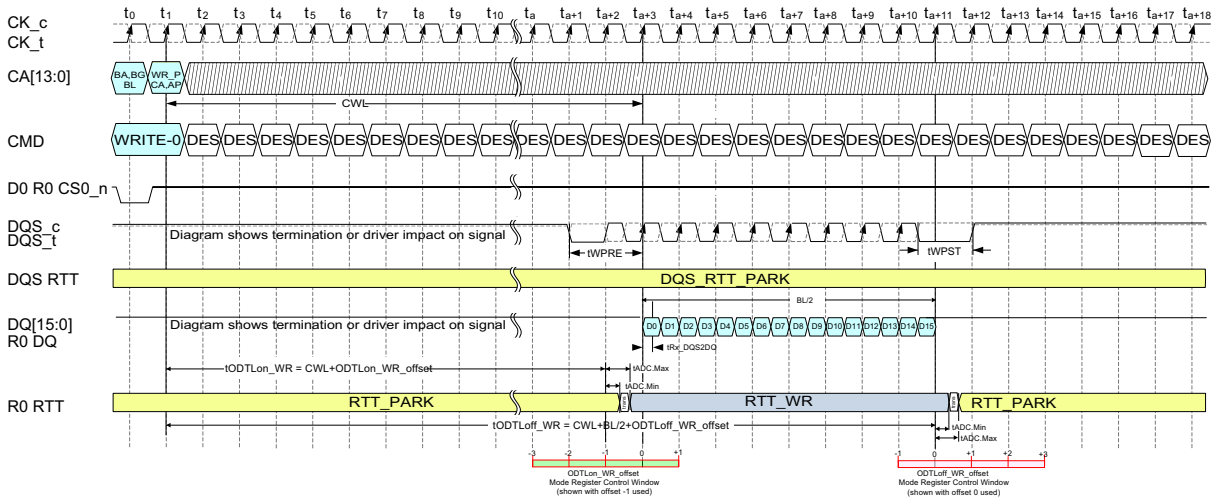
5.3.3 ODT Timing Diagrams

The following pages provide examples of ODT utilization timing diagrams. Examples of Write to Write, Read to Write and Read to Read are provided for clarification only. Implementations may vary, including termination on other DIMMS.

It is the controller's responsibility to manage command spacing and the programmable aspect of tODLon/off times to ensure that preambles and postambles are included in the RTT ON time.

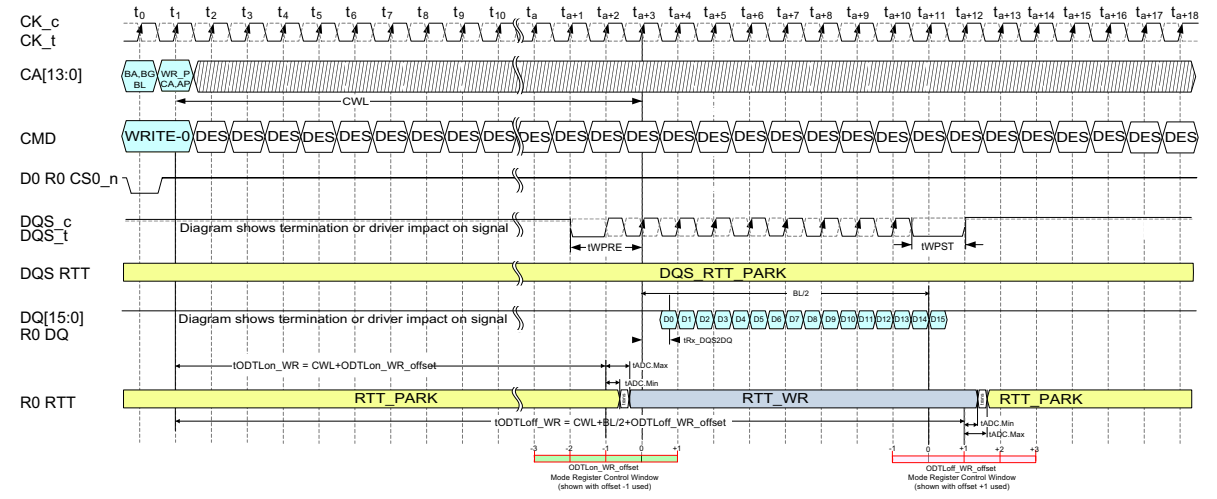
When there is a 1 tCK ODT control gap for any ODT operation (such as shown in Figure 199), the said gap's RTT value will be the same or smaller (stronger termination) than RTT_PARK.

All timings noted in the following figures are just used as reference.



NOTES:
1. The entire range of ODTL control is not shown for simplicity.
2. Example details - 2tCK tWPRE, 1.5tCK tWPST, 0.5UI tRX_DQS2DQ, ODTLon_WR_offset configured for -1, ODTLoff_WR_offset configured for 0. Example shows how the host may aggressively adjust the offset of the tODTLon_WR timing to give tADC the min time to settle before data.
3. System designs and margins may vary requiring larger RTT_WR windows.

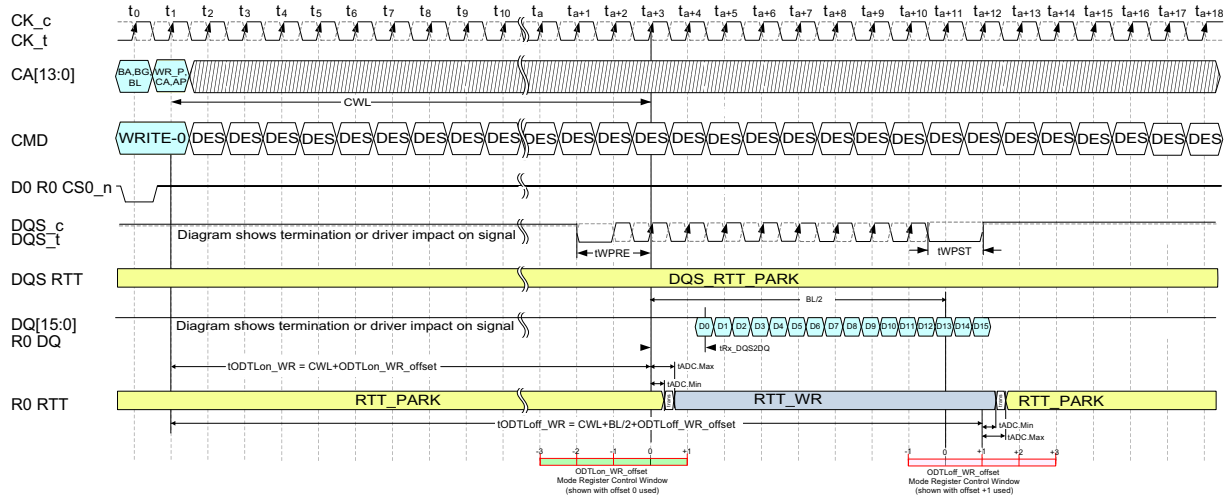
Figure 193 — Example 1 of Burst Write Operation ODT Latencies and Control Diagrams



NOTES:
1. The entire range of ODTL control is not shown for simplicity.
2. Example details - 2tCK tWPRE, 1.5tCK tWPST, 1.5UI tRX_DQS2DQ, ODTLon_WR_offset configured for -1, ODTLoff_WR_offset configured for +1. Example shows how host may want to add an offset to the tODTLoff_WR time so that RTT_WR stays on for the actual burst.
3. System designs and margins may vary requiring larger RTT_WR windows.

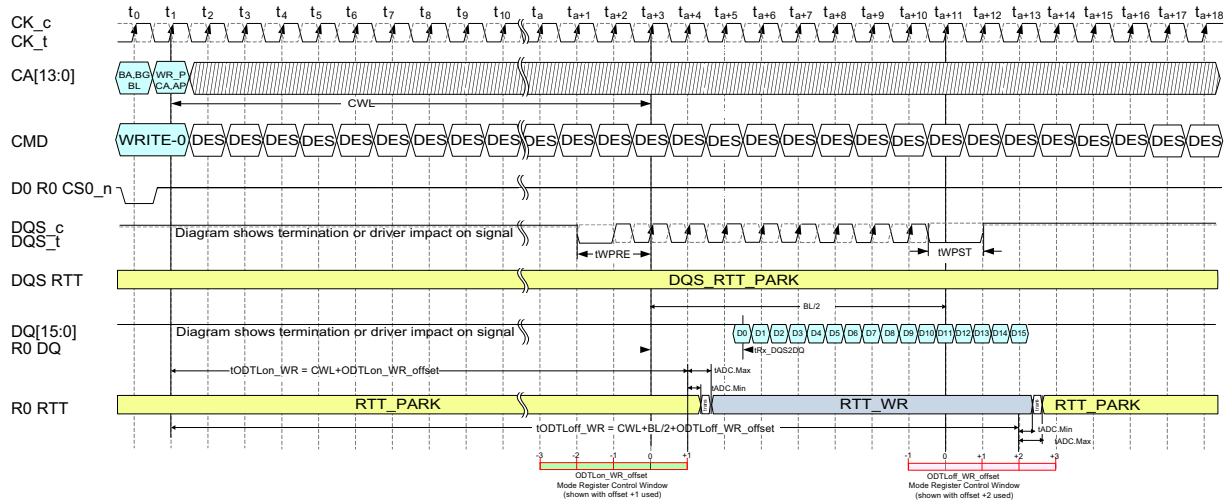
Figure 194 — Example 2 of Burst Write Operation ODT Latencies and Control Diagrams

5.3.3 ODT Timing Diagrams (cont'd)



NOTES:
1. The entire range of ODTL control is now shown for simplicity.
2. Example details - 2tCK tWPRE, 1.5tCK tWPST, 3UI tRX_DQS2DQ, ODTLon_WR_offset configured for 0, ODTLoff_WR_offset configured for +1. Example shows how host could leave the RTT_WR on time to default values with no offset and may want to add an offset to the tODTLoff_WR time so that RTT_WR stays on for the actual burst.
3. System designs & margins may vary requiring larger RTT_WR windows.

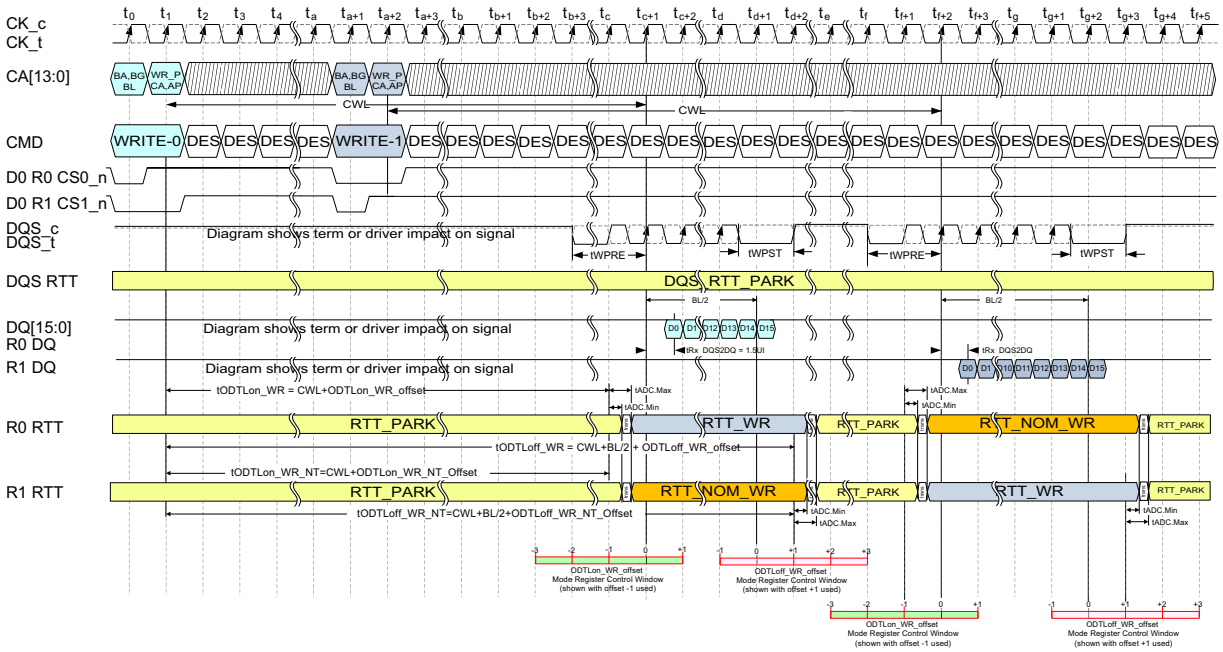
Figure 195 — Example 3 of Burst Write Operation ODT Latencies and Control Diagrams



NOTES:
1. The entire range of ODTL control is not shown for simplicity.
2. Example details - 2tCK tWPRE, 1.5tCK tWPST, 5UI tRX_DQS2DQ, ODTLon_WR_offset configured for +1, ODTLoff_WR_offset configured for +2. Example shows an extreme case where data is significantly delayed from DQS and how the host may want to add an offset to the tODTLon_WR time so that RTT_WR doesn't turn on too early and how the host may want to delay the tODTLoff_WR time so that it says on for the burst.
3. System designs & margins may vary requiring larger RTT_WR windows.

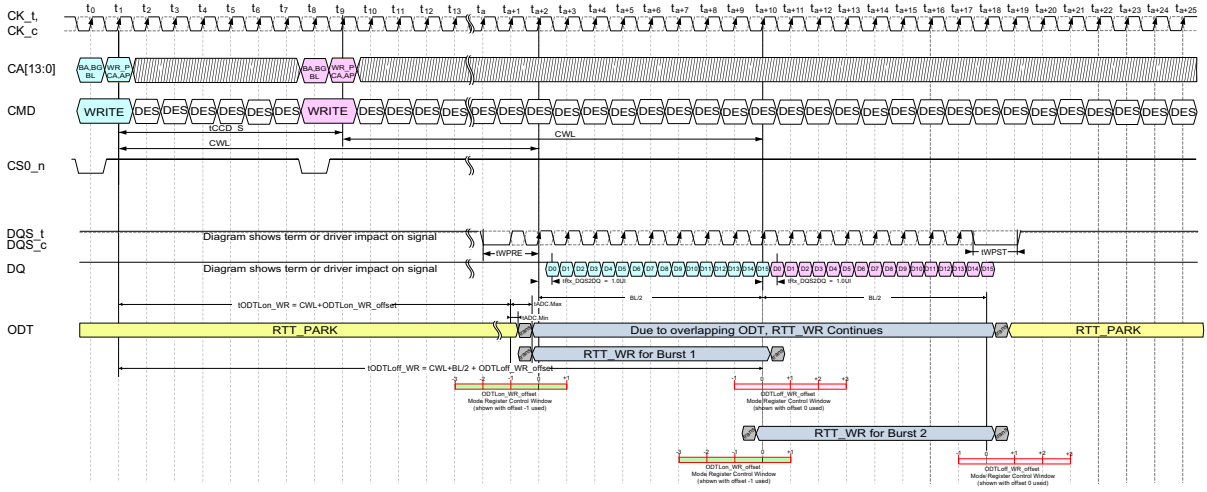
Figure 196 — Example 4 of Burst Write Operation ODT Latencies and Control Diagrams

5.3.3 ODT Timing Diagrams (cont'd)



NOTES:
1. ODTLon_WR, ODTLon_WR_NT, ODTLoff_WR and ODTLoff_WR_NT are based on Mode Register settings that can push out or pull in the RTT enable and disable time.
2. The entire range of ODTL control is not shown for simplicity.

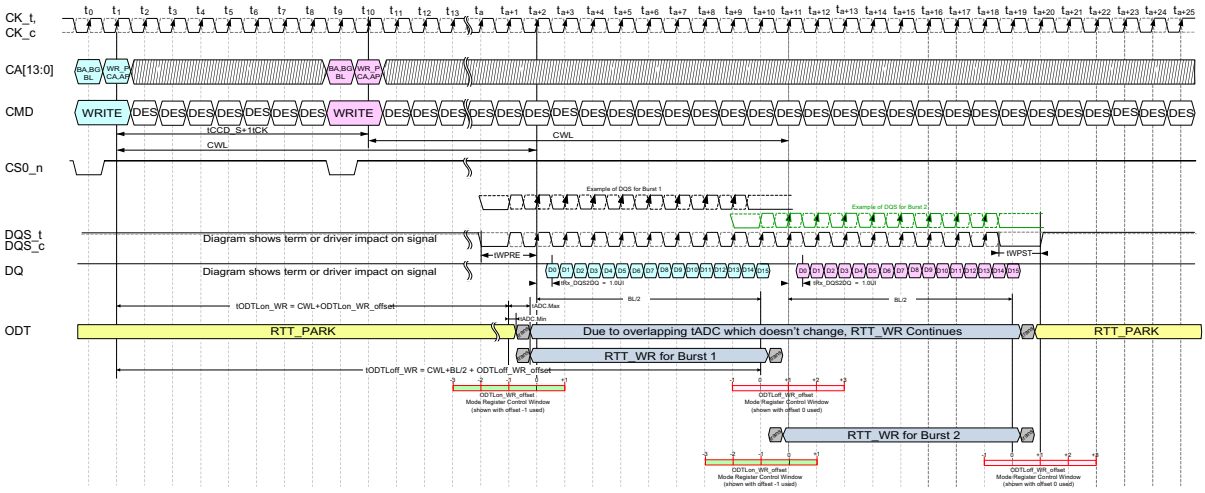
Figure 197 — Example of Write to Write Turn Around, Different Ranks



NOTES:
1. BL=16, Preamble=2tCK - 0010 pattern, Postamble=1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. Figure shown with ODTLon_WR_offset=-1, ODTLoff_WR_offset=0, tRX_DQS2DQ=1UI
4. In the case of Term to Write, the host will keep the DQ signal HIGH 4UI prior to the data driven in D0.
5. The DFE should assume that 4UI prior to D0 the signal is HIGH.

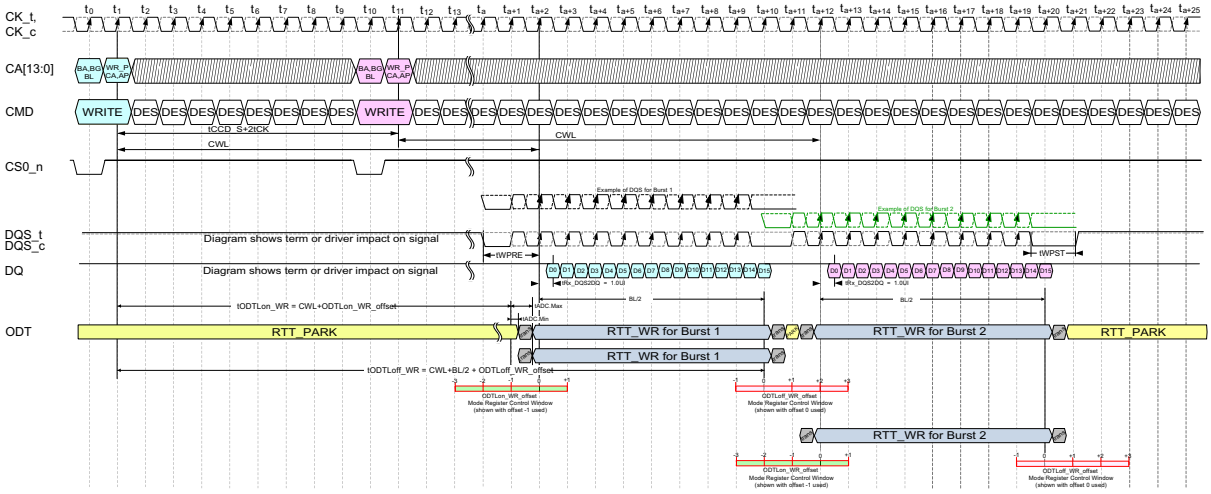
Figure 198 — WRITE (BL16) to WRITE (BL16), Different Bank, Seamless Bursts

5.3.3 ODT Timing Diagrams (cont'd)



NOTES:
1. BL=16, Preamble=2tCK - 0010 pattern, Postamble=1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. Figure shown with ODTLon_WR_offset=-1, ODTLoff_WR_offset=0, tRX_DQS2DQ=1UI
4. Red and Green DQS bursts are shown just for clarification purposes and are not part of an actual signal.
5. In the case of Term to Write, the host will keep the DQ signal HIGH 4UI prior to the data driven in D0.
6. The DFE should assume that 4UI prior to D0 the signal is HIGH.

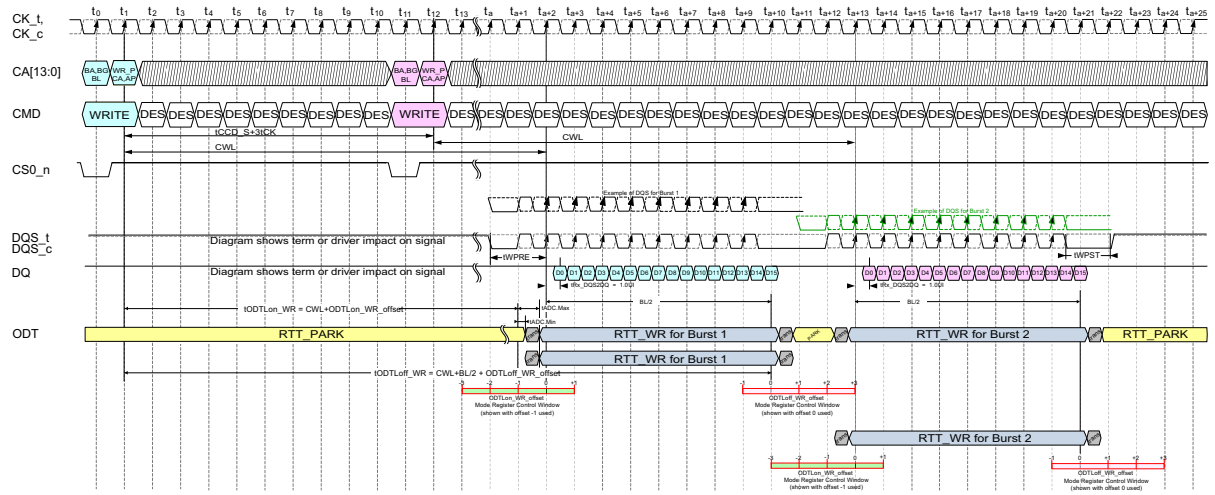
Figure 199 — WRITE (BL16) to WRITE (BL16), Different Bank, 1 tCK Gap



NOTES
1. BL=16, Preamble=2tCK - 0010 pattern, Postamble=1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. Figure shown with ODTLon_WR_offset=-1, ODTLoff_WR_offset=0, tRX_DQS2DQ=1UI
4. Red and Green DQS bursts are shown just for clarification purposes and are not part of an actual signal.
5. In the case of Term to Write, the host will keep the DQ signal HIGH 4UI prior to the data driven in D0.
6. The DFE should assume that 4UI prior to D0 the signal is HIGH.
7. When there is a 1 tCK ODT control gap for any ODT operation (such as shown in Figure 199), the said gap's RTT value will be the same or smaller (stronger termination) than RTT_PARK.

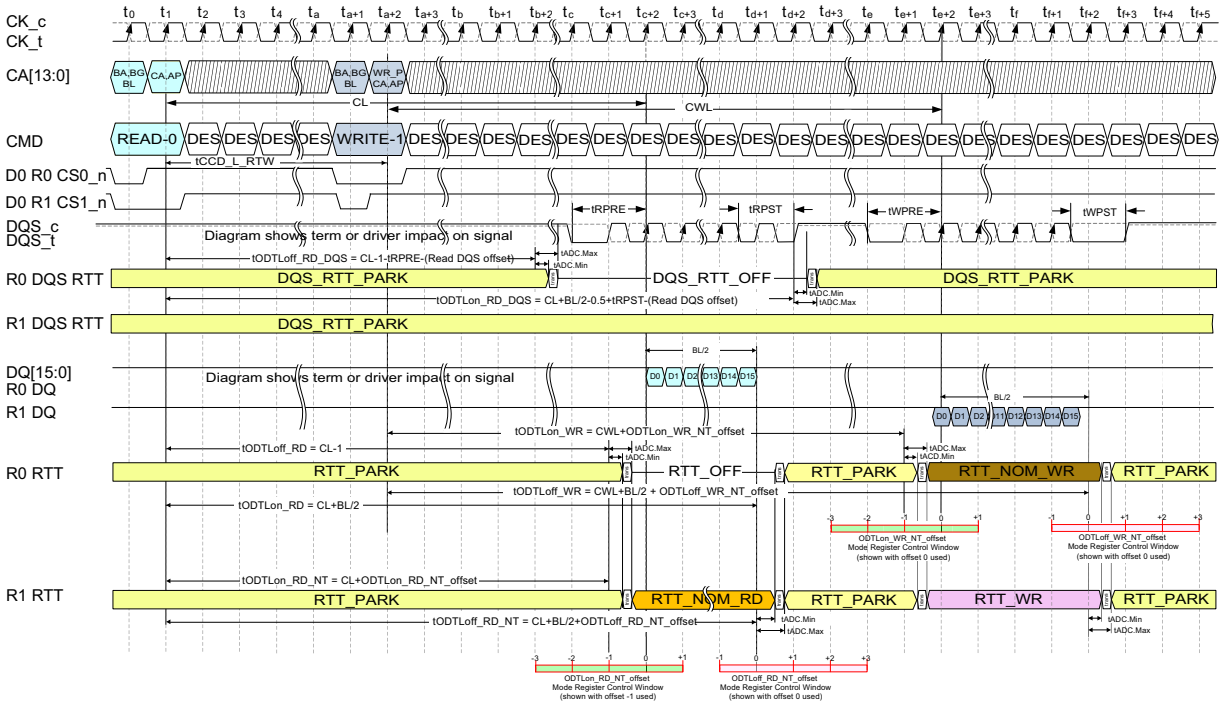
Figure 200 — WRITE (BL16) to WRITE (BL16), Different Bank, 2 tCK Gap

5.3.3 ODT Timing Diagrams (cont'd)



NOTES:
1. BL=16, Preamble=2tCK - 0010 pattern, Postamble=1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. Figure shown with ODTLon_WR_offset=-1, ODTLoff_WR_offset=0, tRX_DQS2DQ=1UI
4. Red and Green DQS bursts are shown just for clarification purposes and are not part of an actual signal.
5. In the case of Term to Write, the host will keep the DQ signal HIGH 4UI prior to the data driven in D0.
6. The DFE should assume that 4UI prior to D0 the signal is HIGH.

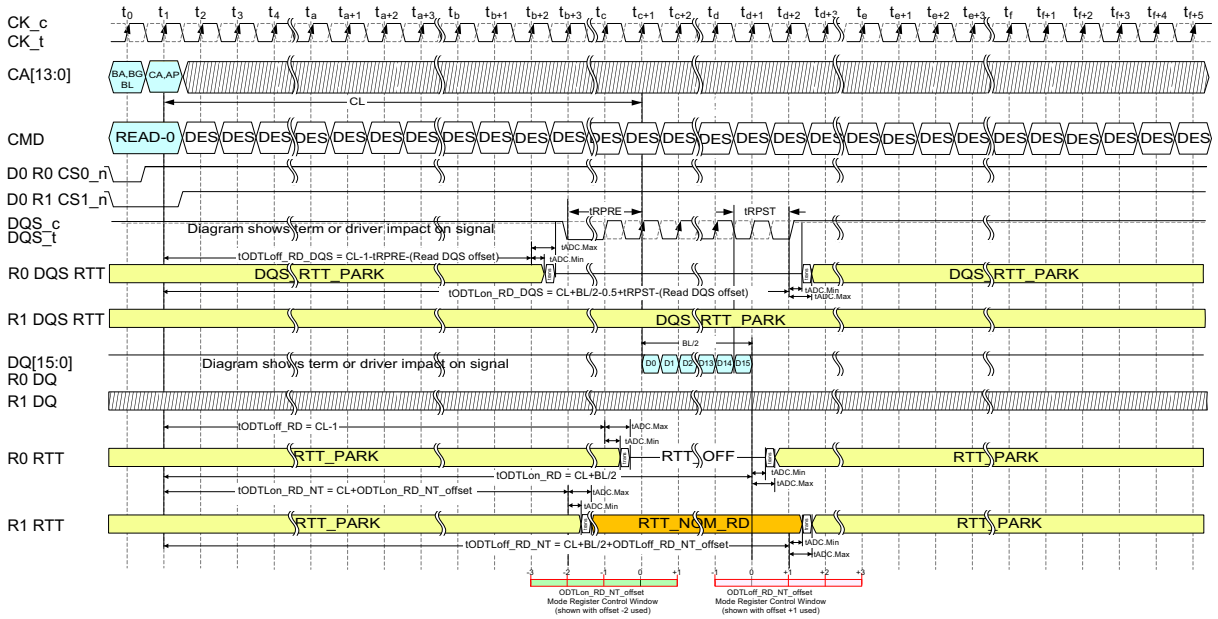
Figure 201 — WRITE (BL16) to WRITE (BL16), Different Bank, 3 tCK Gap



NOTES:
1. ODTLon_WR, ODTLon_WR_NT, ODTLoff_WR and ODTLoff_WR_NT are based on Mode Register settings that can push out or pull in the RTT enable and disable time.
2. ODTLon_RD_NT and ODTLoff_RD_NT are based on Mode Register settings that can push out or pull in the RTT enable and disable time.
3. ODTLon_WR_offset and ODTLoff_WR_offset not shown for simplicity.
4. Example shown with near ideal timings for termination settings, exact offset configurations will vary based on system designs.

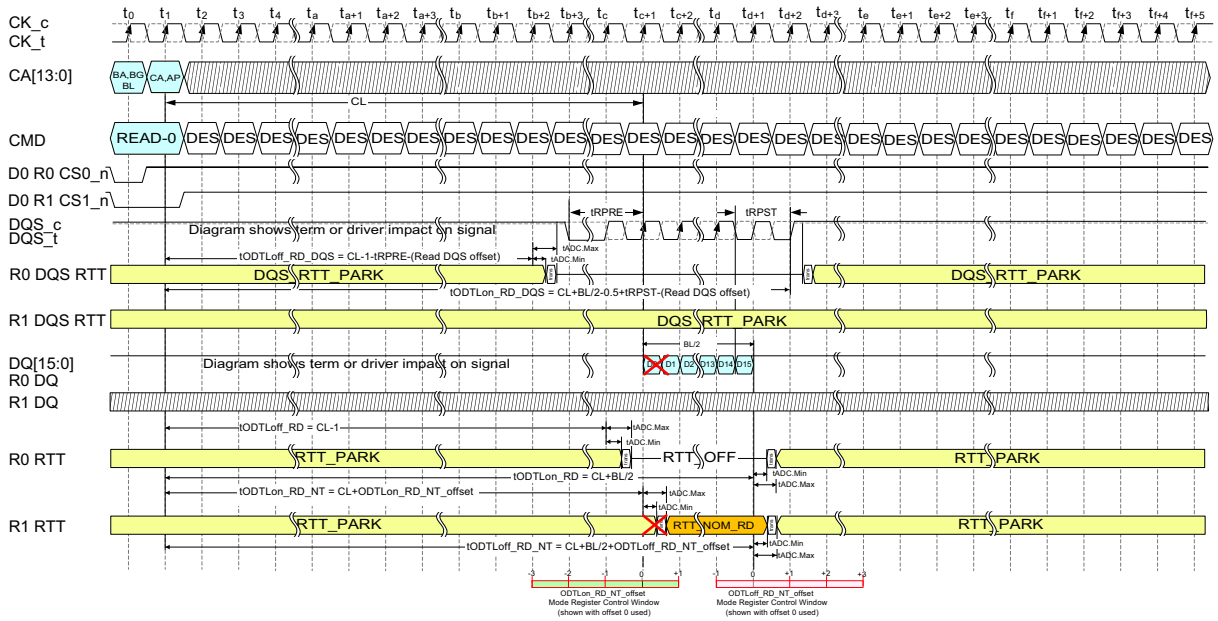
Figure 202 — Example of Read to Write Turn Around, Different Ranks

5.3.3 ODT Timing Diagrams (cont'd)



NOTES:
1. The entire range of ODTL control is now shown for simplicity.
2. Example shown with NT_ODT overlapping normal read disable by 1tCK on both sides (ODTLon_RD_NT_offset = -2 & ODTLoff_RD_NT_offset = +1)

Figure 203 — Example of Burst Read Operation ODT Latencies and Control Diagrams



NOTES:
1. The entire range of ODTL control is now shown for simplicity.
2. Since the ODTLon_RD_NT_Offset was left at zero offset and tADC still had to be considered, the NT RTT turned on too late for the non-target device. tADC is not instantaneous.
3. Since the tODTLoff_RD_NT is referenced from the CL, it is not affected by the offset used for the 'on' time and would turn off 1 clock earlier than the read disable RTT if programed to zero offset. tODTLon_RD_NT and tODTLoff_RD_NT are independently set and calculated from CL.

Figure 204 — Example of Burst Read Operation with ODTLon_RD_NT_offset Set Incorrectly

5.4 On-Die Termination for CA, CS, CK_t, CK_c

The DDR5 DRAM includes ODT (On-Die Termination) termination resistance for CK_t, CK_c, CS, and CA signals.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices via MR setting.

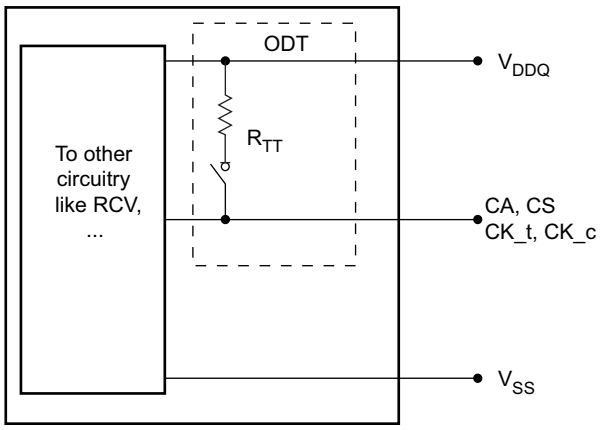


Figure 205 — A Simple Functional Representation of the DRAM CA ODT Feature

The ODT termination resistance during power up will be set to the default values based on MR32 and MR33. The ODT resistance values can be configured by those same registers.

On-Die Termination effective resistance RTT is define by MRS bits. ODT is applied to CK_t, CK_c, CS, and CA pins

$$RTT = \frac{VDDQ\text{-}Vout}{|\ I\ out\ |}$$

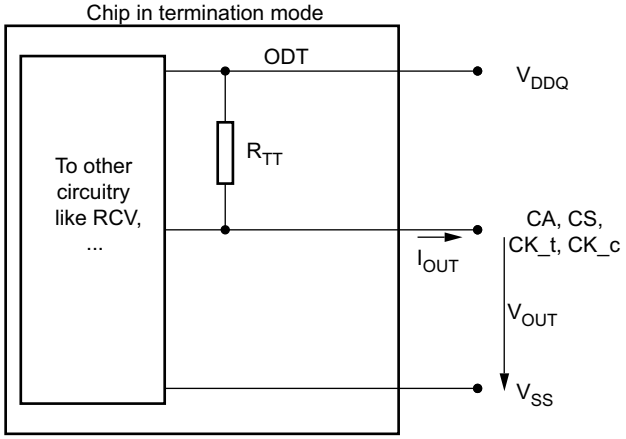


Figure 206 — A Functional Representation of the On-die Termination

5.4.1 Supported On-Die Termination Values

On-die termination effective Rtt values supported are 480, 240,120, 80, 60, and 40 ohms

Table 191 — ODT Electrical Characteristics RZQ=240 Ω +/-1%
Entire Temperature Operation Range; after Proper ZQ Calibration; VDD=VDDQ

MR	RTT	Vout	Min	Nom	Max	Unit	Note
MR32 for CK & CS MR33 for CA	480 Ω	V_{OLdc}= 0.5* VDDQ	0.7	1	1.4	R_{ZQ}*2	1, 2, 4
		V_{OMdc}= 0.8* VDDQ	0.7	1	1.3	R_{ZQ}*2	1, 2, 4
		V_{OHdc}= 0.95* VDDQ	0.6	1	1.3	R_{ZQ}*2	1, 2, 4
MR32 for CK & CS MR33 for CA	240 Ω	V_{OLdc}= 0.5* VDDQ	0.9	1	1.25	R_{ZQ}	1, 2, 4
		V_{OMdc}= 0.8* VDDQ	0.9	1	1.1	R_{ZQ}	1, 2, 4
		V_{OHdc}= 0.95* VDDQ	0.8	1	1.1	R_{ZQ}	1, 2, 4
MR32 for CK & CS MR33 for CA	120 Ω	V_{OLdc}= 0.5* VDD	0.9	1	1.25	R_{ZQ}/2	1, 2, 4, 5
		V_{OMdc}= 0.8* VDD	0.9	1	1.1	R_{ZQ}/2	1, 2, 4, 5
		V_{OHdc}= 0.95* VDD	0.8	1	1.1	R_{ZQ}/2	1, 2, 4, 5
MR32 for CK & CS MR33 for CA	80 Ω	V_{OLdc}= 0.5* VDDQ	0.9	1	1.25	R_{ZQ}/3	1, 2, 4
		V_{OMdc}= 0.8* VDDQ	0.9	1	1.1	R_{ZQ}/3	1, 2, 4
		V_{OHdc}= 0.95* VDDQ	0.8	1	1.1	R_{ZQ}/3	1, 2, 4
MR32 for CK & CS MR33 for CA	60 Ω	V_{OLdc}= 0.5* VDDQ	0.9	1	1.25	R_{ZQ}/4	1, 2, 4
		V_{OMdc}= 0.8* VDDQ	0.9	1	1.1	R_{ZQ}/4	1, 2, 4
		V_{OHdc}= 0.95* VDDQ	0.8	1	1.1	R_{ZQ}/4	1, 2, 4
MR32 for CK & CS MR33 for CA	40 Ω	V_{OLdc}= 0.5* VDDQ	0.9	1	1.25	R_{ZQ}/6	1, 2, 4
		V_{OMdc}= 0.8* VDDQ	0.9	1	1.1	R_{ZQ}/6	1, 2, 4
		V_{OHdc}= 0.95* VDDQ	0.8	1	1.1	R_{ZQ}/6	1, 2, 4
Mismatch CA-CA within Device		0.8* VDDQ	0		10	%	1, 2, 3, 4

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see “ZQ Calibration Commands” section.

NOTE 2 Pull-up ODT resistors are recommended to be calibrated at 0.8*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.5*VDDQ and 0.95*VDDQ.

NOTE 3 CA to CA mismatch within device variation for a given component including CS, CK_t and CK_c (characterized)

$$\text{CA-CA Mismatch in a Device} = \left(\frac{RTTMax - RTTMin}{RTTNOM}\right) \times 100$$

NOTE 4 Without ZQ calibration ODT effective RTT values have an increased tolerance of +/- 30%

NOTE 5 CK ODT RZQ/2 (120Ω), CS ODT RZQ/2 (120Ω), and CA ODT RZQ/2 (120 Ω) are only supported at >5200 MT/s data rates.

5.5 On-Die Termination for Loopback Signals

The DDR5 DRAM includes ODT (On-Die Termination) termination resistance for the Loopback signals LBDQS and LBDQ. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices via MR setting.

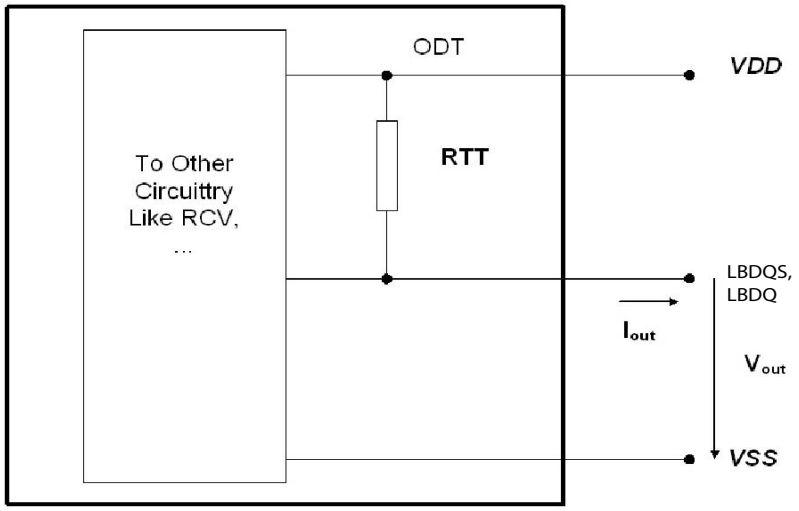


Figure 207 — Functional Representation of Loopback ODT

The ODT termination resistance during power up will be set to the default RTT_OFF values based on MR36:OP[2:0] definition. The ODT resistance values can be configured by MR26:OP[2:0].

On-Die Termination effective resistance RTT is defined by MR36:OP[2:0] bits = 48 ohms.

ODT is applied to Loopback signals LBDQS and LBDQ. On die termination effective Rtt values supported for the Loopback pins is 48 ohms.

$$RTT = \frac{VDDQ - Vout}{|\ Iout\ |}$$

Table 192 — ODT Electrical Characteristics RZQ=240 Ω +/-1%
Entire Temperature Operation Range; after Proper ZQ Calibration; VDD=VDDQ

RTT	Vout	Min	Nom	Max	Unit	NOTE
48 ohms	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1, 2
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1, 2
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/5	1, 2
Mismatch LBDQS - LBDQ within device	VOMdc = 0.8* VDDQ	0		8	%	1, 2, 3

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see “ZQ Calibration Commands” section.

NOTE 2 Pull-up ODT resistors are recommended to be calibrated at 0.8*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5*VDDQ and 0.95*VDDQ.

NOTE 3 Loopback ODT mismatch within device variation for a given component including LBDQS and LBDQ

$$LBDQS\text{-}LBDQ\ Mismatch\ in\ a\ Device = \left(\frac{RTTMax - RTTMin}{RTTNOM}\right) \times 100$$

5.6 On-Die Termination Timing Definitions

5.6.1 Test Load for ODT Timings

The reference load for On-Die Termination (ODT) timings is defined in Figure 208:

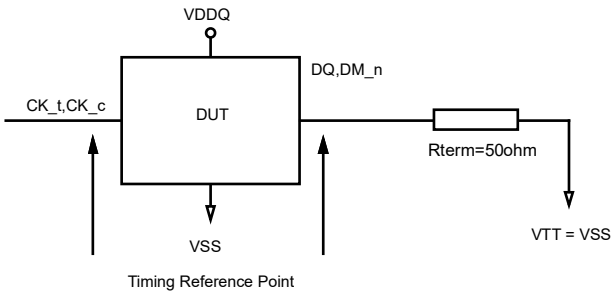


Figure 208 — ODT Timing Reference Load

5.6.2 tADC Measurement Method

Table 193 — tADC Measurement Timing Definitions

Measured Parameter	Begin Point Definition	End Point Definition	Figure
tADC for Target DRAM Write	End of tODTLoff_WR at CK_t/CK_c differential crossing point	Extrapolated point at VRTT_WR	Figure 209
	End of tODTLon_WR at CK_t/CK_c differential crossing point	Extrapolated point at VSS	
tADC for Non Target DRAM Write	End of tODTLoff_WR_NT at CK_t/CK_c differential crossing point	Extrapolated point at VRTT_NOM_WR	Figure 210
	End of tODTLon_WR_NT at CK_t/CK_c differential crossing point	Extrapolated point at VSS	
tADC for Non Target DRAM Read	End of tODTLoff_RD_NT at CK_t/CK_c differential crossing point	Extrapolated point at VRTT_NOM_RD	Figure 211
	End of tODTLon_RD_NT at CK_t/CK_c differential crossing point	Extrapolated point at VSS	

Table 194 — Reference Setting for ODT Timing Measurement

Measured Parameter	RTT_PARK	RTT_WR	RTT_NOM_WR	RTT_NOM_RD	Vsw1	Vsw2	Figure	Note
tADC for Target DRAM Write	RTT_OFF	RZQ/7	-	-	0.20V	0.40V	208	1, 4
tADC for Non Target DRAM Write	RTT_OFF	-	RZQ/7	-	0.20V	0.40V	209	2, 4
tADC for Non Target DRAM Read	RTT_OFF	-	-	RZQ/7	0.20V	0.40V	210	3, 4

NOTE 1 MR34 OP[2:0]=000B (RTT_PARK Setting); MR34 OP[5:3]=111B (RTT_WR Setting)

NOTE 2 MR34 OP[2:0]=000B (RTT_PARK Setting); MR35 OP[2:0]=111B (RTT_NOM_WR Setting)

NOTE 3 MR34 OP[2:0]=000B (RTT_PARK Setting); MR35 OP[5:3]=111B (RTT_NOM_RD Setting)

NOTE 4 tADC measurement method applies to DQs/DM only. It does not apply to DQS_t, DQS_c, TDQS_t and TDQS_c since there is no transition from DQS_RTT_PARK.

5.6.2 tADC Measurement Method (cont'd)

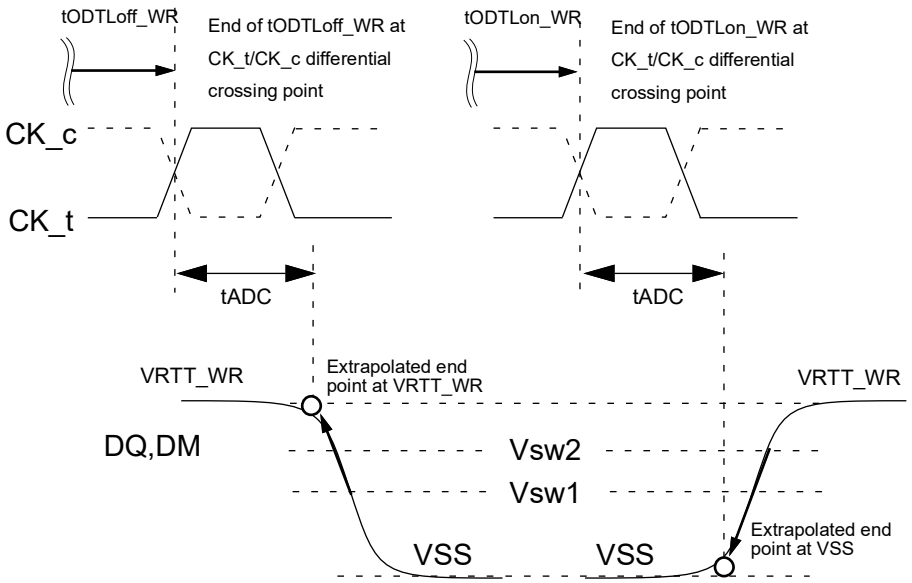


Figure 209 — tADC Measurement Method Target DRAM Write

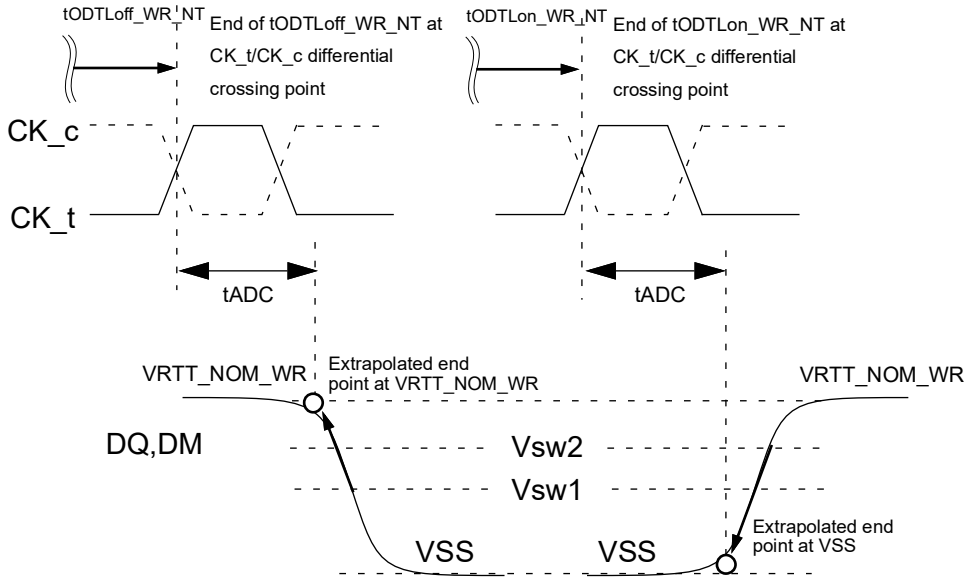


Figure 210 — tADC Measurement Method Non-Target DRAM Write

5.6.2 tADC Measurement Method (cont'd)

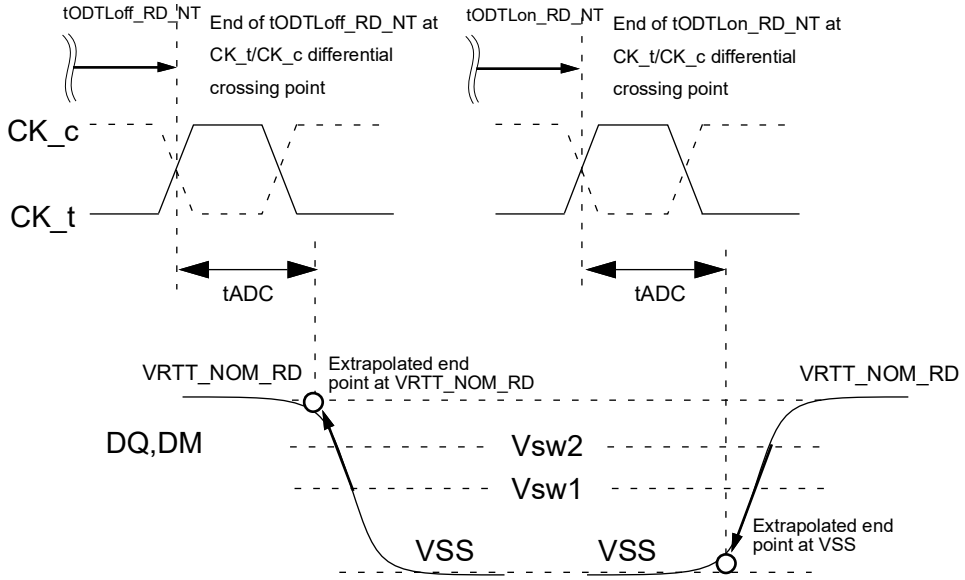


Figure 211 — tADC Measurement Method Non-Target DRAM Read

6 AC and DC Operating Conditions

6.1 Absolute Maximum Ratings

Table 195 — Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.4	V	1, 3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.4	V	1, 3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 2.1	V	4
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.3 ~ 1.4	V	1, 3, 5
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

NOTE 1 Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

NOTE 2 Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

NOTE 3 VDD and VDDQ must be within 300 mV of each other at all times. When VDD and VDDQ are less than 500 mV

NOTE 4 VPP must be equal or greater than VDD/VDDQ at all times.

NOTE 5 Overshoot area above 1.5 V is specified in Section 8.3.4, Section 8.3.5, and Section 8.3.6.

6.2 DC Operating Conditions

Table 196 — DC Operating Conditions

Symbol	Parameter	Low Freq Voltage Spec Freq: DC to 2 MHz				Notes
		Min.	Typ.	Max.	Unit	
VDD	Device Supply Voltage	1.067 (-3%)	1.1	1.166 (+6%)	V	1,2,3,4
VDDQ	Supply Voltage for I/O	1.067 (-3%)	1.1	1.166 (+6%)	V	1,2,3,4
VPP	Core Power Voltage	1.746 (-3%)	1.8	1.908 (+6%)	V	2,3,4

NOTE 1 VDD must be within 66 mv of VDDQ

NOTE 2 This includes all voltage noise from DC to 2 MHz at the DRAM package ball

NOTE 3 For DIMM Z(f), JEDEC recommends to refer to the DIMM Z(f) specification

NOTE 4 For solder down component Z(f), JEDEC recommends to refer to each DRAM memory vendor's Z(f) guidance

6.3 DRAM Component Operating Temperature Range

Table 197 — DC Operating Temperature Range

Symbol	Parameter	Temperature Range (Unit: °C)		Grade	Notes
		Min	Max		
Toper_normal	Normal Operating Temperature	0	85	NT	1, 2, 3, 4
Toper_extended	Extended Operating Temperature	0	95	XT	1, 2, 3, 4, 5

NOTE 1 All operating temperature symbols, ranges, acronyms are referred from JESD402-1.

NOTE 2 Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

NOTE 3 All DDR5 SDRDAMs are required to operate in NT and XT temperature ranges.

NOTE 4 When operating above 85 °C, the host shall provide appropriate Refresh mode controls associated with the increased temperature range. The full description of these settings are defined in Table 68 in section 4.13.5

NOTE 5 Operating Temperature for 3DS needs to be derated by the number of DRAM dies as: $[T_{OPER} - (2.5\ °C \times \log_2 N)]$, where N is the number of the stacked dies.

7 AC and DC Global Definitions

7.1 Bit Error Rate

7.1.1 Introduction

This clause provides an overview of the Bit Error Rate (BER) and the desired Statistical Level of Confidence.

7.1.2 General Equation

$$n = \left(\frac{1}{BER}\right)\left[-\ln(1-SLC) + \ln\left(\sum_{k=0}^{N}\frac{(n\cdot BER)^k}{k!}\right)\right]$$

Where:

n = number of bits in a trial
SLC = statistical level of confidence
BER = Bit Error Rate
k = intermediate number of specific errors found in trial
N = number of errors recorded during trial

If no, errors are assumed in a given test period, the second term drops out and the equation becomes:

$$n = \left(\frac{1}{BER}\right)[-\ln(1-SLC)]$$

JEDEC recommends testing to 99.5% confidence levels; however, one may choose a number that is viable for their own manufacturing levels. To determine how many bits of data should be sent (again, assuming zero errors, or N=0), using BER=E^{-9} and confidence level SLC=99.5%, the result is n=(1/BER)(-ln(1-0.995) =5.298x10^9.

Results for commonly used confidence levels of 99.5% down to 70% are shown in Table 198.

Table 198 — Estimated Number of Transmitted Bits (n) for the Confidence Level of 70% to 99.5%

Number Errors	n = -ln(1-SLC)/BER							
	99.5%	99%	95%	90%	85%	80%	75%	70%
0	5.298/BER	4.61/BER	2.99/BER	2.3/BER	1.90/BER	1.61/BER	1.39/BER	1.20/BER

7.1.3 Minimum Bit Error Rate (BER) Requirements

Table 199 specifies the UIavg and Bit Error Rate requirements over which certain receiver and transmitter timing and voltage specifications need to be validated assuming a 99.5% confidence level at BER=E^{-9}.

Table 199 — Minimum BER Requirements for Rx/Tx Timing and Voltage Tests

Parameter	Symbol	DDR5-3200 to DDR5-9200			Unit	Notes
		Min	Nom	Max		
Average UI	UI_{AVG}	0.999* nominal	1000/f	1.001* nominal	ps	1
Number of UI (min)	$N_{Min_UI_Validation}$	$5.3x10^9$	-	-	UI	2
Bit Error Rate	BER_{Lane}	-	-	E-16	Events	3, 4, 5

NOTE 1 Average UI size, "f" is data rate

NOTE 2 # of UI over which certain Rx/Tx timing and voltage specifications need to be validated assuming a 99.5% confidence level at BER=E^{-9}.

NOTE 3 This is a system parameter. It is the raw bit error rate for every lane before any logical PHY or link layer based correction. It may not be possible to have a validation methodology for this parameter for a standalone transmitter or standalone receiver, therefore, this parameter has to be validated in selected systems using a suitable methodology as deemed by the platform.

NOTE 4 Bit Error Rate per lane. This is a raw bit error rate before any correction. This parameter is primarily used to determine electrical margins during electrical analysis and measurements that are located between two interconnected devices.

NOTE 5 This is the minimum BER requirements for testing timing and voltage parameters listed in Input Clock Jitter, Rx DQS & DQ Voltage Sensitivity, Rx DQS Jitter Sensitivity, Rx DQ Stressed Eye, Tx DQS Jitter, Tx DQ Jitter, and Tx DQ Stressed EH/EW specifications.

7.2 Unit Interval and Jitter Definitions

This section describes the Unit Interval (UI) and UI Jitter definitions associated with the jitter parameters specified in the Input Clock Jitter, Rx Stressed Eye, Tx DQS Jitter, and Tx DQ Jitter sections of this specification.

7.2.1 Unit Interval (UI)

The definition of Unit Interval (UI) is a minimum time interval between condition changes of a signal. DDR-based signals are referenced to the differential crossing point of CK_t and CK_c. 2UI=1tCK for DDR-based signals (for example, DQ, DQS).

The UI definitions shown in Figure 212 and Figure 213 are for DDR-based signals. The times at which the differential crossing points of the clock occur are defined at t1, t2, …, tn-1, tn. The UI at index "n" is defined as an arbitrary time in steady state, where n=0 is chosen as the starting crossing point.

$$UI_n = t_n - t_{n-1}$$

Figure 212 — UI Definition in Terms of Adjacent Edge Timings

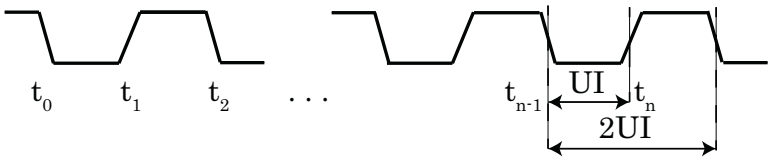


Figure 213 — UI Definition Using Clock Waveforms

7.2.2 UI Jitter Definition

If a number of UI edges are computed or measured at times t1, t2, …, tn-1, tn,..., tK, where K is the maximum number of samples, then the UI jitter at any instance "n" is defined in Figure 214, where T = the ideal UI size.

$$UI_{(jit)_n} = \left(t_n - t_{n-1}\right) - T\ , \quad n=1,2,3,...,K$$

Figure 214 — UI Jitter for "nth" UI Definition (in Terms of Ideal UI)

In a large sample with random Gaussian-like jitter (therefore very close to symmetric distribution), the average of all UI sizes usually turns out to be very close to the ideal UI size.

The equation described in Figure 214 assumes starting from an instant steady state, where n=0 is chosen as the starting point. 1 UI = one bit, which means 2 UI = one full cycle or time period of the forwarded strobe. Example: For 6.4 GT/s signaling, the forwarded strobe frequency is 3.2 GHz, or 1 UI = 156.25 ps.

Deterministic jitter is analyzed in terms of the peak-to-peak value and in terms of specific frequency components present in the jitter, isolating the causes for each frequency. Random jitter is unbounded and analyzed in terms of statistical distribution to convert to a bit error rate (BER) for the link.

7.2.3 UI-UI Jitter Definition

UI-UI (read as "UI to UI") jitter is defined to be the jitter between two consecutive UI as shown in Figure 215.

$$\Delta UI_n = UI_n - UI_{n-1} \qquad n=2,3,...,K$$

Figure 215 — UI-UI Jitter Definitions

7.2.4 Accumulated Jitter (Over "N" UI)

Accumulated jitter is defined as the jitter accumulated over any consecutive "N" UI as shown in Figure 216.

$$T_{acc}^{N} = \sum_{p=m}^{m+N-1}(UI_p - \overline{UI}) \qquad m=1,2,...,K\text{-}N$$

Figure 216 — Definition of Accumulated Jitter (over "N" UI)

where $\overline{UI}$ is defined in the equation shown in Figure 217.

$$\overline{UI} = \frac{\sum_{p=1}^{K} UI_p}{K} \quad p=1,2,...,N,...,K$$

Figure 217 — Definition of $\overline{UI}$

8 AC and DC Input Measurement Levels

8.1 Overshoot and Undershoot Specifications for CAC - No Ballot

8.2 CA Rx Voltage and Timings

Note: The following draft assumes internal CA VREF. If the VREF is external, the specs will be modified accordingly.

The command and address (CA) including CS input receiver compliance mask for voltage and timing is shown in Figure 218. All CA signals apply the same compliance mask and CS signal applies its own compliance mask independently. All signals applied to the compliance mask operate in single data rate mode.

The CA input receiver mask for voltage and timing is shown in the figure below is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

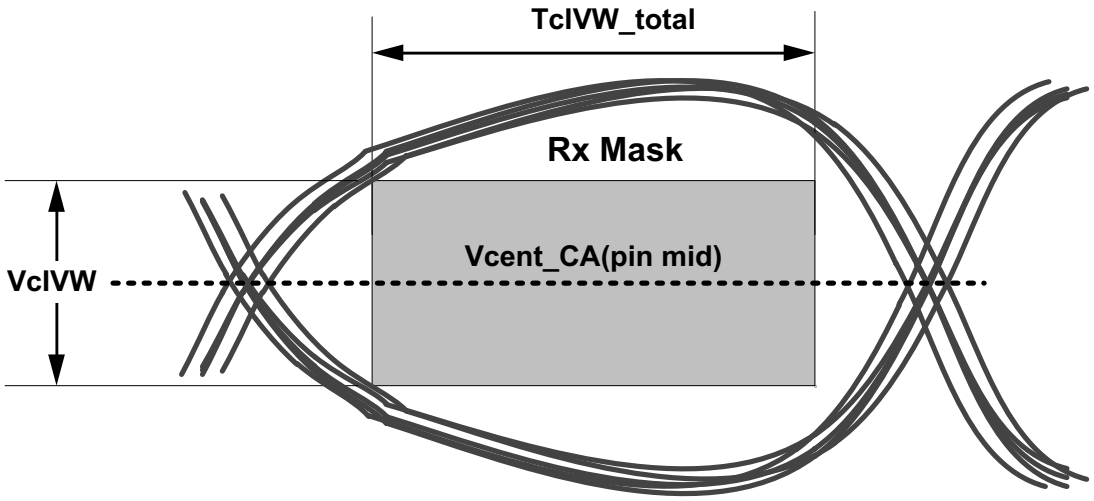


Figure 218 — CA Receiver (Rx) Mask

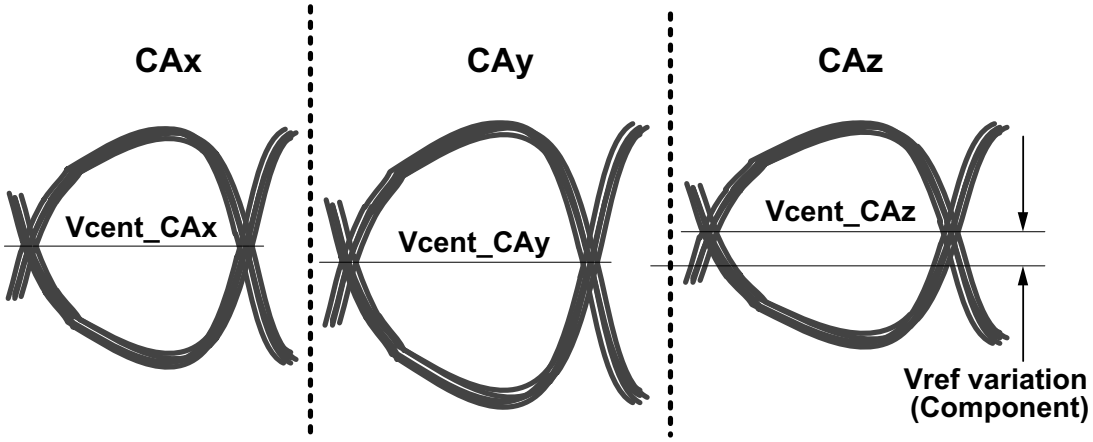
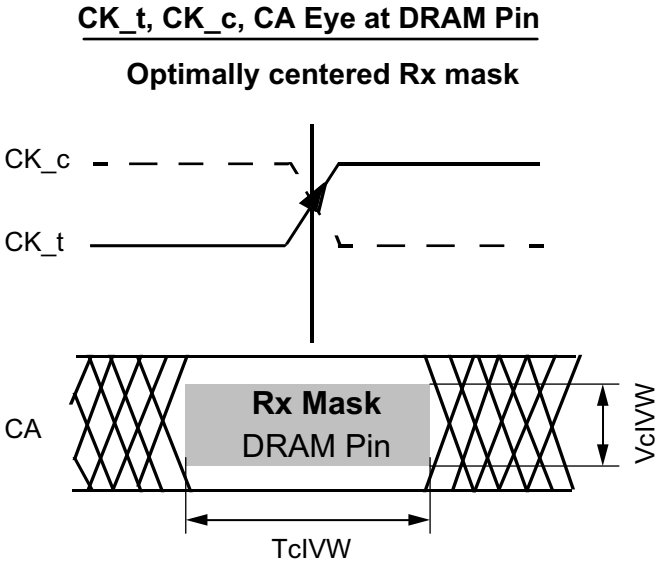


Figure 219 — Across Pin V_{REF}CA Voltage Variation

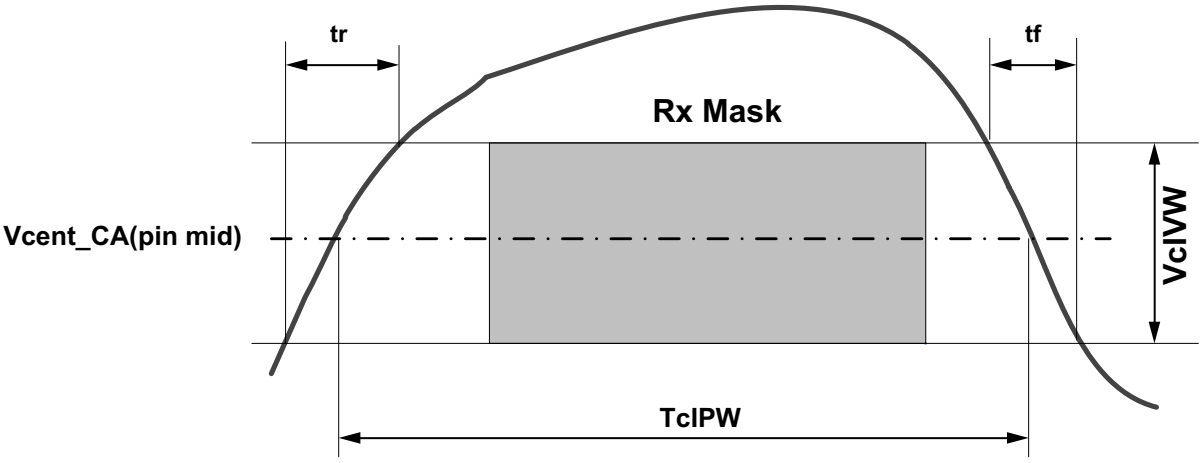
Vcent_CA(pin mid) is defined as the midpoint between the largest Vcent_CA voltage level and the smallest Vcent_CA voltage level across all CA and CS pins for a given DRAM component. Each CA Vcent level is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in Figure 219. This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask. The component level V_{REF} will be set by the system to account for Ron and ODT settings.

8.2 CA Rx Voltage and Timings (cont'd)



TcIVW is not necessarily center aligned on CK_t/CK_c crossing at the DRAM pin, but is assumed to be center aligned at the DRAM Latch.

Figure 220 — CA Timings at the DRAM Pins



Note
1. SRIN_cIVW=VcIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

Figure 221 — CA TcIPW and SRIN_cIVW Definition (for Each Input Pulse)

8.2 CA Rx Voltage and Timings (cont'd)

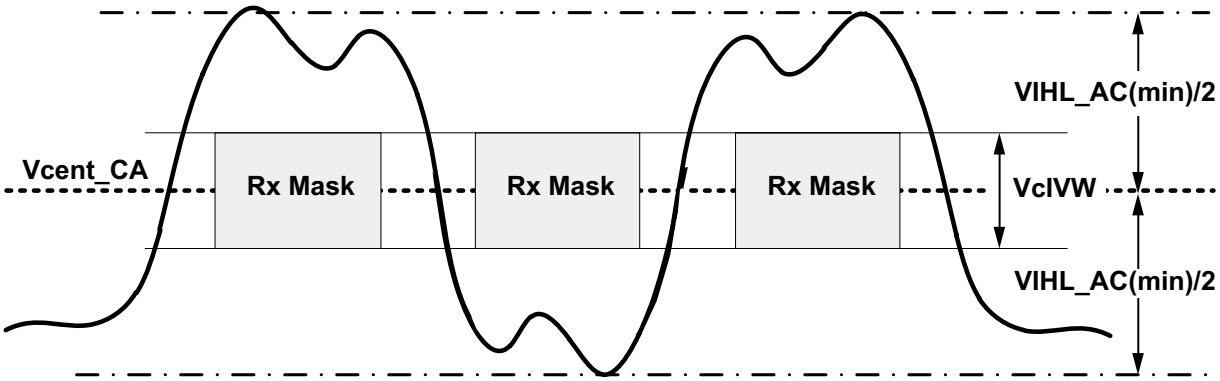


Figure 222 — CA VIHL_AC Definition (for Each Input Pulse)

Table 200 — DRAM CA, CS Parametric Values for DDR5-3200 to 4800

Parameter	Symbol	x4, x8, and x16 Devices										Unit	Notes
		DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Rx Mask voltage - p-p	VciVW	140	-	140	-	140	-	130	-	130	-	mV	1, 2, 4
Rx Timing Window	TcIVW	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	tCK	1, 2, 3, 4
CA Input Pulse Amplitude	VIHL_AC	160		160		160		150		150		mV	7
CA Input Pulse Width	TcIPW	0.58		0.58		0.58		0.58		0.58		tCK	5
Input Slew Rate over VcIVW	SRIN_cIVW	1	7	1	7	1	7	1	7	1	7	V/ns	6

NOTE 1 CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
NOTE 2 Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).
NOTE 3 Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
NOTE 4 Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode.
NOTE 5 CA only minimum input pulse width defined at the Vcent_CA(pin mid).
NOTE 6 Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
NOTE 7 VIHL_AC does not have to be met when no transitions are occurring.

8.2 CA Rx Voltage and Timings (cont'd)

Table 201 — DRAM CA, CS Parametric Values for DDR5-5200 to 5600

Parameter	Symbol	x4 and x8 Devices												x16 Device		Unit	Notes
		Option 3				Option 2				Option 1							
		10 ps <= Tpkg_Delay_CA <=29 ps				29 ps < Tpkg_Delay_CA <=32 ps				32 ps < Tpkg_Delay_CA <=35 ps							
		DDR5-5200		DDR5-5600		DDR5-5200		DDR5-5600		DDR5-5200		DDR5-5600		DDR5-5200 to 5600			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Rx Mask voltage - p-p	VciVW	110	-	110	-	95 (Cl max =0.5 5pF) 100 (Cl max =0.5 pF)	-	95 (Cl max =0.5 5pF) 100 (Cl max =0.5 pF)	-	80 (Cl max =0.5 5pF) 85 (Cl max =0.5 pF)	-	80 (Cl max =0.5 5pF) 85 (Cl max =0.5 pF)	-	110	-	mV	1, 2, 4
Rx Timing Window	TcIVW	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	UI*	1, 2, 3, 4, 8
CA Input Pulse Amplitude	VIHL_AC	125	-	125	-	115	-	115	-	110	-	110	-	125	-	mV	7
CA Input Pulse Width	TcIPW	0.58		0.58		0.58		0.58		0.58		0.58		0.58		UI*	5, 8
Input Slew Rate over VcIVW	SRIN_cIVW	1	7	1	7	1	7	1	7	1	7	1	7	1	7	V/ns	6

NOTE 1 CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
NOTE 2 Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).
NOTE 3 Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
NOTE 4 Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode.
NOTE 5 CA only minimum input pulse width defined at the Vcent_CA(pin mid).
NOTE 6 Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
NOTE 7 VIHL_AC does not have to be met when no transitions are occurring.
NOTE 8 * UI=tck(avg)min

Table 202 — DRAM CA, CS Parametric Values for DDR5-6000 to 6400

Parameter	Symbol	x4 and x8 Devices												x16 Device		Unit	Notes
		Option 3				Option 2				Option 1							
		10 ps <= Tpkg_Delay_CA <=29 ps				29 ps < Tpkg_Delay_CA <=32 ps				32 ps < Tpkg_Delay_CA <=35 ps							
		DDR5-6000		DDR5-6400		DDR5-6000		DDR5-6400		DDR5-6000		DDR5-6400		DDR5-6000 to 6400			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Rx Mask voltage - p-p	VciVW	95	-	95	-	85	-	85	-	80	-	80	-	95	-	mV	1, 2, 4
Rx Timing Window	TcIVW	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	UI*	1, 2, 3, 4, 8
CA Input Pulse Amplitude	VIHL_AC	115	-	115	-	105	-	105	-	100	-	100	-	115	-	mV	7
CA Input Pulse Width	TcIPW	0.58		0.58		0.58		0.58		0.58		0.58		0.58		UI*	5, 8
Input Slew Rate over VcIVW	SRIN_cIVW	1	7	1	7	1	7	1	7	1	7	1	7	1	7	V/ns	6

NOTE 1 CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
NOTE 2 Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).
NOTE 3 Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
NOTE 4 Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode.
NOTE 5 CA only minimum input pulse width defined at the Vcent_CA(pin mid).
NOTE 6 Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
NOTE 7 VIHL_AC does not have to be met when no transitions are occurring.
NOTE 8 * UI=tck(avg)min

8.2 CA Rx Voltage and Timings (cont'd)

Table 203 — DRAM CA, CS Parametric Values for DDR5-6800 to 7200

Parameter	Symbol	x4 and x8 Devices												x16 Device		Unit	Notes
		Option 3				Option 2				Option 1							
		10 ps <= Tpkg_Delay_CA <=29 ps				29 ps < Tpkg_Delay_CA <=32 ps				32 ps < Tpkg_Delay_CA <=35 ps							
		DDR5-6800		DDR5-7200		DDR5-6800		DDR5-7200		DDR5-6800		DDR5-7200		DDR5-6800 to 7200			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Rx Mask voltage - p-p	VciVW	90	-	90	-	80	-	80	-	50	-	50	-	90	-	mV	1, 2, 4
Rx Timing Window	TcIVW	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	UI*	1, 2, 3, 4, 8
CA Input Pulse Amplitude	VIHL_AC	110	-	110	-	100	-	100	-	70	-	70	-	110	-	mV	7
CA Input Pulse Width	TcIPW	0.58		0.58		0.58		0.58		0.58		0.58		0.58		UI*	5, 8
Input Slew Rate over VcIVW	SRIN_cIVW	1	7	1	7	1	7	1	7	1	7	1	7	1	7	V/ns	6

NOTE 1 CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
NOTE 2 Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).
NOTE 3 Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
NOTE 4 Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode.
NOTE 5 CA only minimum input pulse width defined at the Vcent_CA(pin mid).
NOTE 6 Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
NOTE 7 VIHL_AC does not have to be met when no transitions are occurring.
NOTE 8 * UI=tck(avg)min

Table 204 — DRAM CA, CS Parametric Values for DDR5-7600 to 8000

Parameter	Symbol	x4 and x8 Devices												x16 Device		Unit	Notes
		Option 3				Option 2				Option 1							
		10 ps <= Tpkg_Delay_CA <=29 ps				29 ps < Tpkg_Delay_CA <=32 ps				32ps < Tpkg_Delay_CA <=35 ps							
		DDR5-7600		DDR5-8000		DDR5-7600		DDR5-8000		DDR5-7600		DDR5-8000		DDR5-7600 to 8000			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Rx Mask voltage - p-p	VciVW	85	-	85	-	75	-	75	-	45	-	45	-	85	-	mV	1, 2, 4
Rx Timing Window	TcIVW	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	UI*	1, 2, 3, 4, 8
CA Input Pulse Amplitude	VIHL_AC	105	-	105	-	95	-	95	-	65	-	65	-	105	-	mV	7
CA Input Pulse Width	TcIPW	0.58		0.58		0.58		0.58		0.58		0.58		0.58		UI*	5, 8
Input Slew Rate over VcIVW	SRIN_cIVW	1	7	1	7	1	7	1	7	1	7	1	7	1	7	V/ns	6

NOTE 1 CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
NOTE 2 Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).
NOTE 3 Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
NOTE 4 Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode.
NOTE 5 CA only minimum input pulse width defined at the Vcent_CA(pin mid).
NOTE 6 Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
NOTE 7 VIHL_AC does not have to be met when no transitions are occurring.
NOTE 8 * UI=tck(avg)min

8.2 CA Rx Voltage and Timings (cont'd)

Table 205 — DRAM CA, CS Parametric Values for DDR5-8400 to 8800

Parameter	Symbol	x4 and x8 Devices												x16 Device		Unit	Notes
		Option 3				Option 2				Option 1							
		10 ps <= Tpkg_Delay_CA <=29 ps				29 ps < Tpkg_Delay_CA <=32 ps				32 ps < Tpkg_Delay_CA <=35 ps							
		DDR5-8400		DDR5-8800		DDR5-8400		DDR5-8800		DDR5-8400		DDR5-8800		DDR5-8400 to 8800			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Rx Mask voltage - p-p	VciVW	80	-	80	-	70	-	70	-	40	-	40	-	80	-	mV	1, 2, 4
Rx Timing Window	TclVW	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	UI*	1, 2, 3, 4, 8
CA Input Pulse Amplitude	VIHL_AC	100	-	100	-	90	-	90	-	60	-	60	-	100	-	mV	7
CA Input Pulse Width	TclPW	0.58		0.58		0.58		0.58		0.58		0.58		0.58		UI*	5, 8
Input Slew Rate over VclVW	SRIN_clVW	1	7	1	7	1	7	1	7	1	7	1	7	1	7	V/ns	6

NOTE 1 CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
NOTE 2 Rx mask voltage VclVW total(max) must be centered around Vcent_CA(pin mid).
NOTE 3 Rx differential CA to CK jitter total timing window at the VclVW voltage levels.
NOTE 4 Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode.
NOTE 5 CA only minimum input pulse width defined at the Vcent_CA(pin mid).
NOTE 6 Input slew rate over VclVW Mask centered at Vcent_CA(pin mid).
NOTE 7 VIHL_AC does not have to be met when no transitions are occurring.
NOTE 8 * UI=tck(avg)min

Table 206 — DRAM CA, CS Parametric Values for DDR5-9200

Parameter	Symbol	x4 and x8 Devices						x16 Device		Unit	Notes
		Option 3		Option 2		Option 1					
		10 ps <= Tpkg_Delay_CA <=29 ps		29 ps < Tpkg_Delay_CA <=32 ps		32 ps < Tpkg_Delay_CA <=35 ps					
		DDR5-9200		DDR5-9200		DDR5-9200		DDR5-9200			
		Min	Max	Min	Max	Min	Max	Min	Max		
Rx Mask voltage - p-p	VciVW	77.5	-	67.5	-	37.5	-	77.5	-	mV	1, 2, 4
Rx Timing Window	TclVW	0.2	-	0.2	-	0.2	-	0.2	-	UI*	1, 2, 3, 4, 8
CA Input Pulse Amplitude	VIHL_AC	100	-	90	-	60	-	100	-	mV	7
CA Input Pulse Width	TclPW	0.58		0.58		0.58		0.58		UI*	5, 8
Input Slew Rate over VclVW	SRIN_clVW	1	7	1	7	1	7	1	7	V/ns	6

NOTE 1 CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
NOTE 2 Rx mask voltage VclVW total(max) must be centered around Vcent_CA(pin mid).
NOTE 3 Rx differential CA to CK jitter total timing window at the VclVW voltage levels.
NOTE 4 Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode.
NOTE 5 CA only minimum input pulse width defined at the Vcent_CA(pin mid).
NOTE 6 Input slew rate over VclVW Mask centered at Vcent_CA(pin mid).
NOTE 7 VIHL_AC does not have to be met when no transitions are occurring.
NOTE 8 * UI=tck(avg)min

8.3 Input Clock Jitter Specification

8.3.1 Overview

The clock is being driven to the DRAM either by the RCD for L/RDIMM modules, or by the host for U/SODIMM modules (Figure 223).

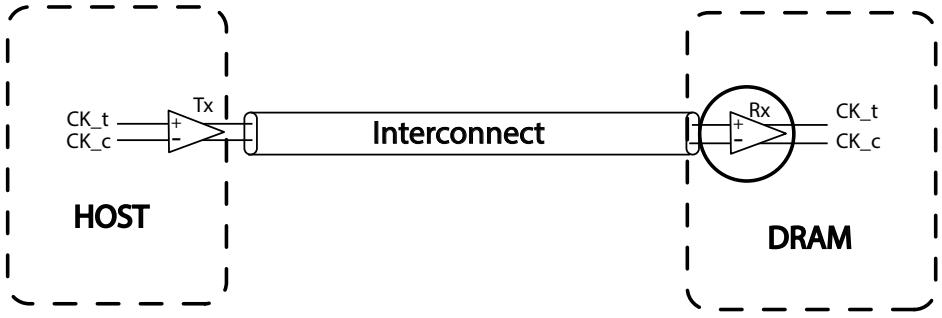


Figure 223 — HOST Driving Clock Signals to the DRAM

8.3.2 Specification for DRAM Input Clock Jitter

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. Input clock violating the min/max jitter values may result in malfunction of the DDR5 SDRAM device.

Table 207 — DRAM Input Clock Jitter Specifications for DDR5-3200 to 4400

[BUJ=Bounded Uncorrelated Jitter; DCD=Duty Cycle Distortion; Dj=Deterministic Jitter; Rj=Random Jitter; Tj=Total jitter; pp=Peak-to-Peak]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DRAM Reference clock frequency	tCK	0.9999 * f0	1.0001 * f0	0.9999 * f0	1.0001 * f0	0.9999 * f0	1.0001 * f0	0.9999 * f0	1.0001 * f0	0.9999 * f0	1.0001 * f0	MHz	1, 11
Duty Cycle Error	tCK_Duty_UI_Error	-	0.05	-	0.05	-	0.05	-	0.05		0.05	UI	1, 4, 11
Rj RMS value of 1-UI Jitter	tCK_1UI_Rj_NoBUJ	-	0.0037	-	0.0037	-	0.0037	-	0.0037	-	0.0037	UI (RMS)	3, 5, 11
Dj pp value of 1-UI Jitter	tCK_1UI_Dj_NoBUJ	-	0.030	-	0.030	-	0.030	-	0.030	-	0.030	UI	3, 6, 11
Tj value of 1-UI Jitter	tCK_1UI_Tj_NoBUJ	-	0.090	-	0.090	-	0.090	-	0.090	-	0.090	UI	3, 6, 11
Rj RMS value of N-UI Jitter, where N=2,3	tCK_NUI_Rj_NoBUJ, where N=2,3	-	0.0040	-	0.0040	-	0.0040	-	0.0040	-	0.0040	UI (RMS)	3, 7, 11
Dj pp value of N-UI Jitter, where N=2,3	tCK_NUI_Dj_NoBUJ, where N=2,3	-	0.074	-	0.074	-	0.074	-	0.074	-	0.074	UI	3, 7, 11
Tj value of N-UI Jitter, where N=2,3	tCK_NUI_Tj_NoBUJ, where N=2,3	-	0.140	-	0.140	-	0.140	-	0.140	-	0.140	UI	3, 8, 11
Rj RMS value of N-UI Jitter, where N=4,5,6,...,30	tCK_NUI_Rj_NoBUJ, where N=4,5,6,...,30	-	-	-	-	-	-	-	-	-	-	UI (RMS)	3, 9, 11, 12
Dj pp value of N-UI Jitter, N=4,5,6,...,30	tCK_NUI_Dj_NoBUJ, where N=4,5,6,...,30	-	-	-	-	-	-	-	-	-	-	UI	3, 10, 11, 12
Tj value of N-UI Jitter, N=4,5,6,...,30	tCK_NUI_Tj_NoBUJ, where N=4,5,6,...,30	-	-	-	-	-	-	-	-	-	-	UI	3, 10, 11, 12

NOTE 1 f0 = Data Rate/2, example: if data rate is 3200 MT/s, then f0=1600

NOTE 2 Rise and fall time slopes (V / nsec) are measured between +100 mV and -100 mV of the differential output of reference clock

NOTE 3 On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility

NOTE 4 Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.

NOTE 5 Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD

NOTE 6 Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD

NOTE 7 Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD

NOTE 8 Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD

NOTE 9 Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD

NOTE 10 Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD

NOTE 11 The validation methodology for these parameters will be covered in future ballots.

NOTE 12 If the clock meets total jitter Tj at BER of $1E^{-16}$, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of $1E^{-16}$

8.3.2 Specification for DRAM Input Clock Jitter (cont'd)

Table 208 — DRAM Input Clock Jitter Specifications for DDR5-5200 to 6400

[BUJ=Bounded Uncorrelated Jitter; DCD=Duty Cycle Distortion; Dj=Deterministic Jitter; Rj=Random Jitter; Tj=Total jitter; pp=Peak-to-Peak]

Parameter	Symbol	DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
DRAM Reference clock frequency	tCK	0.9999* f0	1.0001* f0	0.9999* f0	1.0001* f0	0.9999* f0	1.0001* f0	0.9999* f0	1.0001* f0	MHz	1, 11
Duty Cycle Error	tCK_Duty_UI_Error	-	0.05	-	0.05	-	0.05	-	0.05	UI	1, 4, 11
Rj RMS value of 1-UI Jitter	tCK_1UI_Rj_NoBUJ	-	0.0037	-	0.0037	-	0.0037	-	0.0037	UI (RMS)	3, 5, 11
Dj pp value of 1-UI Jitter	tCK_1UI_Dj_NoBUJ	-	0.030	-	0.030	-	0.030	-	0.030	UI	3, 6, 11
Tj value of 1-UI Jitter	tCK_1UI_Tj_NoBUJ	-	0.090	-	0.090	-	0.090	-	0.090	UI	3, 6, 11
Rj RMS value of N-UI Jitter, where N=2,3,4,5	tCK_NUI_Rj_NoBUJ, where N=2,3,4,5	-	0.0040	-	0.0040	-	0.0040	-	0.0040	UI (RMS)	3, 7, 11
Dj pp value of N-UI Jitter, where N=2,3,4,5	tCK_NUI_Dj_NoBUJ, where N=2,3,4,5	-	0.074	-	0.074	-	0.074	-	0.074	UI	3, 7, 11
Tj value of N-UI Jitter, where N=2,3,4,5	tCK_NUI_Tj_NoBUJ, where N=2,3,4,5	-	0.140	-	0.140	-	0.140	-	0.140	UI	3, 8, 11
Rj RMS value of N-UI Jitter, where N=6,...,30	tCK_NUI_Rj_NoBUJ, where N=6,...,30	-	-	-	-	-	-	-	-	UI (RMS)	3, 9, 11, 12
Dj pp value of N-UI Jitter, N=6,...,30	tCK_NUI_Dj_NoBUJ, where N=6,...,30	-	-	-	-	-	-	-	-	UI	3, 10, 11, 12
Tj value of N-UI Jitter, N=6,...,30	tCK_NUI_Tj_NoBUJ, where N=6,...,30	-	-	-	-	-	-	-	-	UI	3, 10, 11, 12

NOTE 1 f0 = Data Rate/2, example: if data rate is 3200 MT/s, then f0=1600

NOTE 2 Rise and fall time slopes (V / nsec) are measured between +100 mV and -100 mV of the differential output of reference clock

NOTE 3 On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility

NOTE 4 Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.

NOTE 5 Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD

NOTE 6 Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD

NOTE 7 Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD

NOTE 8 Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD

NOTE 9 Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD

NOTE 10 Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD

NOTE 11 The validation methodology for these parameters will be covered in future ballots.

NOTE 12 If the clock meets total jitter Tj at BER of $1E^{-16}$, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of $1E^{-16}$

8.3.2 Specification for DRAM Input Clock Jitter (cont'd)

Table 209 — DRAM Input Clock Jitter Specifications for DDR5-6800 to 9200

[BUJ=Bounded Uncorrelated Jitter; DCD=Duty Cycle Distortion; Dj=Deterministic Jitter; Rj=Random Jitter; Tj=Total jitter; pp=Peak-to-Peak]

Parameter	Symbol	DDR5-6800		DDR5-7200		DDR5-7600-9200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
DRAM Reference clock frequency	tCK	0.9999* f0	1.0001* f0	0.9999* f0	1.0001* f0	0.9999* f0	1.0001* f0	MHz	1, 11
Duty Cycle Error	tCK_Duty_UI_Error	-	0.05	-	0.05	-	0.05	UI	1, 4, 11
Rj RMS value of 1-UI Jitter	tCK_1UI_Rj_NoBUJ	-	0.003145	-	0.003145	-	0.003145	UI (RMS)	3, 5, 11
Dj pp value of 1-UI Jitter	tCK_1UI_Dj_NoBUJ	-	0.0255	-	0.0255	-	0.0255	UI	3, 6, 11
Tj value of 1-UI Jitter	tCK_1UI_Tj_NoBUJ	-	0.0765	-	0.0765	-	0.0765	UI	3, 6, 11
Rj RMS value of N-UI Jitter, where N=2,3,4,5	tCK_NUI_Rj_NoBUJ, where N=2,3,4,5	-	0.0034	-	0.0034	-	0.0034	UI (RMS)	3, 7, 11
Dj pp value of N-UI Jitter, where N=2,3,4,5	tCK_NUI_Dj_NoBUJ, where N=2,3,4,5	-	0.0629	-	0.0629	-	0.0629	UI	3, 7, 11
Tj value of N-UI Jitter, where N=2,3,4,5	tCK_NUI_Tj_NoBUJ, where N=2,3,4,5	-	0.119	-	0.119	-	0.119	UI	3, 8, 11
Rj RMS value of N-UI Jitter, where N=6,...,30	tCK_NUI_Rj_NoBUJ, where N=6,...,30	-	-	-	-	-	-	UI (RMS)	3, 9, 11, 12
Dj pp value of N-UI Jitter, N=6,...,30	tCK_NUI_Dj_NoBUJ, where N=6,...,30	-	-	-	-	-	-	UI	3,1 0, 11, 12
Tj value of N-UI Jitter, N=6,...,30	tCK_NUI_Tj_NoBUJ, where N=6,...,30	-	-	-	-	-	-	UI	3, 10, 11, 12

NOTE 1 f0 = Data Rate/2, example: if data rate is 3200 MT/s, then f0=1600

NOTE 2 Rise and fall time slopes (V / nsec) are measured between +100 mV and -100 mV of the differential output of reference clock

NOTE 3 On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility

NOTE 4 Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.

NOTE 5 Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD

NOTE 6 Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD

NOTE 7 Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD

NOTE 8 Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD

NOTE 9 Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD

NOTE 10 Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD

NOTE 11 The validation methodology for these parameters will be covered in future ballots.

NOTE 12 If the clock meets total jitter Tj at BER of $1E^{-16}$, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of $1E^{-16}$

8.4 Differential Input Clock (CK_t, CK_c) Cross Point Voltage (VIX)

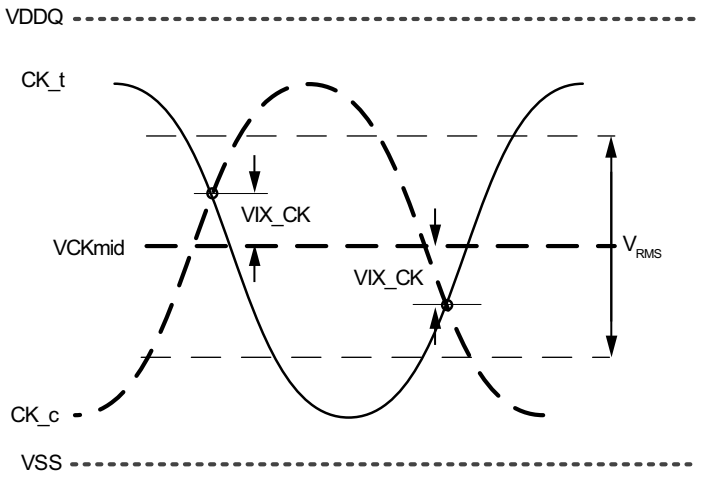


Figure 224 — VIX Definition (CK)

Table 210 — Crosspoint Voltage (VIX) for Differential Input Clock

Parameter	Symbol	DDR5-3200 - 9200		Unit	Notes
		Min	Max		
Clock differential input crosspoint voltage ratio	VIX_CK_Ratio	-	50	%	1, 2, 3

NOTE 1 The VIX_CK voltage is referenced to VCKmid(mean) = (CK_t voltage + CK_c voltage) /2, where the mean is over 8 UI

NOTE 2 VIX_CK_Ratio = (|VIX_CK| / |V_{RMS}|)*100%, where V_{RMS} = RMS(CK_t voltage - CK_c voltage)

NOTE 3 Only applies when both CK_t and CK_c are transitioning

8.5 Differential Input Clock Voltage Sensitivity

The differential input clock voltage sensitivity test provides the methodology for testing the receiver's sensitivity to clock by varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise. This specifies the Rx voltage sensitivity requirement. The system input swing to the DRAM must be larger than the DRAM Rx at the specified BER

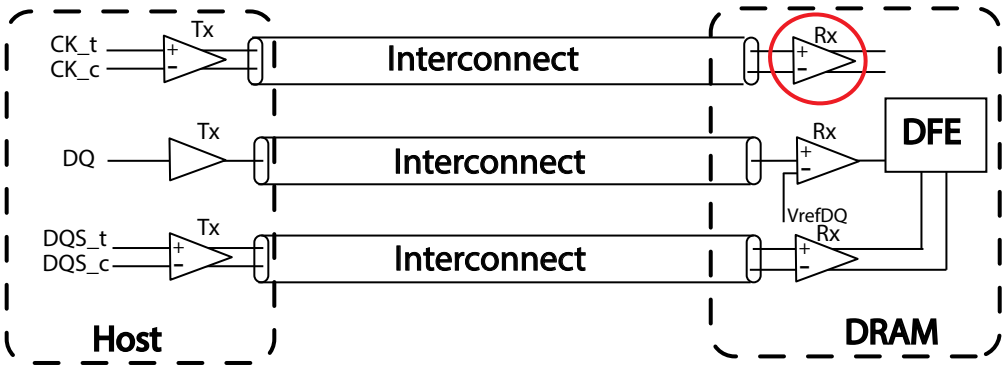


Figure 225 — Example of DDR5 Memory Interconnect

8.5.1 Differential Input Clock Voltage Sensitivity Parameter

Differential input clock (CK_t, CK_c) VRx_CK is defined and measured as shown in Table 211 through Table 213. The clock receiver must pass the minimum BER requirements for DDR5.

Table 211 — Differential Input Clock Voltage Sensitivity Parameter for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Input Clock Voltage Sensitivity (differential pp)	VRx_CK	-	200	-	200	-	180	-	180	-	160	mV	1, 2

NOTE 1 Refer to the minimum BER requirements for DDR5
NOTE 2 The validation methodology for this parameter will be covered in future ballot(s)

Table 212 — Differential Input Clock Voltage Sensitivity Parameter for DDR5-5200 to 6400

Parameter	Symbol	DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Input Clock Voltage Sensitivity (differential pp)	VRx_CK	-	140	-	120	-	100 (*120)	-	100 (*120)	mV	1, 2, 3

NOTE 1 Refer to the minimum BER requirements for DDR5
NOTE 2 The validation methodology for this parameter will be covered in future ballot(s)
NOTE 3 * indicates that it's supported if the CK buffer is present on the module.

Table 213 — Differential Input Clock Voltage Sensitivity Parameter for DDR5-6800 to 9200

Parameter	Symbol	DDR5-6800		DDR5-7200		DDR5-7600		DDR5-8000		DDR5-8400		DDR5-8800		DDR5-9200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Input Clock Voltage Sensitivity (differential pp)	VRx_CK	-	100 (*120)	-	100 (*120)	-	100 (*120)	-	100 (*120)	-	100 (*120)	-	100 (*120)	-	100 (*120)	mV	1, 2

NOTE 1 Refer to the minimum BER requirements for DDR5
NOTE 2 The validation methodology for this parameter will be covered in future ballot(s)
NOTE 3 * indicates that it's supported if the CK buffer is present on the module.

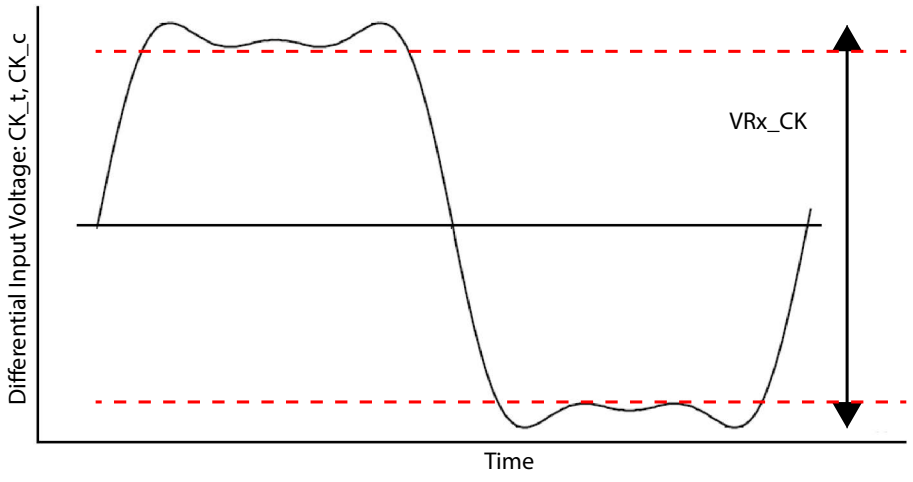


Figure 226 — VRx_CK

8.5.2 Differential Input Voltage Levels for Clock

Table 214 — Differential Clock (CK_t, CK_c) Input Levels for DDR5-3200 to DDR5-6400

From	Parameter [3]	DDR5 3200-6400	Note
$V_{IHdiff}CK$	Differential input high measurement level (CK_t, CK_c)	0.75 x $V_{diffpk-pk}$	1, 2
$V_{ILdiff}CK$	Differential input low measurement level (CK_t, CK_c)	0.25 x $V_{diffpk-pk}$	1, 2

NOTE 1 $V_{diffpk-pk}$ defined in Figure 227
NOTE 2 $V_{diffpk-pk}$ is the mean high voltage minus the mean low voltage over 8UI samples
NOTE 3 All parameters are defined over the entire clock common mode range

Table 215 — Differential Clock (CK_t, CK_c) Input Levels for DDR5-6800 to DDR5-9200

From	Parameter [3]	DDR5 6800-9200	Note
$V_{IHdiff}CK$	Differential input high measurement level (CK_t, CK_c)	0.75 x $V_{diffpk-pk}$	1, 2
$V_{ILdiff}CK$	Differential input low measurement level (CK_t, CK_c)	0.25 x $V_{diffpk-pk}$	1, 2

NOTE 1 $V_{diffpk-pk}$ defined in Figure 227
NOTE 2 $V_{diffpk-pk}$ is the mean high voltage minus the mean low voltage over 8UI samples
NOTE 3 All parameters are defined over the entire clock common mode range

8.5.3 Differential Input Slew Rate Definition for Clock (CK_t, CK_c)

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Figure 227.

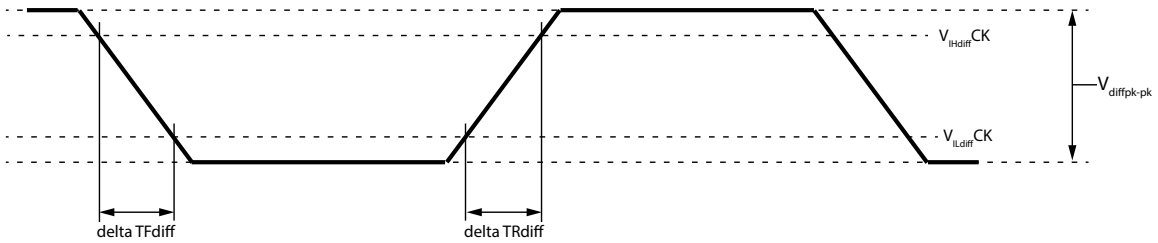


Figure 227 — Differential Input Slew Rate Definition for CK_t, CK_c

Table 216 — Differential Input Slew Rate Definition for CK_t, CK_c

Parameter	Measured		Defined by	Notes
	From	To		
Differential Input slew rate for rising edge (CK_t - CK_c)	$VIL_{diff}CK$	$VIH_{diff}CK$	($VIH_{diff}CK$ - $VIL_{diff}CK$) /deltaTRdiff	
Differential Input slew rate for falling edge (CK_t - CK_c)	$VIH_{diff}CK$	$VIL_{diff}CK$	($VIH_{diff}CK$ - $VIL_{diff}CK$) /deltaTFdiff	

8.5.3 Differential Input Slew Rate Definition for Clock (CK_t, CK_c) (cont'd)

Table 217 — Differential Input Slew Rate for CK_t, CK_c for DDR5-3200 to DDR5-4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate for CK_t, CK_c	SRIdiff_CK	2	14	2	14	2	14	2	14	2	14	V/ns	

Table 218 — Differential Input Slew Rate for CK_t, CK_c for DDR5-5200 to DDR5-6400

Parameter	Symbol	DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate for CK_t, CK_c	SRIdiff_CK	2	30	2	30	2	30	2	30	V/ns	

Table 219 — Differential Input Slew Rate for CK_t, CK_c for DDR5-6800 to DDR5-9200

Parameter	Symbol	DDR5-6800		DDR5-7200		DDR5-7600		DDR5-8000		DDR5-8400		DDR5-8800		DDR5-9200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate for CK_t, CK_c	SRIdiff_CK	2	30	2	30	2	30	2	30	2	30	2	30	2	30	V/ns	

8.6 Rx DQS Jitter Sensitivity

The receiver DQS jitter sensitivity test provides the methodology for testing the receiver's strobe sensitivity to an applied duty cycle distortion (DCD) and/or random jitter (Rj) at the forwarded strobe input without adding jitter, noise and ISI to the data. The receiver must pass the appropriate BER rate when no cross-talk nor ISI is applied, and must pass through the combination of applied DCD and Rj.

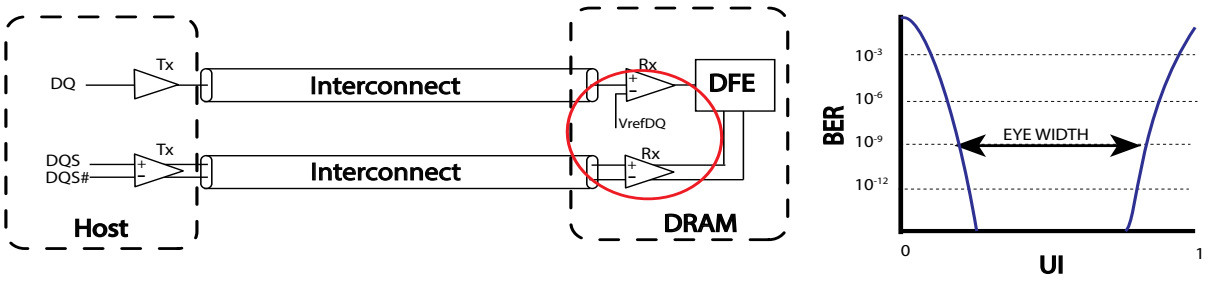


Figure 228 — SDRAM's Rx Forwarded Strobes for Jitter Sensitivity Testing

8.6.1 Rx DQS Jitter Sensitivity Specification

Table 220 provides Rx DQS Jitter Sensitivity Specification for the DDR5 DRAM receivers when operating at various possible transfer rates. These parameters are tested on the CTC2 card without Rx Equalization set. Additive DFE Gain Bias can be set.

Table 220 — Rx DQS Jitter Sensitivity Specification for DDR5-3200 to 4800

[BER = Bit Error Rate; DCD = Duty Cycle Distortion; Rj =Random Jitter]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQ Timing Width	tRx_DQ_tMargin	0.900	-	0.875	-	0.825	-	0.825	-	0.825	-	UI	1, 2, 3, 8, 9, 10
Degradation of timing width compared to tRx_DQ_tMargin, with DCD injection in DQS	ΔtRx_DQ_tMargin_DQS_DCD	-	0.06	-	0.06	-	0.06	-	0.06	-	0.06	UI	1, 4, 8, 9, 10
Degradation of timing width compared to tRx_DQ _tMargin, with Rj injection in DQS	ΔtRx_DQ_tMargin_DQS_Rj	-	0.09	-	0.09	-	0.09	-	0.09	-	0.09	UI	1, 5, 8, 9, 10
Degradation of timing width compared to tRx_DQ_tMargin, with both DCD and Rj injection in DQS	ΔtRx_DQ_tMargin_DQS_DCD_Rj	-	0.15	-	0.15	-	0.15	-	0.15	-	0.15	UI	1, 2, 6, 8, 9, 10
Delay of any data lane relative to the DQS_t/DQS_c crossing	tRx_DQS2DQ	114	937	114	833	114	750	114	738	114	729	ps	1, 7, 8, 9, 10
Delay of any data lane relative to any other data lane	tRX_DQ2DQ	-	50	-	50	-	50	-	50	-	50	ps	1, 7, 8, 9, 10, 11, 12

NOTE 1 Validation methodology will be defined in future ballots. 2UI is defined as 1tCK for this parameter

NOTE 2 Each of ΔtRx_DQ_tMargin_DQS_DCD, ΔtRx_DQ_tMargin_DQS_Rj, and ΔtRx_DQ_tMargin_DQS _DCD_Rj can be relaxed by up to 5% if tRx_DQ_tMargin exceeds the spec by 5% or more

NOTE 3 DQ Timing Width - timing width for any data lane using repetitive patterns (check note 4 for the pattern) measured at BER=E-9

NOTE 4 Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe DQS compared to tRx_DQ_tMargin, measured at BER=E-9. The magnitude of DCD is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 “1s” and 3 “0s”

NOTE 5 Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitude of Rj is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing.

NOTE 6 Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitudes of DCD and Rj are specified under Test Conditions for Rx DQS Jitter Sensitivity Testing.

NOTE 7 Delay of any data lane relative to the strobe lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.

NOTE 8 All measurements at BER=E-9

NOTE 9 This test should be done after the DQS and DQ Voltage Sensitivity tests are completed and passing

NOTE 10 The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

NOTE 11 DQ to DQ offset is skew between DQs within a nibble (x4) or a byte (x8, x16) at the DDR5 SDRAM balls.

NOTE 12 This parameter is relative to the per-pin trained DQS2DQ value, and only applies after per-pin DQS2DQ training is complete.

8.6.1 Rx DQS Jitter Sensitivity Specification (cont'd)

Table 221 — Rx DQS Jitter Sensitivity Specification for DDR5-5200 to 6400

[BER = Bit Error Rate; DCD = Duty Cycle Distortion; Rj =Random Jitter]

Parameter	Symbol	DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
DQ Timing Width	tRx_DQ_tMargin	0.835	-	0.835	-	0.845	-	0.845	-	UI	1, 2, 3, 8, 9, 10
Degradation of timing width compared to tRx_DQ_tMargin, with DCD injection in DQS	ΔtRx_DQ_tMargin_DQS_DCD	-	0.06	-	0.06	-	0.06	-	0.06	UI	1, 4, 8, 9, 10
Degradation of timing width compared to tRx_DQ _tMargin, with Rj injection in DQS	ΔtRx_DQ_tMargin_DQS_Rj	-	0.09	-	0.09	-	0.09	-	0.09	UI	1, 5, 8, 9, 10
Degradation of timing width compared to tRx_DQ_tMargin, with both DCD and Rj injection in DQS	ΔtRx_DQ_tMargin_DQS_DCD_Rj	-	0.15	-	0.15	-	0.15	-	0.15	UI	1, 2, 6, 8, 9, 10
Delay of any data lane relative to the DQS_t/DQS_c crossing	tRx_DQS2DQ	114	721	114	714	114	708	114	703	ps	1, 7, 8, 9, 10
Delay of any data lane relative to any other data lane	tRX_DQ2DQ	-	50	-	50	-	50	-	50	ps	1, 7, 8, 9, 10, 11, 12

NOTE 1 Validation methodology will be defined in future ballots. 2UI is defined as 1tCK for this parameter

NOTE 2 Each of ΔtRx_DQ_tMargin_DQS_DCD, ΔtRx_DQ_tMargin_DQS_Rj, and ΔtRx_DQ_tMargin_DQS _DCD_Rj can be relaxed by up to 5% if tRx_DQ_tMargin exceeds the spec by 5% or more

NOTE 3 DQ Timing Width - timing width for any data lane using repetitive patterns (check note 4 for the pattern) measured at BER=E-9

NOTE 4 Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe DQS compared to tRx_DQ_tMargin, measured at BER=E-9. The magnitude of DCD is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 "1s" and 3 "0s"

NOTE 5 Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitude of Rj is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing.

NOTE 6 Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitudes of DCD and Rj are specified under Test Conditions for Rx DQS Jitter Sensitivity Testing.

NOTE 7 Delay of any data lane relative to the strobe lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.

NOTE 8 All measurements at BER=E-9

NOTE 9 This test should be done after the DQS and DQ Voltage Sensitivity tests are completed and passing

NOTE 10 The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

NOTE 11 DQ to DQ offset is skew between DQs within a nibble (x4) or a byte (x8, x16) at the DDR5 SDRAM balls.

NOTE 12 This parameter is relative to the per-pin trained DQS2DQ value, and only applies after per-pin DQS2DQ training is complete.

8.6.1 Rx DQS Jitter Sensitivity Specification (cont'd)

Table 222 — Rx DQS Jitter Sensitivity Specification for DDR5-6800 to 9200

[BER = Bit Error Rate; DCD = Duty Cycle Distortion; Rj =Random Jitter]

Parameter	Symbol	DDR5-6800		DDR5-7200		DDR5-7600		DDR5-8000		DDR5-8400		DDR5-8800		DDR5-9200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQ Timing Width	tRx_DQ_tMargin	0.845	-	0.845	-	0.845	-	0.845	-	0.845	-	0.845	-	0.845	-	UI	1, 2, 3, 8, 9, 10
Degradation of timing width compared to tRx_DQ_tMargin, with DCD injection in DQS	ΔtRx_DQ_tMargin_DQS_DCD	-	0.06	-	0.06	-	0.06	-	0.06	-	0.06	-	0.06	-	0.06	UI	1, 4, 8, 9, 10
Degradation of timing width compared to tRx_DQ _tMargin, with Rj injection in DQS	ΔtRx_DQ_tMargin_DQS_Rj	-	0.09	-	0.09	-	0.09	-	0.09	-	0.09	-	0.09	-	0.09	UI	1, 5, 8, 9, 10
Degradation of timing width compared to tRx_DQ_tMargin, with both DCD and Rj injection in DQS	ΔtRx_DQ_tMargin_DQS_DCD_Rj	-	0.15	-	0.15	-	0.15	-	0.15	-	0.15	-	0.15	-	0.15	UI	1, 2, 6, 8, 9, 10
Delay of any data lane relative to the DQS_t/DQS_c crossing	tRx_DQS2DQ	114	703	114	703	114	703	114	703	114	703	114	703	114	703	ps	1, 7, 8, 9, 10
Delay of any data lane relative to any other data lane	tRX_DQ2DQ	-	50	-	50	-	50	-	50	-	50	-	50	-	50	ps	1, 7, 8, 9, 10, 11, 12

NOTE 1 Validation methodology will be defined in future ballots. 2UI is defined as 1tCK for this parameter

NOTE 2 Each of ΔtRx_DQ_tMargin_DQS_DCD, ΔtRx_DQ_tMargin_DQS_Rj, and ΔtRx_DQ_tMargin_DQS _DCD_Rj can be relaxed by up to 5% if tRx_DQ_tMargin exceeds the spec by 5% or more

NOTE 3 DQ Timing Width - timing width for any data lane using repetitive patterns (check note 4 for the pattern) measured at BER=E-9

NOTE 4 Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe DQS compared to tRx_DQ_tMargin, measured at BER=E-9. The magnitude of DCD is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 "1s" and 3 "0s"

NOTE 5 Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitude of Rj is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing.

NOTE 6 Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitudes of DCD and Rj are specified under Test Conditions for Rx DQS Jitter Sensitivity Testing.

NOTE 7 Delay of any data lane relative to the strobe lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.

NOTE 8 All measurements at BER=E-9

NOTE 9 This test should be done after the DQS and DQ Voltage Sensitivity tests are completed and passing

NOTE 10 The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

NOTE 11 DQ to DQ offset is skew between DQs within a nibble (x4) or a byte (x8, x16) at the DDR5 SDRAM balls.

NOTE 12 This parameter is relative to the per-pin trained DQS2DQ value, and only applies after per-pin DQS2DQ training is complete.

8.6.2 Test Conditions for Rx DQS Jitter Sensitivity Tests

Table 223 lists the amount of Duty Cycle Distortion (DCD) and/or Random Jitter (Rj) that must be applied to the forwarded strobe when measuring the Rx DQS Jitter Sensitivity parameters specified in Table 220 and Table 221.

Table 223 — Test Conditions for Rx DQS Jitter Sensitivity Testing for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Applied DCD to the DQS	tRx_DQS_DCD	-	0.045	-	0.045	-	0.045	-	0.045	-	0.045	UI	1, 2, 3, 6, 7, 10
Applied Rj RMS to the DQS	tRx_DQS_Rj	-	0.0075	-	0.0075	-	0.0075	-	0.0075	-	0.0075	UI (RMS)	1, 2, 4, 6, 8, 10
Applied DCD and Rj RMS to the DQS	tRx_DQS_DCD_Rj	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	UI	1, 2, 5, 6, 7, 9, 10

NOTE 1 While imposing this spec, the strobe lane is stressed, but the data input is kept large amplitude and no jitter or ISI injection. The specified voltages are at the Rx input pin. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

NOTE 2 The jitter response of the forwarded strobe channel will depend on the input voltage, primarily due to bandwidth limitations of the clock receiver. For this revision, no separate specification of jitter as a function of input amplitude is specified, instead the response characterization done at the specified clock amplitude only. The specified voltages are at the Rx input pin

NOTE 3 Various DCD values should be tested, complying within the maximum limits

NOTE 4 Various Rj values should be tested, complying within the maximum limits

NOTE 5 Various combinations of DCD and Rj should be tested, complying within the maximum limits. The maximum timing margin degradation as a result of these injected jitter is specified in a separate table

NOTE 6 Although DDR5 has bursty traffic, current available BERTs that can be used for this test do not support burst traffic patterns. A continuous strobe and continuous DQ are used for this parameter. The clock like pattern repeating 3 “1s” and 3 “0s” is used for this test.

NOTE 7 Duty Cycle Distortion (in UI DCD) as applied to the input forwarded DQS from BERT (UI)

NOTE 8 RMS value of Rj (specified as Edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI)

NOTE 9 Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI)

NOTE 10 The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

8.6.2 Test Conditions for Rx DQS Jitter Sensitivity Tests (cont'd)

Table 224 — Test Conditions for Rx DQS Jitter Sensitivity Testing for DDR5-5200 to 6400

Parameter	Symbol	DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Applied DCD to the DQS	tRx_DQS_DCD	-	0.045	-	0.045	-	0.045	-	0.045	UI	1, 2, 3, 6, 7, 10
Applied Rj RMS to the DQS	tRx_DQS_Rj	-	0.0075	-	0.0075	-	0.0075	-	0.0075	UI (RMS)	1, 2, 4, 6, 8, 10
Applied DCD and Rj RMS to the DQS	tRx_DQS_DCD_Rj	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	UI	1, 2, 5, 6, 7, 9, 10

NOTE 1 While imposing this spec, the strobe lane is stressed, but the data input is kept large amplitude and no jitter or ISI injection. The specified voltages are at the Rx input pin. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

NOTE 2 The jitter response of the forwarded strobe channel will depend on the input voltage, primarily due to bandwidth limitations of the clock receiver. For this revision, no separate specification of jitter as a function of input amplitude is specified, instead the response characterization done at the specified clock amplitude only. The specified voltages are at the Rx input pin

NOTE 3 Various DCD values should be tested, complying within the maximum limits

NOTE 4 Various Rj values should be tested, complying within the maximum limits

NOTE 5 Various combinations of DCD and Rj should be tested, complying within the maximum limits. The maximum timing margin degradation as a result of these injected jitter is specified in a separate table

NOTE 6 Although DDR5 has bursty traffic, current available BERTs that can be used for this test do not support burst traffic patterns. A continuous strobe and continuous DQ are used for this parameter. The clock like pattern repeating 3 "1s" and 3 "0s" is used for this test.

NOTE 7 Duty Cycle Distortion (in UI DCD) as applied to the input forwarded DQS from BERT (UI)

NOTE 8 RMS value of Rj (specified as Edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI)

NOTE 9 Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI)

NOTE 10 The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

8.6.2 Test Conditions for Rx DQS Jitter Sensitivity Tests (cont'd)

Table 225 — Test Conditions for Rx DQS Jitter Sensitivity Testing for DDR5-6800 to 9200

Parameter	Symbol	DDR5-6800		DDR5-7200		DDR5-7600		DDR5-8000		DDR5-8400		DDR5-8800		DDR5-9200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Applied DCD to the DQS	tRx_DQS_DCD	-	0.045	-	0.045	-	0.045	-	0.045	-	0.045	-	0.045	-	0.045	UI	3, 6, 7, 10
Applied Rj RMS to the DQS	tRx_DQS_Rj	-	0.0075	-	0.0075	-	0.0075	-	0.0075	-	0.0075	-	0.0075	-	0.0075	UI (RMS)	4, 6, 8, 10
Applied DCD and Rj RMS to the DQS	tRx_DQS_DCD_Rj	-	0.045 UI DCD + 0.0075 UI Rj RMS	-	0.045 UI DCD + 0.0075 UI Rj RMS	-	0.045 UI DCD + 0.0075 UI Rj RMS	-	0.045 UI DCD + 0.0075 UI Rj RMS	-	0.045 UI DCD + 0.0075 UI Rj RMS	-	0.045 UI DCD + 0.0075 UI Rj RMS	-	0.045 UI DCD + 0.0075 UI Rj RMS	UI	5, 6, 7, 9, 10

NOTE 1 While imposing this spec, the strobe lane is stressed, but the data input is kept large amplitude and no jitter or ISI injection. The specified voltages are at the Rx input pin. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

NOTE 2 The jitter response of the forwarded strobe channel will depend on the input voltage, primarily due to bandwidth limitations of the clock receiver. For this revision, no separate specification of jitter as a function of input amplitude is specified, instead the response characterization done at the specified clock amplitude only. The specified voltages are at the Rx input pin

NOTE 3 Various DCD values should be tested, complying within the maximum limits

NOTE 4 Various Rj values should be tested, complying within the maximum limits

NOTE 5 Various combinations of DCD and Rj should be tested, complying within the maximum limits. The maximum timing margin degradation as a result of these injected jitter is specified in a separate table

NOTE 6 Although DDR5 has bursty traffic, current available BERTs that can be used for this test do not support burst traffic patterns. A continuous strobe and continuous DQ are used for this parameter. The clock like pattern repeating 3 "1s" and 3 "0s" is used for this test.

NOTE 7 Duty Cycle Distortion (in UI DCD) as applied to the input forwarded DQS from BERT (UI)

NOTE 8 RMS value of Rj (specified as Edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI)

NOTE 9 Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI)

NOTE 10 The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

8.7 Rx DQS Voltage Sensitivity

8.7.1 Overview

The receiver DQS (strobe) input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

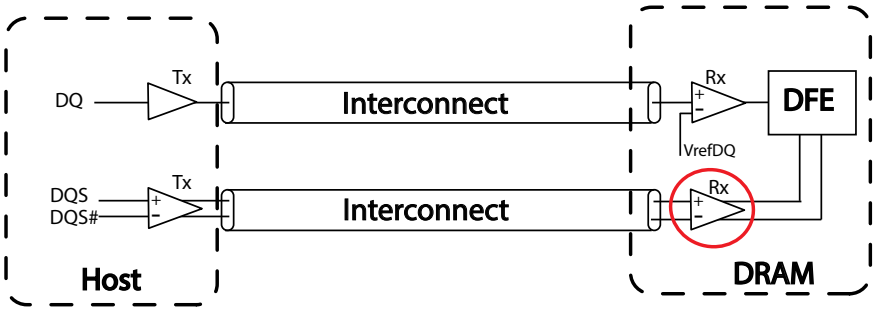


Figure 229 — Example of DDR5 Memory Interconnect

8.7.2 Receiver DQS Voltage Sensitivity Parameter

Input differential (DQS_t, DQS_c) VRx_DQS is defined and measured as shown in Table 226 through Table 228. The receiver must pass the minimum BER requirements for DDR5. These parameters are tested on the CTC2 card with neither additive gain nor Rx Equalization set.

Table 226 — Rx DQS Input Voltage Sensitivity Parameter for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS Rx Input Voltage Sensitivity (differential pp)	VRx_DQS	-	130	-	115	-	105	-	100	-	100	mV	1, 2, 3
NOTE 1 Refer to the minimum BER requirements for DDR5 NOTE 2 The validation methodology for this parameter will be covered in future ballot(s) NOTE 3 Test using clock like pattern of repeating 3 “1s” and 3 “0s”													

Table 227 — Rx DQS Input Voltage Sensitivity Parameter for DDR5-5200 to 6400

Parameter	Symbol	DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		DDR5-6800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS Rx Input Voltage Sensitivity (differential pp)	VRx_DQS	-	90	-	90	-	83	-	83	-	80	mV	1, 2, 3
NOTE 1 Refer to the minimum BER requirements for DDR5 NOTE 2 The validation methodology for this parameter will be covered in future ballot(s) NOTE 3 Test using clock like pattern of repeating 3 “1s” and 3 “0s”													

Table 228 — Rx DQS Input Voltage Sensitivity Parameter for DDR5-6800 to 9200

Parameter	Symbol	DDR5-7200		DDR5-7600		DDR5-8000		DDR5-8400		DDR5-8800		DDR5-9200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS Rx Input Voltage Sensitivity (differential pp)	VRx_DQS	-	80	-	77.5	-	77.5	-	75	-	75	-	73.5	mV	1, 2, 3
NOTE 1 Refer to the minimum BER requirements for DDR5 NOTE 2 The validation methodology for this parameter will be covered in future ballot(s) NOTE 3 Test using clock like pattern of repeating 3 “1s” and 3 “0s”															

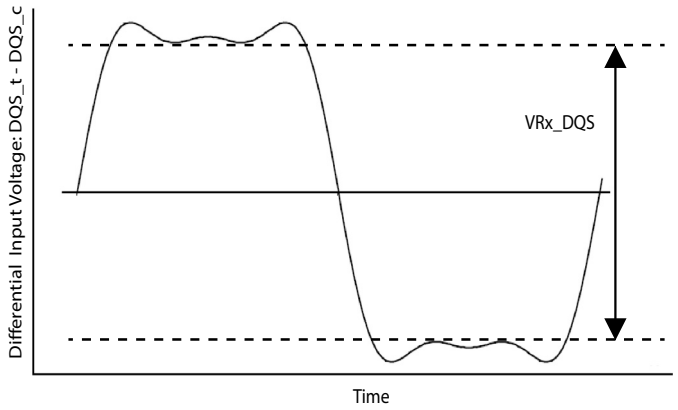


Figure 230 — VRx_DQS

8.8 Differential Strobe (DQS_t, DQS_c) Input Cross Point Voltage (VIX)

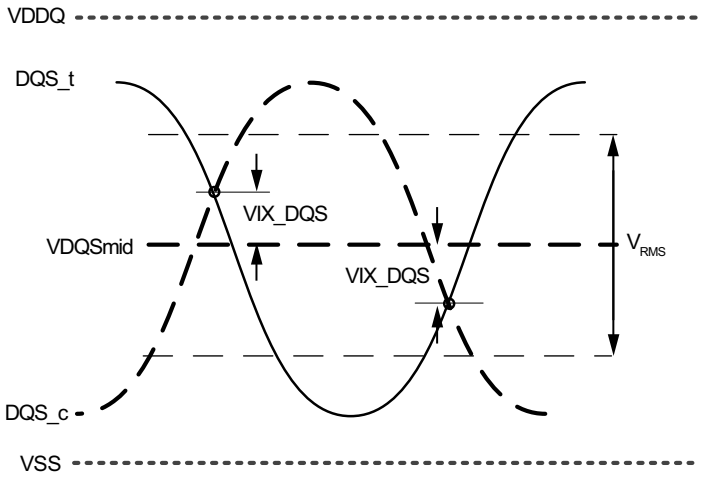


Figure 231 — VIX Definition (DQS)

Table 229 — Crosspoint Voltage (VIX) for DQS Differential Input Signals

Parameter	Symbol	DDR5-3200 - 9200		Unit	Notes
		Min	Max		
DQS differential input crosspoint voltage ratio	VIX_DQS_Ratio	-	50	%	1, 2, 3

NOTE 1 The VIX_DQS voltage is referenced to VDQSmid(mean) = (DQS_t voltage + DQS_c voltage) /2, where the mean is over 8 UI

NOTE 2 VIX_DQS_Ratio = (|VIX_DQS| / $|V_{RMS}|$)*100%, where V_{RMS} = RMS(DQS_t voltage - DQS_c voltage)

NOTE 3 Only applies when both DQS_t and DQS_c are transitioning (including preamble)

8.9 Rx DQ Voltage Sensitivity

8.9.1 Overview

The receiver data input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

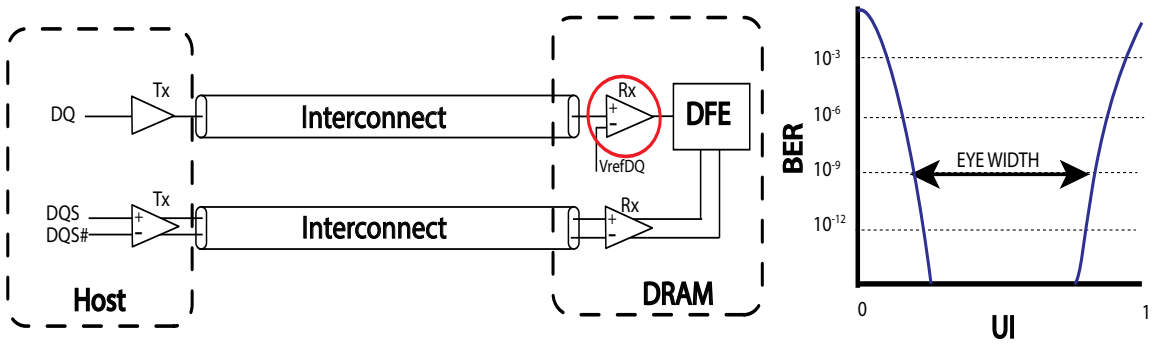


Figure 232 — Example of DDR5 Memory Interconnect

8.9.2 Receiver DQ Input Voltage Sensitivity Parameters

Input single-ended VRx_DQ is defined and measured as shown below. The receiver must pass the minimum BER requirements for DDR5. These parameters are tested on the CTC2 card with neither additive gain nor Rx Equalization set.

Table 230 — Rx DQ Input Voltage Sensitivity Parameters for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Minimum DQ Rx input voltage sensitivity applied around Vref	VRx_DQ	-	85	-	75	-	70	-	65	-	65	mV	1, 2, 3

NOTE 1 Refer to the minimum BER requirements for DDR5
NOTE 2 The validation methodology for this parameter will be covered in future ballot(s)
NOTE 3 Test using clock like pattern of repeating 3 “1s” and 3 “0s”

Table 231 — Rx DQ Input Voltage Sensitivity Parameters for DDR5-5200 to 6400

Parameter	Symbol	DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		DDR5-6800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Minimum DQ Rx input voltage sensitivity applied around Vref	VRx_DQ	-	60	-	60	-	55	-	55	-	50	mV	1, 2, 3

NOTE 1 Refer to the minimum BER requirements for DDR5
NOTE 2 The validation methodology for this parameter will be covered in future ballot(s)
NOTE 3 Test using clock like pattern of repeating 3 “1s” and 3 “0s”

Table 232 — Rx DQ Input Voltage Sensitivity Parameters for DDR5-6800 to 9200

Parameter	Symbol	DDR5-7200		DDR5-7600		DDR5-8000		DDR5-8400		DDR5-8800		DDR5-9200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Minimum DQ Rx input voltage sensitivity applied around Vref	VRx_DQ	-	50	-	50	-	50	-	47.5	-	47.5	-	46.5	mV	1, 2, 3

NOTE 1 Refer to the minimum BER requirements for DDR5
NOTE 2 The validation methodology for this parameter will be covered in future ballot(s)
NOTE 3 Test using clock like pattern of repeating 3 “1s” and 3 “0s”

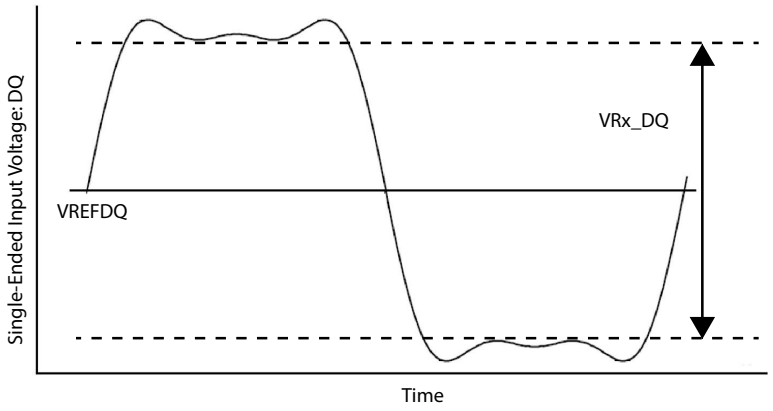


Figure 233 — VRx_DQ

8.9.3 Differential Input Levels for DQS

Table 233 — Differential Input Levels for DQS (DQS_t, DQS_c) for DDR5-3200 to DDR5-6400

From	Parameter	DDR5 3200-6400	Note
$V_{IHdiff}DQS$	Differential input high measurement level (DQS_t, DQS_c)	0.75 x $V_{diffpk-pk}$	1, 2, 3
$V_{ILdiff}DQS$	Differential input low measurement level (DQS_t, DQS_c)	0.25 x $V_{diffpk-pk}$	1, 2, 3

NOTE 1 $V_{diffpk-pk}$ defined in Figure 234
NOTE 2 $V_{diffpk-pk}$ is the mean high voltage minus the mean low voltage over 8UI samples
NOTE 3 All parameters are defined over the entire clock common mode range

Table 234 — Differential Input Levels for DQS (DQS_t, DQS_c) for DDR5-6800 to DDR5-9200

From	Parameter	DDR5 6800-9200	Note
$V_{IHdiff}DQS$	Differential input high measurement level (DQS_t, DQS_c)	0.75 x $V_{diffpk-pk}$	1, 2, 3
$V_{ILdiff}DQS$	Differential input low measurement level (DQS_t, DQS_c)	0.25 x $V_{diffpk-pk}$	1, 2, 3

NOTE 1 $V_{diffpk-pk}$ defined in Figure 234
NOTE 2 $V_{diffpk-pk}$ is the mean high voltage minus the mean low voltage over 8UI samples
NOTE 3 All parameters are defined over the entire clock common mode range

8.9.4 Differential Input Slew Rate for DQS_t, DQS_c

Input slew rate for differential signals are defined and measured as shown in Figure 234.

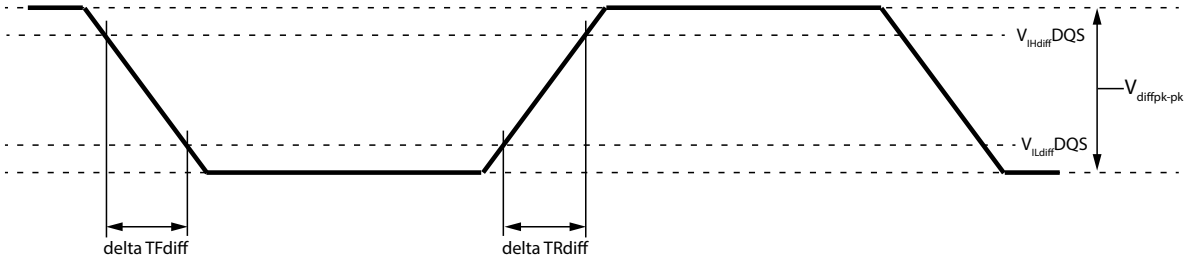


Figure 234 — Differential Input Slew Rate Definition for DQS_t, DQS_c

Table 235 — Differential Input Slew Rate Definition for DQS_t, DQS_c

Parameter	Measured		Defined by	Notes
	From	To		
Differential Input slew rate for rising edge (DQS_t, DQS_c)	$V_{ILdiff}DQS$	$V_{IHdiff}DQS$	($V_{IHdiff}DQS$ - $V_{ILdiff}DQS$) /deltaTRdiff	1, 2, 3
Differential Input slew rate for falling edge (DQS_t, DQS_c)	$V_{IHdiff}DQS$	$V_{ILdiff}DQS$	($V_{IHdiff}DQS$ - $V_{ILdiff}DQS$) /deltaTFdiff	1, 2, 3

8.9.4 Differential Input Slew Rate for DQS_t, DQS_c (cont'd)

Table 236 — Differential Input Slew Rate for DQS_t, DQS_c for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate for DQS_t, DQS_c	SRIdiff_DQS	1.5	30	1.5	30	1.5	30	1.5	30	1.5	30	V/ns	1
NOTE 1 Only applies when both DQS_t and DQS_c are transitioning.													

Table 237 — Differential Input Slew Rate for DQS_t, DQS_c for DDR5-5200 to 6400

Parameter	Symbol	DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate for DQS_t, DQS_c	SRIdiff_DQS	2.0	30	2.0	30	2.0	30	2.0	30	V/ns	1
NOTE 1 Only applies when both DQS_t and DQS_c are transitioning.											

Table 238 — Differential Input Slew Rate for DQS_t, DQS_c for DDR5-6800 to 9200

Parameter	Symbol	DDR5-6800		DDR5-7200		DDR5-7600		DDR5-8000		DDR5-8400		DDR5-8800		DDR5-9200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate for DQS_t, DQS_c	SRIdiff_DQS	2.0	30	2.0	30	2.0	30	2.0	30	2.0	30	2.0	30	2.0	30	V/ns	1
NOTE 1 Only applies when both DQS_t and DQS_c are transitioning.																	

8.10 Rx Stressed Eye

The stressed eye tests provide the methodology for creating the appropriate stress for the DRAM's receiver with the combination of ISI (both loss and reflective), jitter (Rj, Dj, DCD), and crosstalk noise. The receiver must pass the appropriate BER rate when the equivalent stressed eye is applied through the combination of ISI, jitter and crosstalk.

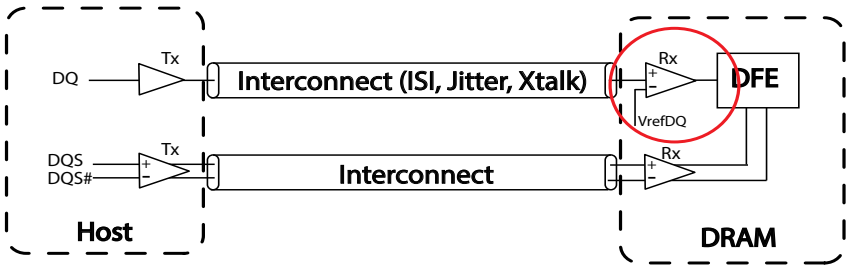


Figure 235 — Example of Rx Stressed Test Setup in the Presence of ISI, Jitter, and Crosstalk

8.10 Rx Stressed Eye (cont'd)

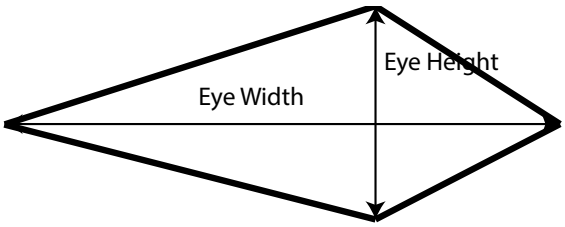


Figure 236 — Example of Rx Stressed Eye Height and Eye Width

8.10.1 Parameters for DDR5 Rx Stressed Eye Tests

Table 239 — Test Conditions for Rx Stressed Eye Tests for DDR5-3200 to 4800

[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Eye height of stressed eye for Golden Reference Channel 1	RxEH_Stressed_Eye_ Golden_Ref_Channel_1	95	-	85	-	80	-	75	-	70	-	mV	1, 2, 3, 4, 5, 6, 7, 8, 9, 10
Eye width of stressed eye Golden Reference Channel 1	RxEW_Stressed_Eye_ Golden_Ref_Channel_1	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	UI	1, 2, 3, 4, 5, 6, 7, 8, 9, 10
Vswing stress to meet above data eye	Vswing_Stressed_Eye_ Golden_Ref_Channel_1	-	600	-	600	-	600	-	600	-	600	mV	1. 2
Injected sinusoidal jitter at 200 MHz to meet above data eye	Sj_Stressed_Eye_Golden _Ref_Channel_1	0	0.45	0	0.45	0	0.45	0	0.45	0	0.45	UI p-p	1, 2
Injected Random wide band (10 MHz-1 GHz) Jitter to meet above data eye	Rj_Stressed_Eye_Golden _Ref_Channel_1	0	0.04	0	0.04	0	0.04	0	0.04	0	0.04	UI RMS	1, 2
Injected voltage noise as PRBS23, or Injected voltage noise at 2.1 GHz	Vnoise_Stressed_Eye_ Golden_Ref_Channel_1	0	125	0	125	0	125	0	125	0	125	mV p-p	1, 2
Golden Reference Channel 1 Characteristics as measured at TBD	Golden_Ref_Channel_1_ Characteristics	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	dB	3

NOTE 1 Must meet minimum BER of $1E^{-16}$ or better requirement with the stressed eye at the slice of the receiver (after equalization is applied in the summer). The eye shape is verified by measuring to BER E^{-9} and extrapolating to BER E^{-16}.

NOTE 2 These parameters are applied on the defined golden reference channel with parameters TBD.

NOTE 3 DFE Tap 1-4 Bias settings that give the best eye margin are used and referring to Table 132, Min/Max Ranges for the DFE Tap Coefficients. DFE tap range limits apply: sum of absolute values of Tap-2, Tap-3, and Tap-4 shall be less than 60 mV (|Tap-2| + |Tap-3| + |Tap-4| < 60 mV) after the tap multiflier is applied.

NOTE 4 Evaluated with no DC supply voltage drift.

NOTE 5 Evaluated with no temperature drift.

NOTE 6 Supply voltage noise limited according to DC bandwidth spec, see DC Operating Conditions

NOTE 7 The stressed eye is to be assumed to have a diamond shape

NOTE 8 The VREFDQ, DFE Gain Bias Step, and DFE Taps 1,2,3,4 Bias Step can be adjusted as needed, without exceeding the specifications, for this test, including the limits placed in Note 3.

NOTE 9 The stressed eye is defined as centered on the DQS_t/DQS_c crossing during the calibration. Measurement includes an optimal set of DQS_t/DQS_c location, VrefDQ, and DFE solution to give the best eye margin.

NOTE 10 The Rx stressed eye spec applies at 2933 MT/s and faster data rates.

NOTE 11 EH/EW are measured at the slicer of the receiver

LIGHT GREY - All Light Grey text is defined as something that should be considered TBD. The content may be accurate or the same as previous technologies but has not yet been reviewed or determined to be the working assumption.

8.10.1 Parameters for DDR5 Rx Stressed Eye Tests (cont'd)

Table 240 — Test Conditions for Rx Stressed Eye Tests for DDR5-5200 to 6400

[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Parameter	Symbol	DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Eye height of stressed eye for Golden Reference Channel 1	RxEH_Stressed_Eye_ Golden_Ref_Channel_1	65	-	60	-	57.5	-	57.5	-	mV	1, 2, 3, 4, 5, 6, 7, 8, 9, 10
Eye width of stressed eye Golden Reference Channel 1	RxEW_Stressed_Eye_ Golden_Ref_Channel_1	0.235	-	0.235	-	0.230	-	0.230	-	UI	1, 2, 3, 4, 5, 6, 7, 8, 9, 10
Vswing stress to meet above data eye	Vswing_Stressed_Eye_ Golden_Ref_Channel_1	-	600	-	600	-	600	-	600	mV	1, 2
Injected sinusoidal jitter at 200 MHz to meet above data eye	Sj_Stressed_Eye_Golden _Ref_Channel_1	-	0.45	-	0.45	-	0.45	-	0.45	UI p-p	1, 2
Injected Random wide band (10 MHz-1 GHz) Jitter to meet above data eye	Rj_Stressed_Eye_Golden _Ref_Channel_1	0	0.04	0	0.04	0	0.04	0	0.04	UI RMS	1, 2
Injected voltage noise as PRBS23, or Injected voltage noise at 2.1 GHz	Vnoise_Stressed_Eye_ Golden_Ref_Channel_1	0	125	0	125	0	125	0	125	mV p-p	1, 2
Golden Reference Channel 1 Characteristics as measured at TBD	Golden_Ref_Channel_1_ Characteristics	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	dB	3

NOTE 1 Must meet minimum BER of $1E^{-16}$ or better requirement with the stressed eye at the slice of the receiver (after equalization is applied in the summer). The eye shape is verified by measuring to BER E^{-9} and extrapolating to BER E^{-16}.

NOTE 2 These parameters are applied on the defined golden reference channel with parameters TBD.

NOTE 3 DFE tap range limits apply: sum of absolute values of Tap-2, Tap-3, and Tap-4 shall be less than 6 0mV (|Tap-2| + |Tap-3| + |Tap-4| < 60 mV).

NOTE 4 Evaluated with no DC supply voltage drift.

NOTE 5 Evaluated with no temperature drift.

NOTE 6 Supply voltage noise limited according to DC bandwidth spec, see DC Operating Conditions

NOTE 7 The stressed eye is to be assumed to have a diamond shape

NOTE 8 The VREFDQ, DFE Gain Bias Step, and DFE Taps 1,2,3,4 Bias Step can be adjusted as needed, without exceeding the specifications, for this test, including the limits placed in Note 3.

NOTE 9 The stressed eye is defined as centered on the DQS_t/DQS_c crossing during the calibration. Measurement includes an optimal set of DQS_t/DQS_c location, VrefDQ, and DFE solution to give the best eye margin.

NOTE 10 EH/EW are measured at the slicer of the receiver.

8.10.1 Parameters for DDR5 Rx Stressed Eye Tests (cont'd)

Table 241 — Test Conditions for Rx Stressed Eye Tests for DDR5-6800 to 9200

[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Parameter	Symbol	DDR5-6800		DDR5-7200		DDR5-7600		DDR5-8000		DDR5-8400		DDR-8800		DDR-9200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Eye height of stressed eye for Golden Reference Channel 1	RxEH_Stressed_Eye_Golden_Ref_Channel_1	55	-	55	-	54	-	54	-	53	-	53	-	52.5	-	mV	1, 2, 3, 4, 5, 6, 7, 8, 9
Eye width of stressed eye Golden Reference Channel 1	RxEW_Stressed_Eye_Golden_Ref_Channel_1	0.230	-	0.230	-	0.230	-	0.230	-	0.230	-	0.230	-	0.230	-	UI	1, 2, 3, 4, 5, 6, 7, 8, 9
Vswing stress to meet above data eye	Vswing_Stressed_Eye_Golden_Ref_Channel_1	-	600	-	600	-	600	-	600	-	600	-	600	-	600	mV	1, 2
Injected sinusoidal jitter at 200 MHz to meet above data eye	Sj_Stressed_Eye_Golden_Ref_Channel_1	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	UI p-p	1, 2
Injected Random wide band (10 MHz-1 GHz) Jitter to meet above data eye	Rj_Stressed_Eye_Golden_Ref_Channel_1	0	0.04	0	0.04	0	0.04	0	0.04	-	0.04	-	0.04	0	0.04	UI RMS	1, 2
Injected voltage noise as PRBS23, or Injected voltage noise at 2.1 GHz	Vnoise_Stressed_Eye_Golden_Ref_Channel_1	0	125	0	125	0	125	0	125	-	125	-	125	0	125	mV p-p	1, 2
Golden Reference Channel 1 Characteristics as measured at TBD	Golden_Ref_Channel_1_Characteristics	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	dB	3

NOTE 1 Must meet minimum BER of $1E^{-16}$ or better requirement with the stressed eye at the slice of the receiver (after equalization is applied in the summer). The eye shape is verified by measuring to BER E^{-9} and extrapolating to BER E^{-16}.

NOTE 2 These parameters are applied on the defined golden reference channel with parameters TBD.

NOTE 3 DFE tap range limits apply: sum of absolute values of Tap-2, Tap-3, and Tap-4 shall be less than 60mV (|Tap-2| + |Tap-3| + |Tap-4| < 60 mV).

NOTE 4 Evaluated with no DC supply voltage drift.

NOTE 5 Evaluated with no temperature drift.

NOTE 6 Supply voltage noise limited according to DC bandwidth spec, see DC Operating Conditions.

NOTE 7 The stressed eye is to be assumed to have a diamond shape

NOTE 8 The VREFDQ, DFE Gain Bias Step, and DFE Taps 1,2,3,4 Bias Step can be adjusted as needed, without exceeding the specifications, for this test, including the limits placed in Note 3.

NOTE 9 The stressed eye is defined as centered on the DQS_t/DQS_c crossing during the calibration. Measurement includes an optimal set of DQS_t/DQS_c location, VrefDQ, and DFE solution to give the best eye margin.

NOTE 10 EH/EW are measured at the slicer of the receiver.

8.11 Connectivity Test Mode - Input level and Timing Requirement

During CT Mode, input levels are defined below.

TEN pin: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ
CS_n: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.
Test Input pins: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.
RESET_n: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.

Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable.

Upon the assertion of the TEN pin, the CK_t and CK_c signals will be ignored and the DDR5 memory device will enter into the CT mode after time tCT_Enable. In the CT mode, no refresh activities in the memory arrays, initiated either externally (i.e., auto-refresh) or internally (i.e., self-refresh), will be maintained.

8.11.1 Connectivity Test Mode - Input level and Timing Requirement (cont'd)

The TEN pin may be asserted after the DRAM has completed power-on, after RESET_n has de-asserted, the wait time after the RESET_n de-assertion has elapsed, and prior to starting clocks (CK_t, CK_c).

The TEN pin may be de-asserted at any time in the CT mode. Upon exiting the CT mode, the states of the DDR5 memory device are unknown and the integrity of the original content of the memory array is not guaranteed; therefore, the reset initialization sequence is required.

All output signals at the test output pins will be stable within tCT_valid after the test inputs have been applied to the test input pins with TEN input and CS_n input maintained High and Low, respectively.

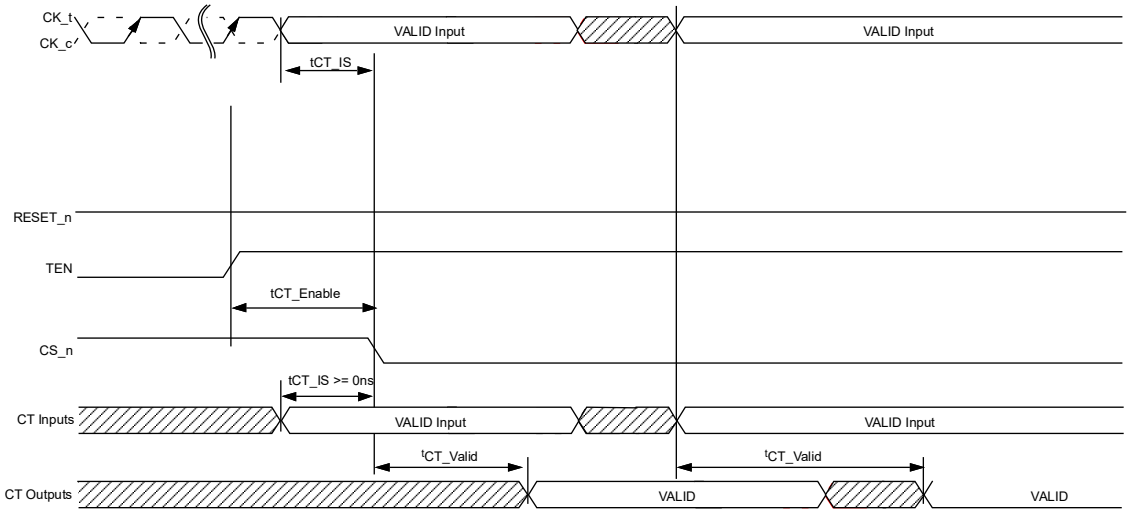


Figure 237 — Timing Diagram for Connectivity Test (CT) Mode

Table 242 — AC Parameters for Connectivity Test (CT) Mode

Symbol	Min	Max	Unit
tCT_IS	0	-	ns
tCT_Enable	200	-	ns
tCT_Valid	-	200	ns

8.11.1 Connectivity Test (CT) Mode Input Levels

Following input parameters will be applied for DDR5 SDRAM Input Signals during Connectivity Test Mode.

Table 243 — CMOS Rail to Rail Input Levels for TEN, CS_n, and Test inputs

Parameter	Symbol	Min	Max	Unit	Notes
TEN AC Input High Voltage	VIH(AC)_TEN	0.8 * VDDQ	VDDQ	V	1
TEN DC Input High Voltage	VIH(DC)_TEN	0.7 * VDDQ	VDDQ	V	
TEN DC Input Low Voltage	VIL(DC)_TEN	VSS	0.3 * VDDQ	V	
TEN AC Input Low Voltage	VIL(AC)_TEN	VSS	0.2 * VDDQ	V	2
TEN Input signal Falling time	TF_input_TEN	-	10	ns	
TEN Input signal Rising time	TR_input_TEN	-	10	ns	

NOTE 1 Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
NOTE 2 Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

8.11.1 Connectivity Test (CT) Mode Input Levels (cont'd)

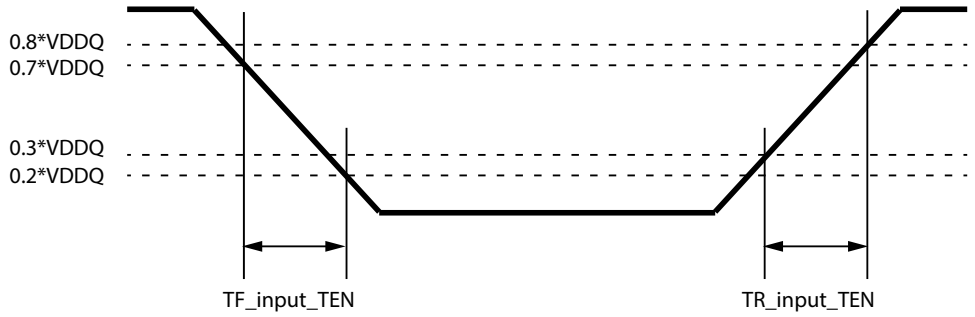


Figure 238 — TEN Input Slew Rate Definition

8.11.2 CMOS Rail to Rail Input Levels for RESET_n

Table 244 — CMOS Rail to Rail Input Levels for RESET_n

Parameter	Symbol	Min	Max	Unit	Note
AC Input High Voltage	VIH(AC)_RESET	0.8*VDDQ	VDDQ	V	5
DC Input High Voltage	VIH(DC)_RESET	0.7*VDDQ	VDDQ	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDDQ	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDDQ	V	6
Rising time	TR_RESET	-	1.0	µs	
RESET pulse width	tPW_RESET	1.0	-	µs	3, 4

NOTE 1 After RESET_n is registered LOW, RESET_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not be reset.
NOTE 2 Once RESET_n is registered HIGH, RESET_n level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET_n signal LOW.
NOTE 3 RESET is destructive to data contents.
NOTE 4 This definition is applied only for "Reset Procedure at Power Stable".
NOTE 5 Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
NOTE 6 Undershoot might occur. It should be limited by Absolute Maximum DC Ratings

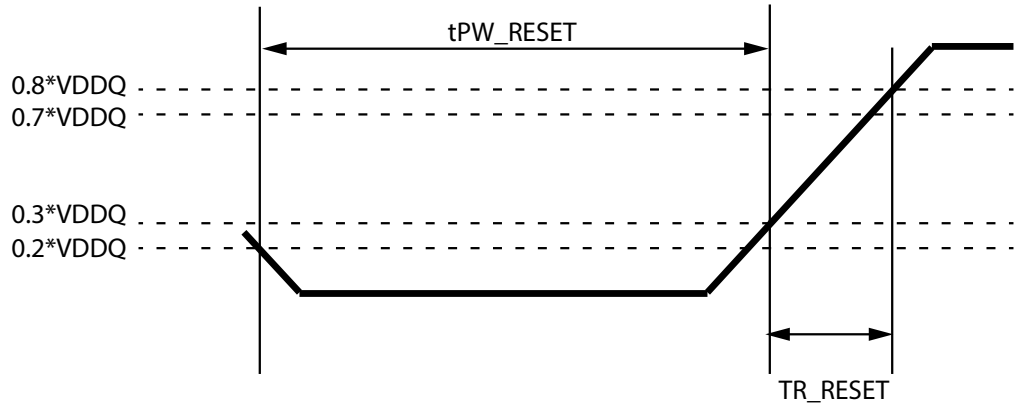


Figure 239 — RESET_n Input Slew Rate Definition

9 AC and DC Output Measurement Levels and Timing

9.1 Output Driver DC Electrical Characteristics for DQS and DQ

The DDR5 driver supports two different Ron values. These Ron values are referred as strong(low Ron) and weak mode(high Ron). A functional representation of the output buffer is shown in Figure 240.

Output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\,out|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|I\,out|}$$ under the condition that RON_{Pu} is off

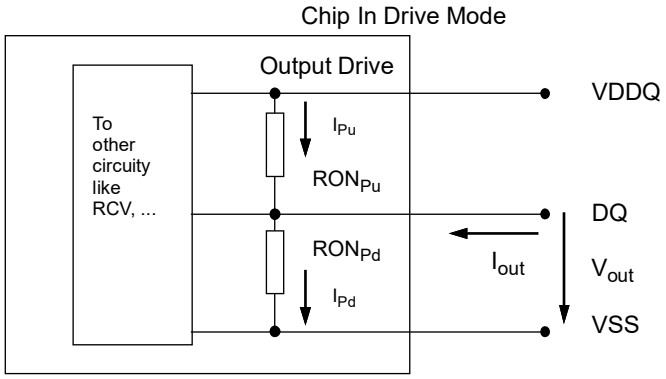


Figure 240 — Strong (Low Ron) and Weak Mode (High Ron) Output Buffer

9.1 Output Driver DC Electrical Characteristics for DQS and DQ (cont'd)

Table 245 — Output Driver DC Electrical Characteristics, Assuming RZQ = 240 Ohms; Entire Operating Temperature Range; after Proper ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.73	1	1.1	RZQ/7	1, 2
		VOMdc= 0.8* VDDQ	0.83	1	1.1	RZQ/7	1, 2
		VOHdc= 0.95* VDDQ	0.83	1	1.25	RZQ/7	1, 2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1, 2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1, 2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/7	1, 2
48Ω	RON48Pd	VOLdc= 0.5*VDDQ	0.73	1	1.1	RZQ/5	1, 2
		VOMdc= 0.8* VDDQ	0.83	1	1.1	RZQ/5	1, 2
		VOHdc= 0.95* VDDQ	0.83	1	1.25	RZQ/5	1, 2
	RON48Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1, 2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1, 2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/5	1, 2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10		10	%	1, 2, 3, 4
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOMdc= 0.8* VDDQ			10	%	1, 2, 4
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ			10	%	1, 2, 4

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see "ZQ Calibration Commands" section.

NOTE 2 Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 0.95 * VDDQ.

NOTE 3 Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately; Ronnom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

NOTE 4 RON variance range ratio to RON Nominal value in a given component, including DQS_t and DQS_c.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

NOTE 5 This parameter of x16 device is specified for Upper byte and Lower byte.

9.2 Output Driver DC Electrical Characteristics for Loopback Signals LBDQS, LBDQ

The DDR5 Loopback driver supports 34 ohms. A functional representation of the output buffer is shown in Figure 241.

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\ out|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|I\ out|}$$ under the condition that RON_{Pu} is off

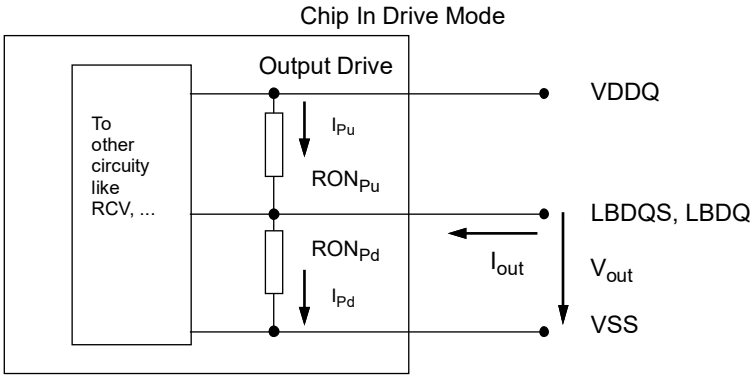


Figure 241 — Output Driver for Loopback Signals

Table 246 — Output Driver DC Electrical Characteristics, Assuming RZQ = 240 Ohms; Entire Operating Temperature Range; after Proper ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/7	1, 2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1, 2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/7	1, 2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1, 2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1, 2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/7	1, 2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10		10	%	1, 2, 3, 4
Mismatch LBDQS-LBDQ within device variation pull-up, MMPudd		VOMdc= 0.8* VDDQ			10	%	1, 2, 4
Mismatch LBDQS-LBDQ within device variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ			10	%	1, 2, 4

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see “ZQ Calibration Commands” section.

NOTE 2 Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 0.95 * VDDQ.

NOTE 3 Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately; Ronnom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

NOTE 4 RON variance range ratio to RON Nominal value in a given component, including LBDQS and LBDQ.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

9.3 Loopback Output Timing

Loopback strobe LBDQS to Loopback data LBDQ relationship is illustrated in Figure 242.

- tLBQSH describes the single-ended LBDQS strobe high pulse width
- tLBQSL describes the single-ended LBDQS strobe low pulse width
- tLBQ_Set describes the setup time of LBDQS and where LBDQ needs to remain stable
- tLBQ_Hld describes the hold time of LBDQS and where LBDQ needs to remain stable
- tLBDVW describes the data valid window per device per UI

Table 247 — Loopback Output Timing Parameters for DDR5-3200 to 4800

Speed		DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Loopback Timing													
Loopback LBDQS Output Low Time	tLBQSL	0.7	-	0.7	-	0.7	-	0.7	-	0.7	-	tCK	1
Loopback LBDQS Output High Time	tLBQSH	0.7	-	0.7	-	0.7	-	0.7	-	0.7	-	tCK	1
Loopback Setup time for LBDQS	tLBQ_Set	0.5		0.5		0.5		0.5		0.5		tCK	1, 2
Loopback Hold time for LBDQS	tLBQ_Hld	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	tCK	1, 2
Loopback Data valid window of each UI per DRAM	tLBDVW	1.6	-	1.6	-	1.6	-	1.6	-	1.6	-	tCK	1

NOTE 1 Based on Loopback 4-way interleave setting (see MR53)
NOTE 2 tLBQ_Set is measured from LBDQ first transition to LBDQS falling edge and tLBQ_Hld is measured from LBDQS falling edge to LBDQ last transition.

Table 248 — Loopback Output Timing Parameters for DDR5-5200 to 6400

Speed		DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Loopback Timing											
Loopback LBDQS Output Low Time	tLBQSL	0.7	-	0.7	-	0.75	-	0.75	-	tCK	1
Loopback LBDQS Output High Time	tLBQSH	0.7	-	0.7	-	0.75	-	0.75	-	tCK	1
Loopback Setup time for LBDQS	tLBQ_Set	0.5		0.5		0.5		0.5		tCK	1, 2
Loopback Hold time for LBDQS	tLBQ_Hld	0.5	-	0.5	-	0.5	-	0.5	-	tCK	1, 2
Loopback Data valid window of each UI per DRAM	tLBDVW	1.6	-	1.6	-	1.6	-	1.6	-	tCK	1

NOTE 1 Based on Loopback 4-way interleave setting (see MR53)
NOTE 2 tLBQ_Set is measured from LBDQ first transition to LBDQS falling edge and tLBQ_Hld is measured from LBDQS falling edge to LBDQ last transition.

Table 249 — Loopback Output Timing Parameters for DDR5-6800 to 8400

Speed		DDR5-6800		DDR5-7200		DDR5-7600		DDR5-8000		DDR5-8400		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Loopback Timing													
Loopback LBDQS Output Low Time	tLBQSL	0.75	-	0.75	-	0.75	-	0.75	-	0.75	-	tCK	1
Loopback LBDQS Output High Time	tLBQSH	0.75	-	0.75	-	0.75	-	0.75	-	0.75	-	tCK	1
Loopback Setup time for LBDQS	tLBQ_Set	0.55	-	0.55	-	0.55	-	0.55	-	0.55	-	tCK	1, 2
Loopback Hold time for LBDQS	tLBQ_Hld	0.55	-	0.55	-	0.55	-	0.55	-	0.55	-	tCK	1, 2
Loopback Data valid window of each UI per DRAM	tLBDVW	1.6	-	1.6	-	1.6	-	1.6	-	1.6	-	tCK	1

NOTE 1 Based on Loopback 4-way interleave setting (see MR53)
NOTE 2 tLBQ_Set is measured from LBDQ first transition to LBDQS falling edge and tLBQ_Hld is measured from LBDQS falling edge to LBDQ last transition.

9.3 Loopback Output Timing (cont'd)

Table 250 — Loopback Output Timing Parameters for DDR5-9200

Speed		DDR5-8800		DDR5-9200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX		
Loopback Timing							
Loopback LBDQS Output Low Time	tLBQSL	0.75	-	0.75	-	tCK	1
Loopback LBDQS Output High Time	tLBQSH	0.75	-	0.75	-	tCK	1
Loopback Setup time for LBDQS	tLBQ_Set	0.55	-	0.55	-	tCK	1, 2
Loopback Hold time for LBDQS	tLBQ_Hld	0.55	-	0.55	-	tCK	1, 2
Loopback Data valid window of each UI per DRAM	tLBDVW	1.6	-	1.6	-	tCK	1

NOTE 1 Based on Loopback 4-way interleave setting (see MR53)
NOTE 2 tLBQ_Set is measured from LBDQ first transition to LBDQS falling edge and tLBQ_Hld is measured from LBDQS falling edge to LBDQ last transition.

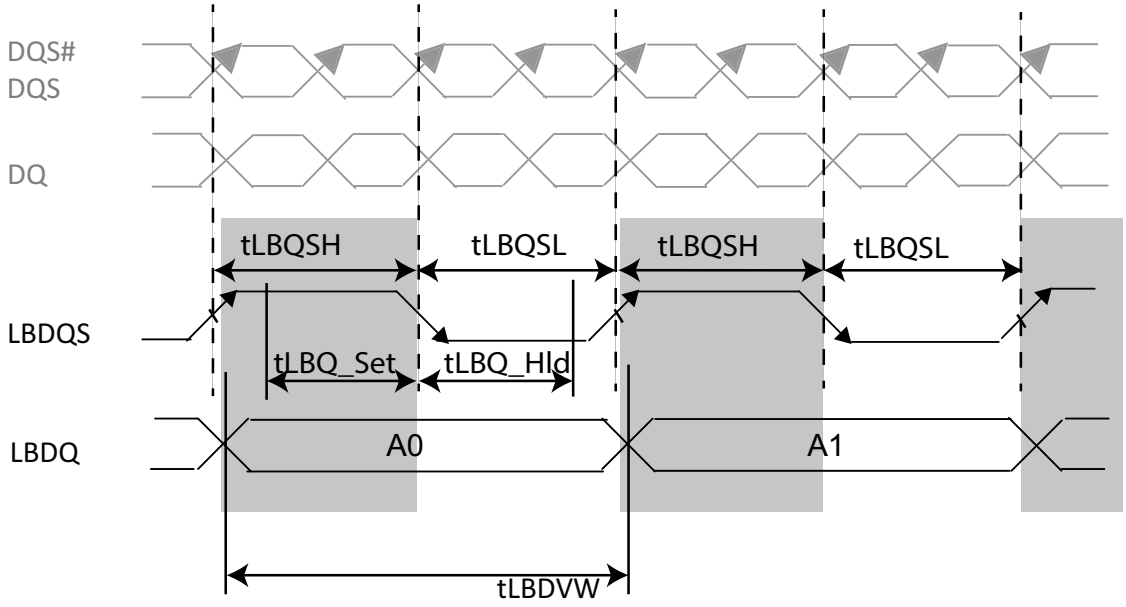


Figure 242 — Loopback Strobe to Data Relationship

9.3.1 ALERT_n Output Drive Characteristic

A functional representation of the output buffer is shown in Figure 243. Output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{Vout}{|\ Iout\ |}$$ under the condition that RON_{Pu} is off

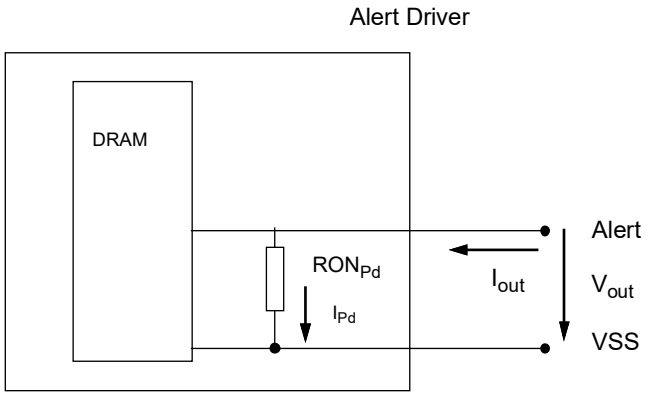


Figure 243 — Output Buffer Ron

Table 251 — Output Driver Impedance RON

Resistor	Vout	Min	Max	Unit	Note
RON_{Pd}	VOLdc= 0.1* VDDQ	0.3	1.1	$R_{ZQ}/7$	
	V_{OMdc} = 0.8* VDDQ	0.4	1.1	$R_{ZQ}/7$	
	V_{OHdc} = 0.95* VDDQ	0.4	1.25	$R_{ZQ}/7$	

9.3.2 Output Driver Characteristic of Connectivity Test (CT) Mode

Following Output driver impedance RON will be applied to the Test Output Pin during Connectivity Test (CT) Mode.

The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu_CT} = \frac{V_{DDQ}-V_{OUT}}{|Iout|}$$

$$RON_{Pd_CT} = \frac{V_{OUT}}{|Iout|}$$

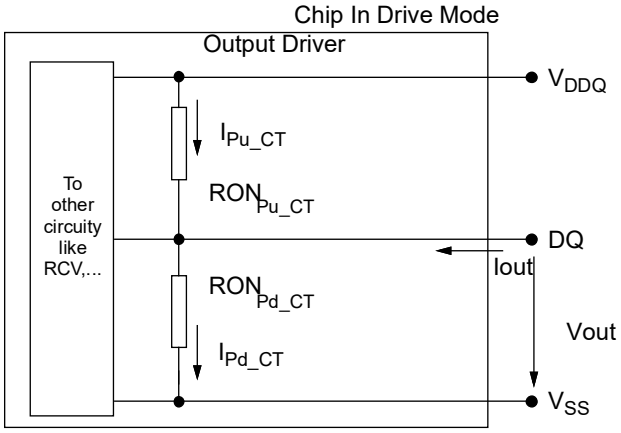


Figure 244 — Output Driver

Table 252 — Output Driver Characteristic of Connectivity Test (CT) Mode

RONNOM_CT	Resistor	Vout	Max	Units	Note
34 Ω	RONPd_CT	VOBdc = 0.2 x VDDQ	1.9	$R_{ZQ}/7$	1, 2
		VOLdc = 0.5 x VDDQ	2.0	$R_{ZQ}/7$	1, 2
		VOMdc = 0.8 x VDDQ	2.2	$R_{ZQ}/7$	1, 2
		VOHdc = 0.95 x VDDQ	2.5	$R_{ZQ}/7$	1, 2
	RONPu_CT	VOBdc = 0.2 x VDDQ	1.9	$R_{ZQ}/7$	1, 2
		VOLdc = 0.5 x VDDQ	2.0	$R_{ZQ}/7$	1, 2
		VOMdc = 0.8 x VDDQ	2.2	$R_{ZQ}/7$	1, 2
		VOHdc = 0.95 x VDDQ	2.5	$R_{ZQ}/7$	1, 2

NOTE 1 Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.
NOTE 2 Uncalibrated drive strength tolerance is specified at +/- 30%

9.4 Single-ended Output Levels - VOL/VOH

Table 253 — Single-ended Output Levels for DDR5-3200 to DDR5-6400

Symbol	Parameter	DDR5-3200-6400	Units	Notes
V_{OH}	Output high measurement level (for output SR)	0.75 x V_{pk-pk}	V	1
V_{OL}	Output low measurement level (for output SR)	0.25 x V_{pk-pk}	V	1
NOTE 1 V_{pk-pk} is the mean high voltage minus the mean low voltage over 8UI samples.				

Table 254 — Single-ended Output Levels for DDR5-6800 to DDR5-9200

Symbol	Parameter	DDR5-6800-9200	Units	Notes
VOH	Output high measurement level (for output SR)	0.75 x Vpk-pk	V	1
VOL	Output low measurement level (for output SR)	0.25 x Vpk-pk	V	1
NOTE 1 V_{pk-pk} is the mean high voltage minus the mean low voltage over 8UI samples.				

9.4.1 DDP Single-ended Output Levels - VOL/VOH

Table 255 — DDP Single-Ended Output Levels for DDR5 DDP 3200 to 6400

Symbol	Parameter	DDR5 DDP 3200-6400	Units	Notes
VOH	Output high measurement level (for output SR)	0.75 x V_{pk-pk}	V	1
VOL	Output low measurement level (for output SR)	0.25 x V_{pk-pk}	V	1
NOTE 1 V_{pk-pk} is the mean high voltage minus the mean low voltage over 8UI samples.				

9.5 Single-Ended Output Levels - VOL/VOH for Loopback Signals

Table 256 — Single-ended Output Levels for Loopback Signals DDR5-3200 to DDR5-6400

Symbol	Parameter	DDR5-3200-6400	Units	Notes
V_{OH}	Output high measurement level (for output SR)	0.75 x V_{pk-pk}	V	1
V_{OL}	Output low measurement level (for output SR)	0.25 x V_{pk-pk}	V	1
NOTE 1 V_{pk-pk} is the mean high voltage minus the mean low voltage over 8UI samples.				

Table 257 — Single-ended Output Levels for Loopback Signals DDR5-6800 to DDR5-9200

Symbol	Parameter	DDR5-6800-9200	Units	Notes
V_{OH}	Output high measurement level (for output SR)	0.75 x V_{pk-pk}	V	1
V_{OL}	Output low measurement level (for output SR)	0.25 x V_{pk-pk}	V	1
NOTE 1 V_{pk-pk} is the mean high voltage minus the mean low voltage over 8UI samples.				

9.5.1 DDP Single-Ended Output Levels - VOL/VOH for Loopback Signals

Table 258 — DDP Single-ended Output Levels for Loopback Signals DDR5 DDP 3200 to 6400

Symbol	Parameter	DDR5 DDP 3200-6400	Units	Notes
V_{OH}	Output high measurement level (for output SR)	0.75 x V_{pk-pk}	V	1
V_{OL}	Output low measurement level (for output SR)	0.25 x V_{pk-pk}	V	1
NOTE 1 V_{pk-pk} is the mean high voltage minus the mean low voltage over 8UI samples.				

9.6 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OL} and V_{OH} for single ended signals as shown in Table 259 and Figure 245.

Table 259 — Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}	V_{OH}	[V_{OH}-V_{OL}] / delta TRse
Single ended output slew rate for falling edge	V_{OH}	V_{OL}	[V_{OH}-V_{OL}] / delta TFse
NOTE 1 Output slew rate is verified by design and characterization, and may not be subject to production test.			

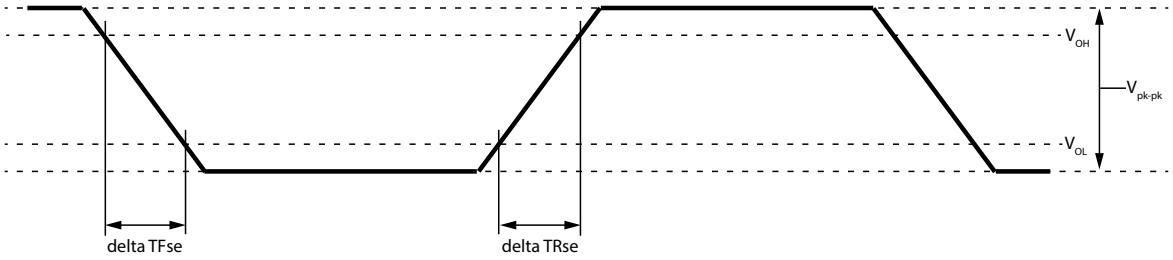


Figure 245 — Single-ended Output Slew Rate Definition

Table 260 — Single-ended Output Slew Rate for DDR5-3200 to DDR5-4800

Speed		DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Single ended output slew rate	SRQse	8	24	8	24	8	24	8	24	8	24	V/ns	

Table 261 — Single-ended Output Slew Rate for DDR5-5200 to DDR5-6400

Speed		DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Single ended output slew rate	SRQse	12	24	12	24	12	24	12	24	V/ns	

Table 262 — Single-ended Output Slew Rate for DDR5-6800 to DDR5-9200

Speed		DDR5-6800		DDR5-7200		DDR5-7600		DDR5-8000		DDR5-8400		DDR5-8800		DDR5-9200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Single ended output slew rate	SRQse	12	24	12	24	12	24	12	24	12	24	12	24	12	24	V/ns	

9.6.1 DDP Single-Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OL} and V_{OH} for single ended signals as shown in Table 263 and Figure 246.

Table 263 — DDP Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}	V_{OH}	[V_{OH}-V_{OL}] / delta TRse
Single ended output slew rate for falling edge	V_{OH}	V_{OL}	[V_{OH}-V_{OL}] / delta TFse
NOTE 1 Output slew rate is verified by design and characterization, and may not be subject to production test.			

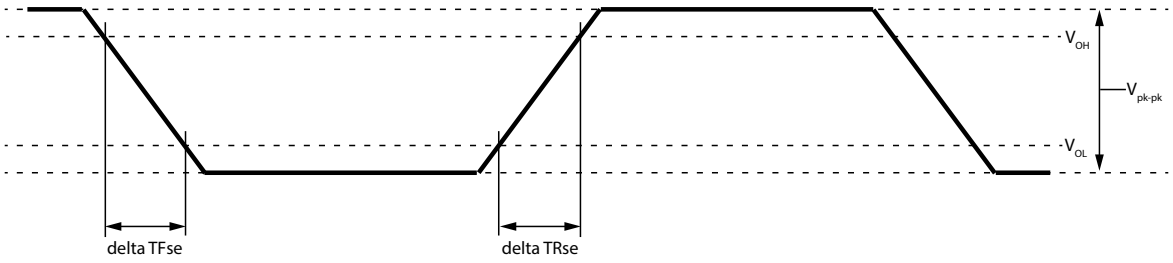


Figure 246 — Single-ended Output Slew Rate Definition

Table 264 — DDP Single-ended Output Slew Rate for DDR5-3200 to DDR5-6400

Speed		DDR5 DDP 3200-6400		Units	NOTE
Parameter	Symbol	MIN	MAX		
Single ended output slew rate	SRQse	4	15	V/ns	

9.7 Differential Output Levels

Table 265 — Differential Output levels for DDR5-3200 to DDR5-6400

Symbol	Parameter	DDR5-3200-6400	Units	Notes
V_{OHdiff}	Differential output high measurement level (for output SR)	0.75 x $V_{diffpk-pk}$	V	1
V_{OLdiff}	Differential output low measurement level (for output SR)	0.25 x $V_{diffpk-pk}$	V	1
NOTE 1 $V_{diffpk-pk}$ is the mean high voltage minus the mean low voltage over 8UI samples.				

Table 266 — Differential AC and DC Output Levels for DDR5-6800 to DDR5-9200

Symbol	Parameter	DDR5-6800-9200	Units	Notes
V_{OHdiff}	Differential output high measurement level (for output SR)	0.75 x $V_{diffpk-pk}$	V	1
V_{OLdiff}	Differential output low measurement level (for output SR)	0.25 x $V_{diffpk-pk}$	V	1
NOTE 1 $V_{diffpk-pk}$ is the mean high voltage minus the mean low voltage over 8UI samples.				

9.7.1 DDP Differential Output Levels

Table 267 — DDP Differential Output Levels for DDR5-3200 to DDR5-6400

Symbol	Parameter	DDR5-3200-6400	Units	Notes
V_{OHdiff}	Differential output high measurement level (for output SR)	0.75 x $V_{diffpk-pk}$	V	1
V_{OLdiff}	Differential output low measurement level (for output SR)	0.25 x $V_{diffpk-pk}$	V	1
NOTE 1 $V_{diffpk-pk}$ is the mean high voltage minus the mean low voltage over 8UI samples.				

9.8 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL-diff}$ and V_{OHdiff} for differential signals as shown in Table 268 and Figure 247

Table 268 — Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	V_{OLdiff}	V_{OHdiff}	[V_{OHdiff}-V_{OLdiff}] / delta TRdiff
Differential output slew rate for falling edge	V_{OHdiff}	V_{OLdiff}	[V_{OHdiff}-V_{OLdiff}] / delta TFdiff
NOTE 1 Output slew rate is verified by design and characterization, and may not be subject to production test.			

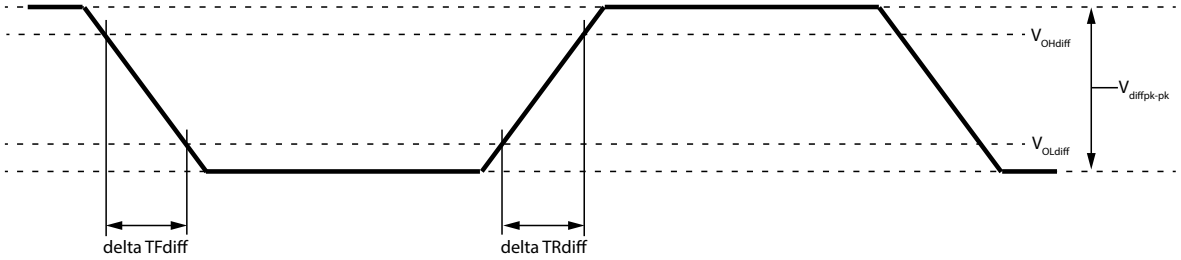


Figure 247 — Differential Output Slew Rate Definition

Table 269 — Differential Output Slew Rate for DDR5-3200 to DDR5-4800

Speed		DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Differential output slew rate	SRQdiff	16	48	16	48	16	48	16	48	16	48	V/ns	

Table 270 — Differential Output Slew Rate for DDR5-5200 to DDR5-6400

Speed		DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Differential output slew rate	SRQdiff	24	48	24	48	24	48	24	48	V/ns	

Table 271 — Differential Output Slew Rate for DDR5-6800 to DDR5-9200

Speed		DDR5-6800		DDR5-7200		DDR5-7600		DDR5-8000		DDR5-8400		DDR5-8800		DDR5-8800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Differential output slew rate	SRQdiff	24	48	24	48	24	48	24	48	24	48	24	48	24	48	V/ns	

9.8.1 DDP Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OLdiff} and V_{OHdiff} for differential signals as shown in Table 272 and Figure 248

Table 272 — DDP Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	V_{OLdiff}	V_{OHdiff}	[V_{OHdiff}-V_{OLdiff}] / delta TRdiff
Differential output slew rate for falling edge	V_{OHdiff}	V_{OLdiff}	[V_{OHdiff}-V_{OLdiff}] / delta TFdiff
NOTE 1 Output slew rate is verified by design and characterization, and may not be subject to production test.			

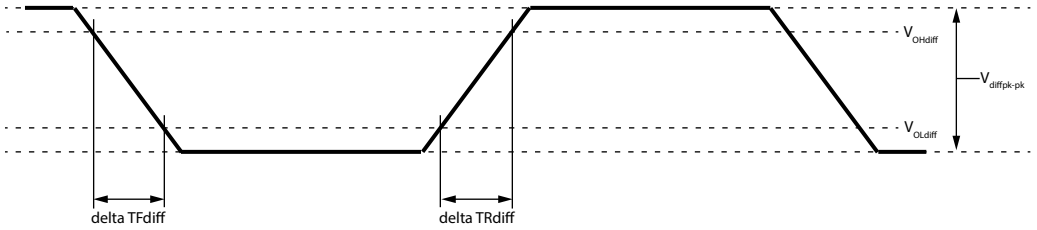


Figure 248 — Differential Output Slew Rate Definition

Table 273 — DDP Differential Output Slew Rate for DDR5-3200 to DDR5-6400

Speed		DDR5 DDP 3200-6400		Units	NOTE
Parameter	Symbol	MIN	MAX		
Differential output slew rate	SRQdiff	8	30	V/ns	

9.9 Tx DQS Jitter

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in Table 274.

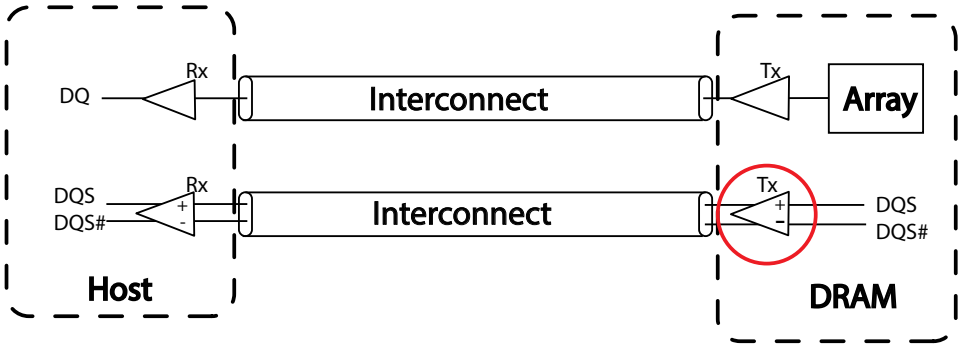


Figure 249 — Tx DQS Jitter

9.9 Tx DQS Jitter (cont'd)

Table 274 — Tx DQS Jitter Parameters for DDR5-3200 to 4800

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Rj RMS Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Rj_NoBUJ	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	UI (RMS)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12
Dj pp Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Dj_NoBUJ	-	0.150	-	0.150	-	0.150	-	0.150	-	0.150	UI	1, 2, 3, 5, 6, 7, 8, 9, 10, 11
Rj RMS Value of N-UI jitter without BUJ, where 1<N< 4	tTx_DQS_NUI_Rj_NoBUJ	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	UI (RMS)	1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12
Dj pp Value of N-UI Jitter without BUJ, where 1<N < 4	tTx_DQS_NUI_Dj_NoBUJ	-	0.150	-	0.150	-	0.150	-	0.150	-	0.150	UI	1, 2, 3, 5, 6, 7, 8, 9, 10, 11

NOTE 1 On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility

NOTE 2 On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers, so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility

NOTE 3 The validation methodology for these parameters will be covered in future ballots

NOTE 4 Rj RMS value of 1-UI jitter. Without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD

NOTE 5 See Section 7.1 for details on the minimum BER requirements

NOTE 6 See Section 7.2 for details on UI, NUI and Jitter definitions

NOTE 7 Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running the Tx DQ Jitter test

NOTE 8 The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44, and the Mode Registers for the Per Pin DCA of DQS are MR103 - MR110.

NOTE 9 Spread Spectrum Clocking (SSC) must be disabled while running the Tx DQ Jitter test

NOTE 10 These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to "1" to enable this feature.

NOTE 11 Tested on the CTC2 card only

NOTE 12 The max value of tTx_DQS_Rj_1UI_NoBUJ and tTx_DQS_Rj_NUI_NoBUJ can be 6 mUI RMS

9.9 Tx DQS Jitter (cont'd)

Table 275 — Tx DQS Jitter Parameters for DDR5-5200 to 6400

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Rj RMS Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Rj_NoBUJ	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	UI (RMS)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12
Dj pp Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Dj_NoBUJ	-	0.130	-	0.130	-	0.130	-	0.130	UI	1, 2, 3, 5, 6, 7, 8, 9, 10, 11
Rj RMS Value of N-UI jitter without BUJ, where 1<N< 4	tTx_DQS_NUI_Rj_NoBUJ	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	-	-	-	UI (RMS)	1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12
Dj pp Value of N-UI Jitter without BUJ, where 1<N < 4	tTx_DQS_NUI_Dj_NoBUJ	-	0.130	-	0.130	-	-	-	-	UI	1, 2, 3, 5, 6, 7, 8, 9, 10, 11
Rj RMS Value of N-UI jitter without BUJ, where 1<N< 5	tTx_DQS_NUI_Rj_NoBUJ	-	-	-	-	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	UI (RMS)	1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12
Dj pp Value of N-UI Jitter without BUJ, where 1<N < 5	tTx_DQS_NUI_Dj_NoBUJ	-	-	-	-	-	0.130	-	0.130	UI	1, 2, 3, 5, 6, 7, 8, 9, 10, 11

NOTE 1 On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility

NOTE 2 On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers, so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility

NOTE 3 The validation methodology for these parameters will be covered in future ballots

NOTE 4 Rj RMS value of 1-UI jitter. Without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD

NOTE 5 See Section 7.1 for details on the minimum BER requirements

NOTE 6 See Section 7.2 for details on UI, NUI and Jitter definitions

NOTE 7 Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running the Tx DQ Jitter test

NOTE 8 The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44, and the Mode Registers for the Per Pin DCA of DQS are MR103 - MR110.

NOTE 9 Spread Spectrum Clocking (SSC) must be disabled while running the Tx DQ Jitter test

NOTE 10 These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to "1" to enable this feature.

NOTE 11 Tested on the CTC2 card only

NOTE 12 The max value of tTx_DQS_Rj_1UI_NoBUJ and tTx_DQS_Rj_NUI_NoBUJ can be 6 mUI RMS

9.9 Tx DQS Jitter (cont'd)

Table 276 — Tx DQS Jitter Parameters for DDR5-6800 to 9200

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-6800		DDR5-7200		DDR5-7600		DDR5-8000		DDR5-8400		DDR5-8800		DDR5-9200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Rj RMS Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Rj_NoBUJ	-	0.006	-	0.006	-	0.006	-	0.006	-	0.006	-	0.006	-	0.006	UI (RMS)	1,2,3,4, 5,6,7,8,9, 10,11,12
Dj pp Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Dj_NoBUJ	-	0.130	-	0.130	-	0.130	-	0.130	-	0.130	-	0.130	-	0.130	UI	1,2,3,5,6, 7,8,9,10, 11
Rj RMS Value of N-UI jitter without BUJ, where 1<N< 6	tTx_DQS_NUI_Rj_NoBUJ	-	0.006	-	0.006	-	0.006	-	0.006	-	0.006	-	0.006	-	0.006	UI (RMS)	1,2,3,5,6, 7,8,9,10, 11,12
Dj pp Value of N-UI Jitter without BUJ, where 1<N < 6	tTx_DQS_NUI_Dj_NoBUJ	-	0.130	-	0.130	-	0.130	-	0.130	-	0.130	-	0.130	-	0.130	UI	1,2,3,5,6, 7,8,9,10, 11

NOTE 1 On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility

NOTE 2 On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers, so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility

NOTE 3 The validation methodology for these parameters will be covered in future ballots

NOTE 4 Rj RMS value of 1-UI jitter. Without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD

NOTE 5 See Section 7.1 for details on the minimum BER requirements

NOTE 6 See Section 7.2 for details on UI, NUI and Jitter definitions

NOTE 7 Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running the Tx DQ Jitter test

NOTE 8 The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44.

NOTE 9 Spread Spectrum Clocking (SSC) must be disabled while running the Tx DQ Jitter test

NOTE 10 These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to "1" to enable this feature.

NOTE 11 Tested on the CTC2 card only

NOTE 12 The max value of tTx_DQS_Rj_1UI_NoBUJ and tTx_DQS_Rj_NUI_NoBUJ can be 6 mUI RMS

9.10 Tx DQ Jitter

9.10.1 Overview

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in Table 277.

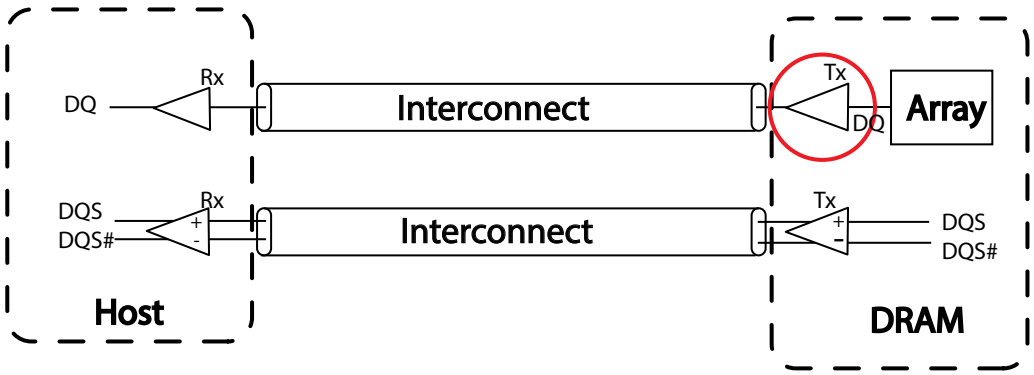


Figure 250 — Random Jitter R_j

9.10.2 Tx DQ Jitter Parameters

Table 277 — Tx DQ Jitter Parameters for DDR5-3200 to 4800

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Rj RMS of 1-UI jitter without BUJ	tTx_DQ_1UI_Rj_NoBUJ	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	UI (RMS)	1, 3, 4, 5, 7, 8, 9, 10, 11, 12, 13, 14
Dj pp 1-UI jitter without BUJ	tTx_DQ_1UI_Dj_NoBUJ	-	0.150	-	0.150	-	0.150	-	0.150	-	0.150	UI	3, 5, 7, 8, 9, 10, 11, 12, 13
Rj RMS of N-UI jitter without BUJ, where 1<N<4	tTx_DQ_NUI_Rj_NoBUJ	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	UI (RMS)	3, 5, 7, 8, 9, 10, 11, 12, 13, 14
Dj pp N-UI jitter without BUJ, where 1<N<4	tTx_DQ_NUI_Dj_NoBUJ	-	0.150	-	0.150	-	0.150	-	0.150	-	0.150	UI	3, 6, 7, 8, 9, 10, 11, 12, 13
Delay of any data lane relative to strobe lane	tTx_DQS2DQ	-0.100	0.100	-0.100	0.100	-0.100	0.100	-0.100	0.100	-0.100	0.100	UI	3, 5, 6, 7, 9, 10, 11, 12, 13

NOTE 1 On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.

NOTE 2 On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility

NOTE 3 The validation methodology for these parameters will be covered in future ballots

NOTE 4 Rj RMS value of 1-UI jitter without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD

NOTE 5 Delay of any data lane relative to strobe lane, as measured at Tx output

NOTE 6 Vref noise level to DQ jitter should be adjusted to minimize DCD

NOTE 7 See **Chapter 7** for details on the minimum BER requirements

NOTE 8 See **Chapter 7** for details on UI, NUI and Jitter definitions

NOTE 9 Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running this test

NOTE 10 The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44. Also the Mode Registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where $0 \le x \le 7$, and the Mode Registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where $0 \le y \le 7$.

NOTE 11 Spread Spectrum Clocking (SSC) must be disabled while running this test

NOTE 12 These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to “1” to enable this feature.

NOTE 13 Tested on the CTC2 card only

NOTE 14 The max value of tTx_DQ_Rj_1UI_NoBUJ and tTx_DQ_Rj_NUI_NoBUJ can be 6 mUI RMS

9.10.2 Tx DQ Jitter Parameters (cont'd)

Table 278 — Tx DQ Jitter Parameters for DDR5-5200 to 6400

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Rj RMS of 1-UI jitter without BUJ	tTx_DQ_1UI_Rj_NoBUJ	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	UI (RMS)	1, 3, 4, 5, 7, 8, 9, 10, 11, 12, 13, 14,
Dj pp 1-UI jitter without BUJ	tTx_DQ_1UI_Dj_NoBUJ	-	0.130	-	0.130	-	0.130	-	0.130	UI	3, 5, 7, 8, 9, 10, 11, 12, 13
Rj RMS of N-UI jitter without BUJ, where 1<N<4	tTx_DQ_NUI_Rj_NoBUJ	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	-	-	-	UI (RMS)	3, 5, 7, 8, 9, 10, 11, 12, 13, 14
Dj pp N-UI jitter without BUJ, where 1<N<4	tTx_DQ_NUI_Dj_NoBUJ	-	0.130	-	0.130	-	-	-	-	UI	3, 6, 7, 8, 9, 10, 11, 12, 13
Rj RMS of N-UI jitter without BUJ, where 1<N<5	tTx_DQ_NUI_Rj_NoBUJ	-	-	-	-	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	UI (RMS)	
Dj pp N-UI jitter without BUJ, where 1<N<5	tTx_DQ_NUI_Dj_NoBUJ	-	-	-	-	-	0.130		0.130	UI	
Delay of any data lane relative to strobe lane	tTx_DQS2DQ	-0.100	0.100	-0.100	0.100	-0.100	0.100	-0.100	0.100	UI	3, 5, 6, 7, 9, 10, 11, 12, 13

NOTE 1 On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.

NOTE 2 On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility

NOTE 3 The validation methodology for these parameters will be covered in future ballots

NOTE 4 Rj RMS value of 1-UI jitter without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD

NOTE 5 Delay of any data lane relative to strobe lane, as measured at Tx output

NOTE 6 Vref noise level to DQ jitter should be adjusted to minimize DCD

NOTE 7 See **Chapter 7** for details on the minimum BER requirements

NOTE 8 See **Chapter 7** for details on UI, NUI and Jitter definitions

NOTE 9 Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running this test

NOTE 10 The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44. Also the Mode Registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where $0 \le x \le 7$, and the Mode Registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where $0 \le y \le 7$.

NOTE 11 Spread Spectrum Clocking (SSC) must be disabled while running this test

NOTE 12 These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to "1" to enable this feature.

NOTE 13 Tested on the CTC2 card only

NOTE 14 The max value of tTx_DQ_Rj_1UI_NoBUJ and tTx_DQ_Rj_NUI_NoBUJ can be 6mUI RMS

9.10.2 Tx DQ Jitter Parameters (cont'd)

Table 279 — Tx DQ Jitter Parameters for DDR5-6800 to 9200

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-6800		DDR5-7200		DDR5-7600		DDR5-8000		DDR5-8400		DDR5-8800		DDR5-9200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Rj RMS of 1-UI jitter without BUJ	tTx_DQ_1UI_Rj_NoBUJ	-	0.006	-	0.006	-	0.006	-	0.006	-	0.006	-	0.006	-	0.006	UI (RMS)	1, 3, 5, 9, 11, 12, 13, 14, 15, 16, 17, 18
Dj pp 1-UI jitter without BUJ	tTx_DQ_1UI_Dj_NoBUJ	-	0.130	-	0.130	-	0.130	-	0.130	-	0.130	-	0.130	-	0.130	UI	3, 6, 9, 11, 12, 13, 14, 15, 16, 17
Rj RMS of N-UI jitter without BUJ, where 1<N<6	tTx_DQ_NUI_Rj_NoBUJ	-	0.006	-	0.006	-	0.006	-	0.006	-	0.006	-	0.006	-	0.006	UI (RMS)	3, 7, 9, 11, 12, 13, 14, 15, 16, 17, 18
Dj pp N-UI jitter without BUJ, where 1<N<6	tTx_DQ_NUI_Dj_NoBUJ	-	0.130	-	0.130	-	0.130	-	0.130	-	0.130	-	0.130	-	0.130	UI	3, 8, 10, 11, 12, 13, 14, 15, 16, 17
Delay of any data lane relative to strobe lane	tTx_DQS2DQ	-0.100	0.100	-0.100	0.100	-0.100	0.100	-0.100	0.100	-0.100	0.100	-0.100	0.100	-0.100	0.100	UI	3, 9, 10, 11, 13, 14, 15, 16, 17

NOTE 1 On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.

NOTE 2 On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility

NOTE 3 The validation methodology for these parameters will be covered in future ballots

NOTE 4 Rj RMS value of 1-UI jitter without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD

NOTE 5 Delay of any data lane relative to strobe lane, as measured at Tx output

NOTE 6 Vref noise level to DQ jitter should be adjusted to minimize DCD

NOTE 7 See **Chapter 7** for details on the minimum BER requirements

NOTE 8 See **Chapter 7** for details on UI, NUI and Jitter definitions

NOTE 9 Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Duty Cycle Adjuster feature prior to running this test

NOTE 10 The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44

NOTE 11 Spread Spectrum Clocking (SSC) must be disabled while running this test

NOTE 12 These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to "1" to enable this feature.

NOTE 13 Tested on the CTC2 card only

NOTE 14 The max value of tTx_DQ_Rj_1UI_NoBUJ and tTx_DQ_Rj_NU_NoBUJ can be 6mUI RMS

9.11 Tx DQ Stressed Eye

Tx DQ stressed eye height and eye width must meet minimum specification values at BER=E^{-9} and confidence level 99.5%. Tx DQ Stressed Eye shows the DQS to DQ skew for both Eye Width and Eye Height. In order to support different Host Receiver (Rx) designs, it is the responsibility of the Host to insure the advanced DQS edges are adjusted accordingly via the Read DQS Offset Timing mode register settings (MR40 OP[3:0]).

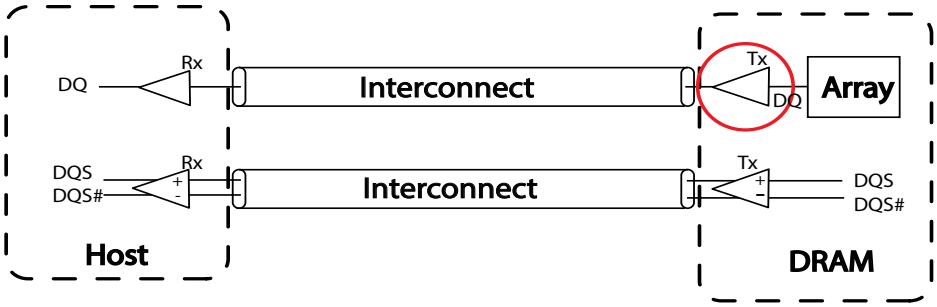


Figure 251 — Example of DDR5 Memory Interconnect

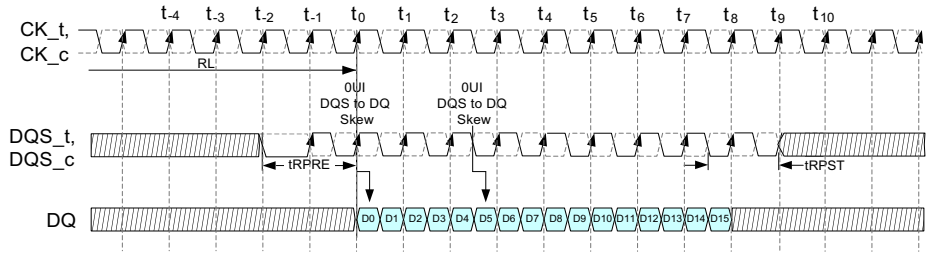


Figure 252 — Read Burst Example for Pin DQx Depicting Bit 0 and 5 Relative to the DQS Edge for 0 UI Skew

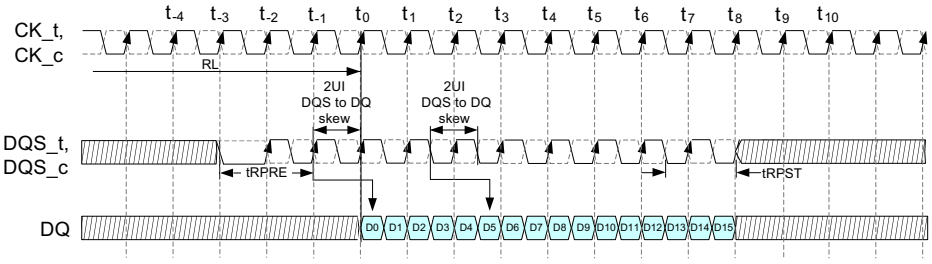


Figure 253 — Read Burst Example for Pin DQx Depicting Bit 0 and 5 Relative to the DQS Edge for 2 UI Skew with Read DQS Offset Timing Set to 1 Clock (2UI)

9.11.1 Tx DQ Stressed Eye Parameters

Table 280 — Tx DQ Stressed Eye Parameters for DDR5-3200 to 4800

[EH=Eye Height, EW=Eye Width; BER=Bit Error Rate, SES=Stressed Eye Skew]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Eye Width specified at the transmitter with a skew between DQ and DQS of 1UI	TxEW_DQ_SES_1UI	0.72	-	0.72	-	0.72	-	0.72	-	0.72	-	UI	1, 2, 3, 4, 6, 7, 8, 9, 10, 11
Eye Width specified at the transmitter with a skew between DQ and DQS of 2UI	TxEW_DQ_SES_2UI	0.72	-	0.72	-	0.72	-	0.72	-	0.72	-	UI	1, 2, 3, 4, 6, 7, 8, 9, 10, 11
Eye Width specified at the transmitter with a skew between DQ and DQS of 3UI	TxEW_DQ_SES_3UI	0.72	-	0.72	-	0.72	-	0.72	-	0.72	-	UI	1, 2, 3, 4, 6, 7, 8, 9, 10, 11

NOTE 1 Minimum BER E^{-9} and Confidence Level of 99.5% per pin

NOTE 2 Refer to the minimum Bit Error Rate (BER) requirements for DDR5

NOTE 3 The validation methodology for these parameters will be covered in future ballot(s)

NOTE 4 Mismatch is defined as DQS to DQ mismatch, in UI increments

NOTE 5 The number of UI's accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds, N=4,5 UI may not be applicable

NOTE 6 Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running this test

NOTE 7 The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44. Also the Mode Registers for the Per Pin DCA of DQS are MR103-MR110, the Mode Registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where $0 \le x \le 7$, and the Mode Registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where $0 \le y \le 7$.

NOTE 8 Spread Spectrum Clocking (SSC) must be disabled while running this test

NOTE 9 These parameters are tested using the continuous PRBS8 LFSR training pattern which are sent out on all DQ lanes off the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to "1" to enable this feature.

NOTE 10 Tested on the CTC2 card only

NOTE 11 Matched DQS to DQ would require the DQs to be adjusted by 0.5UI to place it in the center of the DQ eye. 1UI mismatch would require the DQS to be adjusted 1.5 UI. Generally, for XUI mismatch the DQ must be adjusted XUI + 0.5 UI to be placed in the center of the eye.

9.11.1 Tx DQ Stressed Eye Parameters (cont'd)

Table 281 — Tx DQ Stressed Eye Parameters for DDR5-5200 to 6400

[EH=Eye Height, EW=Eye Width; BER=Bit Error Rate]

Parameter	Symbol	DDR5-5200		DDR5-5600		DDR5-6000		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Eye Width specified at the transmitter with a skew between DQ and DQS of 1UI	TxEW_DQ_SES_1UI	0.74	-	0.74	-	0.75	-	0.75	-	UI	1, 2, 3, 4, 6, 7, 8, 9, 10, 11
Eye Width specified at the transmitter with a skew between DQ and DQS of 2UI	TxEW_DQ_SES_2UI	0.74	-	0.74	-	0.75	-	0.75	-	UI	1, 2, 3, 4, 6, 7, 8, 9, 10, 11
Eye Width specified at the transmitter with a skew between DQ and DQS of 3UI	TxEW_DQ_SES_3UI	0.74	-	0.74	-	0.75	-	0.75	-	UI	1, 2, 3, 4, 6, 7, 8, 9, 10, 11
Eye Width specified at the transmitter with a skew between DQ and DQS of 4UI	TxEW_DQ_SES_4UI	0.74	-	0.74	-	0.75	-	0.75	-	UI	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Eye Width specified at the transmitter with a skew between DQ and DQS of 5UI	TxEW_DQ_SES_5UI	-	-	-	-	0.75	-	0.75	-	UI	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

NOTE 1 Minimum BER E^{-9} and Confidence Level of 99.5% per pin

NOTE 2 Refer to the minimum Bit Error Rate (BER) requirements for DDR5

NOTE 3 The validation methodology for these parameters will be covered in future ballot(s)

NOTE 4 Mismatch is defined as DQS to DQ mismatch, in UI increments

NOTE 5 The number of UI's accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds, N=4,5 UI may not be applicable

NOTE 6 Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running this test

NOTE 7 The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44. Also the Mode Registers for the Per Pin DCA of DQS are MR103-MR110, the Mode Registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where $0 \le x \le 7$, and the Mode Registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where $0 \le y \le 7$

NOTE 8 Spread Spectrum Clocking (SSC) must be disabled while running this test

NOTE 9 These parameters are tested using the continuous PRBS8 LFSR training pattern which are sent out on all DQ lanes off the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to "1" to enable this feature.

NOTE 10 Tested on the CTC2 card only

NOTE 11 Matched DQS to DQ would require the DQs to be adjusted by 0.5UI to place it in the center of the DQ eye. 1UI mismatch would require the DQS to be adjusted 1.5UI. Generally, for XUI mismatch the DQ must be adjusted XUI + 0.5UI to be placed in the center of the eye.

9.11.1 Tx DQ Stressed Eye Parameters (cont'd)

Table 282 — Tx DQ Stressed Eye Parameters for DDR5-6800 to 9200

[EH=Eye Height, EW=Eye Width; BER=Bit Error Rate]

Parameter	Symbol	DDR5-6800		DDR5-7200		DDR5-7600		DDR5-8000		DDR5-8400		DDR5-8800		DDR5-9200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Eye Width specified at the transmitter with a skew between DQ and DQS of 1UI	TxEW_DQ_SES_1UI	0.76	-	0.76	-	0.76	-	0.76	-	0.76	-	0.76	-	0.76	-	UI	1, 2, 3, 4, 6, 7, 8, 9, 10, 11
Eye Width specified at the transmitter with a skew between DQ and DQS of 2UI	TxEW_DQ_SES_2UI	0.76	-	0.76	-	0.76	-	0.76	-	0.76	-	0.76	-	0.76	-	UI	1, 2, 3, 4, 6, 7, 8, 9, 10, 11
Eye Width specified at the transmitter with a skew between DQ and DQS of 3UI	TxEW_DQ_SES_3UI	0.76	-	0.76	-	0.76	-	0.76	-	0.76	-	0.76	-	0.76	-	UI	1, 2, 3, 4, 6, 7, 8, 9, 10, 11
Eye Width specified at the transmitter with a skew between DQ and DQS of 4UI	TxEW_DQ_SES_4UI	0.76	-	0.76	-	0.76	-	0.76	-	0.76	-	0.76	-	0.76	-	UI	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Eye Width specified at the transmitter with a skew between DQ and DQS of 5UI	TxEW_DQ_SES_5UI	0.76	-	0.76	-	0.76	-	0.76	-	0.76	-	0.76	-	0.76	-	UI	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

NOTE 1 Minimum BER E^{-9} and Confidence Level of 99.5% per pin

NOTE 2 Refer to the minimum Bit Error Rate (BER) requirements for DDR5

NOTE 3 The validation methodology for these parameters will be covered in future ballot(s)

NOTE 4 Mismatch is defined as DQS to DQ mismatch, in UI increments

NOTE 5 The number of UI's accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds, N=4,5 UI may not be applicable

NOTE 6 Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Duty Cycle Adjuster feature prior to running this test

NOTE 7 The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44

NOTE 8 Spread Spectrum Clocking (SSC) must be disabled while running this test

NOTE 9 These parameters are tested using the continuous PRBS8 LFSR training pattern which are sent out on all DQ lanes off the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to "1" to enable this feature.

NOTE 10 Tested on the CTC2 card only

NOTE 11 Matched DQS to DQ would require the DQs to be adjusted by 0.5UI to place it in the center of the DQ eye. 1UI mismatch would require the DQS to be adjusted 1.5UI. Generally, for XUI mismatch the DQ must be adjusted XUI + 0.5UI to be placed in the center of the eye.

10 Speed Bins

DDR5 Standard Speed Bins defined as:

3200 / 3600 / 4000 / 4400 / 4800 / 5200 / 5600 / 6000 / 6400 / 6800 / 7200 / 7600 / 8000 / 8400 / 8800

10.1 DDR5-3200 Speed Bins and Operations

Table 283 — DDR5-3200 Speed Bins and Operations

Speed Bin					DDR5-3200AN		DDR5-3200B		DDR5-3200BN		DDR5-3200C		Unit	Note
CL-nRCD-nRP					24-24-24		26-26-26		26-26-26		28-28-28			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	15.000	22.222	16.250	22.222	16.250	22.222	17.500	22.222	ns	12
Activate to Read or Write command delay time				tRCD	15.000	-	16.250	-	16.250	-	17.500	-	ns	7
Row Precharge time				tRP	15.000	-	16.250	-	16.250	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7,13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	47.000	-	48.250	-	48.250	-	49.500	-	ns	7,8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	RESERVED		ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
Supported CL					22,24,26,28		22,26,28		22,26,28		22,28		nCK	12

10.2 DDR5-3600 Speed Bins and Operations

Table 284 — DDR5-3600 Speed Bins and Operations

Speed Bin					DDR5-3600AN		DDR5-3600B		DDR5-3600BN		DDR5-3600C		Unit	Note
CL-nRCD-nRP					26-26-26		30-30-30		30-30-30		32-32-32			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	14.444	22.222	16.250	22.222	16.666	22.222	17.500	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.444	-	16.250	-	16.666	-	17.500	-	ns	7
Row Precharge time				tRP	14.444	-	16.250	-	16.666	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x* tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 x* tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 x* tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 x* tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7,13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.444	-	48.250	-	48.666	-	49.500	-	ns	7,8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	0.555	<0.625	RESERVED						ns	
Supported CL					22,24,26,28,30,32		22,26,28,30,32		22,28,30,32		22,28,32		nCK	12

10.3 DDR5-4000 Speed Bins and Operations

Table 285 — DDR5-4000 Speed Bins and Operations

Speed Bin					DDR5-4000AN		DDR5-4000B		DDR5-4000BN		DDR5-4000C		Unit	Note
CL-nRCD-nRP					28-28-28		32-32-32		32-32-32		36-35-35			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	14.000	22.222	16.000	22.222	16.000	22.222	17.500	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.000	-	16.000	-	16.000	-	17.500	-	ns	7
Row Precharge time				tRP	14.000	-	16.000	-	16.000	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x* tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 x* tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 x* tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 x* tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7,13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.000	-	48.000	-	48.000	-	49.500	-	ns	7,8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	RESERVED		ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	RESERVED		ns	
4000AN	14.000	14.000	28	tCK(AVG)	0.500	<0.555	RESERVED						ns	
Supported CL					22,24,26,28, 30,32,36		22,26,28, 30,32,36		22,26,28,30,32,36		22,28,32,36		nCK	12

10.4 DDR5-4400 Speed Bins and Operations

Table 286 — DDR5-4400 Speed Bins and Operations

Speed Bin					DDR5-4400AN		DDR5-4400B		DDR5-4400BN		DDR5-4400C		Unit	Note
CL-nRCD-nRP					32-32-32		36-36-36		36-36-36		40-39-39			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	14.545	22.222	16.000	22.222	16.363	22.222	17.500	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.545	-	16.000	-	16.363	-	17.500	-	ns	7
Row Precharge time				tRP	14.545	-	16.000	-	16.363	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x* tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 x* tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 x* tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 x* tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7, 13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.545	-	48.000	-	48.363	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	RESERVED								ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED								ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	14.545	14.545	32	tCK(AVG)	0.454	<0.500	RESERVED						ns	
Supported CL					22,24,26,28,30,32,36,40		22,26,28,30,32,36,40		22,28,30,32,36,40		22,28,32,36,40		nCK	12

10.5 DDR5-4800 Speed Bins and Operations

Table 287 — DDR5-4800 Speed Bins and Operations

Speed Bin					DDR5-4800AN		DDR5-4800B		DDR5-4800BN		DDR5-4800C		Unit	Note
CL-nRCD-nRP					34-34-34		40-39-39		40-40-40		42-42-42			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	14.166	22.222	16.000	22.222	16.666	22.222	17.500	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.166	-	16.000	-	16.666	-	17.500	-	ns	7
Row Precharge time				tRP	14.166	-	16.000	-	16.666	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7, 13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.166	-	48.000	-	48.666	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]		Supported Frequency Down Bins									
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED								ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	RESERVED				ns	
4400AN	14.545	14.545	32	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	14.166	14.166	34	tCK(AVG)	0.416	<0.454	RESERVED						ns	
Supported CL					22,24,26,28,30,32,34, 36,40,42		22,26,28,30,32,36, 40,42		22,28,30,32,36,40,42		22,28,32,36,40,42		nCK	12

10.6 DDR5-5200 Speed Bins and Operations

Table 288 — DDR5-5200 Speed Bins and Operations

Speed Bin					DDR5-5200AN		DDR5-5200B		DDR5-5200BN		DDR5-5200C		Unit	Note
CL-nRCD-nRP					38-38-38		42-42-42		42-42-42		46-46-46			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	14.615	22.222	16.000	22.222	16.153	22.222	17.500	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.615	-	16.000	-	16.153	-	17.500	-	ns	7
Row Precharge time				tRP	14.615	-	16.000	-	16.153	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7, 13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.615	-	48.000	-	48.153	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	RESERVED		ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	RESERVED								ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED								ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	14.545	14.545	32	tCK(AVG)	RESERVED								ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800AN	14.166	14.166	34	tCK(AVG)	RESERVED								ns	
5200C	17.692	17.692	46	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	RESERVED		ns	
5200AN	14.615	14.615	38	tCK(AVG)	0.384	<0.416	RESERVED						ns	
Supported CL					22,24,26,28,30,32,36, 38,40,42,46		22,26,28,30,32,36,40, 42,46		22,26,28,30,32,36,40, 42,46		22,28,32,36,40,42,46		nCK	12

10.7 DDR5-5600 Speed Bins and Operations

Table 289 — DDR5-5600 Speed Bins and Operations

Speed Bin					DDR5-5600AN		DDR5-5600B		DDR5-5600BN		DDR5-5600C		Unit	Note
CL-nRCD-nRP					40-40-40		46-45-45		46-46-46		50-49-49			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	14.285	22.222	16.000	22.222	16.428	22.222	17.500	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.285	-	16.000	-	16.428	-	17.500	-	ns	7
Row Precharge time				tRP	14.285	-	16.000	-	16.428	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7, 13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.285	-	48.000	-	48.428	-	49.500	-	ns	7 ,8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED								ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	RESERVED				ns	
4400AN	14.545	14.545	32	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	14.166	14.166	34	tCK(AVG)	RESERVED								ns	
5200C	17.692	17.692	46	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	tCK(AVG)	0.384	<0.416	0.384	<0.416	RESERVED				ns	
5200AN	14.615	14.615	38	tCK(AVG)	0.384	<0.416	RESERVED						ns	
5600C	17.857	17.500	50	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600B	16.428	16.071	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600AN	14.285	14.285	40	tCK(AVG)	0.357	<0.384	RESERVED						ns	
Supported CL					22,24,26,28,30,32,36, 38,40,42,46,50		22,26,28,30,32,36,40, 42,46,50		22,28,30,32,36,40,42, 46,50		22,28,32,36,40,42, 46,50		nCK	12

10.8 DDR5-6000 Speed Bins and Operations

Table 290 — DDR5-6000 Speed Bins and Operations

Speed Bin					DDR5-6000AN		DDR5-6000B		DDR5-6000BN		DDR5-6000C		Unit	Note
CL-nRCD-nRP					42-42-42		48-48-48		48-48-48		54-53-53			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	14.000	22.222	16.000	22.222	16.000	22.222	17.500	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.000	-	16.000	-	16.000	-	17.500	-	ns	7
Row Precharge time				tRP	14.000	-	16.000	-	16.000	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x* tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 x* tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 x* tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 x* tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7,13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.000	-	48.000	-	48.000	-	49.500	-	ns	7,8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	RESERVED		ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	RESERVED		ns	
4000AN	14.000	14.000	28	tCK(AVG)	0.500	<0.555	RESERVED						ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	14.545	14.545	32	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800AN	14.166	14.166	34	tCK(AVG)	0.416	<0.454	RESERVED						ns	
5200C	17.692	17.692	46	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	RESERVED		ns	
5200AN	14.615	14.615	38	tCK(AVG)	0.384	<0.416	RESERVED						ns	
5600C	17.857	17.500	50	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600B	16.428	16.071	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600AN	14.285	14.285	40	tCK(AVG)	0.357	<0.384	RESERVED						ns	
6000C	18.000	17.666	54	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	RESERVED		ns	
6000AN	14.000	14.000	42	tCK(AVG)	0.333	<0.357	RESERVED						ns	
Supported CL					22,24,26,28,30,32,34, 36,38,40,42,46,48,50, 54		22,26,28,30,32,36,40, 42,46,48,50,54		22,26,28,30,32,36,40, 42,46,48,50,54		22,28,32,36,40,42,46, 50,54		nCK	12

10.9 DDR5-6400 Speed Bins and Operations

Table 291 — DDR5-6400 Speed Bins and Operations

Speed Bin					DDR5-6400AN		DDR5-6400B		DDR5-6400BN		DDR5-6400C		Unit	Note
CL-nRCD-nRP					46-46-46		52-52-52		52-52-52		56-56-56			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	14.375	22.222	16.000	22.222	16.250	22.222	17.500	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.375	-	16.000	-	16.250	-	17.500	-	ns	7
Row Precharge time				tRP	14.375	-	16.000	-	16.250	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7, 13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.375	-	48.000	-	48.250	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	RESERVED		ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED								ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	14.545	14.545	32	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800AN	14.166	14.166	34	tCK(AVG)	RESERVED								ns	
5200C	17.692	17.692	46	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	tCK(AVG)	0.384	<0.416	0.384	<0.416	RESERVED				ns	
5200AN	14.615	14.615	38	tCK(AVG)	0.384	<0.416	RESERVED						ns	
5600C	17.857	17.500	50	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600B	16.428	16.071	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600AN	14.285	14.285	40	tCK(AVG)	RESERVED								ns	
6000C	18.000	17.666	54	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	tCK(AVG)	0.333	<0.357	0.333	<0.357	RESERVED		RESERVED		ns	
6000AN	14.000	14.000	42	tCK(AVG)	RESERVED								ns	
6400C	17.500	17.500	56	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	16.250	16.250	52	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	RESERVED		ns	
6400AN	14.375	14.375	46	tCK(AVG)	0.312	<0.333	RESERVED						ns	
Supported CL					22,24,26,28,30,32,36, 38,40,42,46,48,50,52, 54,56		22,26,28,30,32,36,40, 42,46,48,50,52,54,56		22,26,28,30,32,36,40, 42,46,50,52,54,56		22,28,32,36,40,42,46, 50,54,56		nCK	12

10.10 DDR5-6800 Speed Bins and Operations

Table 292 — DDR5-6800 Speed Bins and Operations

Speed Bin					DDR5-6800AN		DDR5-6800B		DDR5-6800BN		DDR5-6800C		Unit	Note
CL-nRCD-nRP					48-48-48		56-55-55		56-56-56		60-60-60			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	14.117	-	16.000	-	16.470	-	17.500	-	ns	12
Activate to Read or Write command delay time				tRCD	14.117	-	16.000	-	16.470	-	17.500	-	ns	7
Row Precharge time				tRP	14.117	-	16.000	-	16.470	-	17.500		ns	7
Activate to Precharge command period				tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7,13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.117	-	48.000	-	48.000		49.500	-	ns	7,8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED								ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	RESERVED				ns	
4400AN	14.545	14.545	32	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	14.166	14.166	34	tCK(AVG)	0.416	<0.454	RESERVED						ns	
5200C	17.692	17.692	46	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	tCK(AVG)	0.384	<0.416	0.384	<0.416	RESERVED				ns	
5200AN	14.615	14.615	38	tCK(AVG)	0.384	<0.416	RESERVED						ns	
5600C	17.857	17.500	50	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600B	16.428	16.071	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600AN	14.285	14.285	40	tCK(AVG)	0.357	<0.384	RESERVED						ns	
6000C	18.000	17.666	54	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	tCK(AVG)	0.333	<0.357	0.333	<0.357	RESERVED				ns	
6000AN	14.000	14.000	42	tCK(AVG)	RESERVED								ns	
6400C	17.500	17.500	56	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	16.250	16.250	52	tCK(AVG)	0.312	<0.333	0.312	<0.333	RESERVED				ns	
6400AN	14.375	14.375	46	tCK(AVG)	0.312	<0.333	RESERVED						ns	
6800C	17.647	17.647	60	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	16.470	16.470	56	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	RESERVED		ns	
6800B	16.470	16.176	56	tCK(AVG)	0.294	<0.312	0.294	<0.312	RESERVED				ns	
6800AN	14.117	14.117	48	tCK(AVG)	0.294	<0.312	RESERVED						ns	
Supported CL					22,24,26,28,30,32,34,36,38,40,42,46,48,50,52,54,56,60		22,26,28,30,32,36,40,42,46,48,50,52,54,56,60		22,28,30,32,36,40,42,46,50,54,56,60		22,28,32,36,40,42,46,50,54,56,60		nCK	12

10.11 DDR5-7200 Speed Bins and Operations

Table 293 — DDR5-7200 Speed Bins and Operations

Speed Bin				DDR5-7200AN		DDR5-7200B		DDR5-7200BN		DDR5-7200C		Unit	Note
CL-nRCD-nRP				52-52-52		58-58-58		58-58-58		64-63-63			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data			tAA	14.444	-	16.000	-	16.111	-	17.500	-	ns	12
Activate to Read or Write command delay time			tRCD	14.444	-	16.000	-	16.111	-	17.500	-	ns	7
Row Precharge time			tRP	14.444	-	16.000	-	16.111	-	17.500	-	ns	7
Activate to Precharge command period			tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7, 13
Activate to Activate or Refresh command period			tRC (tRAS +tRP)	46.444	-	48.000	-	48.111	-	49.500	-	ns	7, 8
CAS Write Latency			CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table									
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	RESERVED		ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED								ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	14.545	14.545	32	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800AN	14.166	14.166	34	tCK(AVG)	RESERVED								ns	
5200C	17.692	17.692	46	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	RESERVED		ns	
5200AN	14.615	14.615	38	tCK(AVG)	0.384	<0.416	RESERVED						ns	
5600C	17.857	17.500	50	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600B	16.428	16.071	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600AN	14.285	14.285	40	tCK(AVG)	RESERVED								ns	
6000C	18.000	17.666	54	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	tCK(AVG)	0.333	<0.357	0.333	<0.357	RESERVED				ns	
6000AN	14.000	14.000	42	tCK(AVG)	RESERVED								ns	
6400C	17.500	17.500	56	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	16.250	16.250	52	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	RESERVED		ns	
6400AN	14.375	14.375	46	tCK(AVG)	RESERVED								ns	
6800C	17.647	17.647	60	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	16.470	16.470	56	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	RESERVED		ns	
6800B	16.470	16.176	56	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	RESERVED		ns	
6800AN	14.117	14.117	48	tCK(AVG)	RESERVED								ns	
7200C	17.777	17.500	64	tCK(AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200BN,B	16.111	16.111	58	tCK(AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	RESERVED		ns	
7200AN	14.444	14.444	52	tCK(AVG)	0.277	<0.294	RESERVED						ns	
Supported CL				22,24,26,28,30,32,36,38,40,42,46,48,50,52,54,56,58,60,64		22,26,28,30,32,36,40,42,46,48,50,52,54,56,58,60,64		22,26,28,30,32,36,40,42,46,50,52,54,56,58,60,64		22,28,32,36,40,42,46,50,54,56,60,64		nCK	12

10.12 DDR5-7600 Speed Bins and Operations

Table 294 — DDR5-7600 Speed Bins and Operations

Speed Bin					DDR5-7600AN		DDR5-7600B		DDR5-7600BN		DDR5-7600C		Unit	Note
CL-nRCD-nRP					54-54-54		62-61-61		62-62-62		68-67-67			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	14.210	-	16.000	-	16.315	-	17.500	-	ns	12
Activate to Read or Write command delay time				tRCD	14.210	-	16.000	-	16.315	-	17.500	-	ns	7
Row Precharge time				tRP	14.210	-	16.000	-	16.315	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7, 13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.210	-	48.000	-	48.315	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED								ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	14.545	14.545	32	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	14.166	14.166	34	tCK(AVG)	RESERVED								ns	
5200C	17.692	17.692	46	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	tCK(AVG)	0.384	<0.416	0.384	<0.416	RESERVED				ns	
5200AN	14.615	14.615	38	tCK(AVG)	0.384	<0.416	RESERVED						ns	
5600C	17.857	17.500	50	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600B	16.428	16.071	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600AN	14.285	14.285	40	tCK(AVG)	0.357	<0.384	RESERVED						ns	
6000C	18.000	17.666	54	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	tCK(AVG)	0.333	<0.357	0.333	<0.357	RESERVED				ns	
6000AN	14.000	14.000	42	tCK(AVG)	RESERVED								ns	
6400C	17.500	17.500	56	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	16.250	16.250	52	tCK(AVG)	0.312	<0.333	0.312	<0.333	RESERVED				ns	
6400AN	14.375	14.375	46	tCK(AVG)	0.312	<0.333	RESERVED						ns	
6800C	17.647	17.647	60	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	16.470	16.470	56	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	RESERVED		ns	
6800B	16.470	16.176	56	tCK(AVG)	0.294	<0.312	0.294	<0.312	RESERVED				ns	
6800AN	14.117	14.117	48	tCK(AVG)	RESERVED								ns	
7200C	17.777	17.500	64	tCK(AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200BN,B	16.111	16.111	58	tCK(AVG)	0.277	<0.294	0.277	<0.294	RESERVED				ns	
7200AN	14.444	14.444	52	tCK(AVG)	0.277	<0.294	RESERVED						ns	
7600C	17.894	17.631	68	tCK(AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	0.263	<0.277	ns	
7600BN	16.315	16.315	62	tCK(AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	RESERVED		ns	
7600B	16.315	16.052	62	tCK(AVG)	0.263	<0.277	0.263	<0.277	RESERVED				ns	
7600AN	14.210	14.210	54	tCK(AVG)	0.263	<0.277	RESERVED						ns	
Supported CL					22,24,26,28,30,32, 36,38,40,42,46,48, 50,52,54,56,58,60, 62,64,68		22,26,28,30,32,36, 40,42,46,48,50,52, 54,56,58,60,62,64, 68		22,28,30,32,36,40, 42,46,50,54,56,60, 62,64,68		22,28,32,36,40,42, 46,50,54,56,60,64, 68		nCK	12

10.13 DDR5-8000 Speed Bins and Operations

Table 295 — DDR5-8000 Speed Bins and Operations

Speed Bin					DDR5-8000AN		DDR5-8000B		DDR5-8000BN		DDR5-8000C		Unit	Note
CL-nRCD-nRP					56-56-56		64-64-64		64-64-64		70-70-70			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	14.000	-	16.000		16.000	-	17.500	-	ns	12
Activate to Read or Write command delay time				tRCD	14.000	-	16.000	-	16.000	-	17.500	-	ns	7
Row Precharge time				tRP	14.000	-	16.000	-	16.000	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7, 13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.000	-	48.000	-	48.000	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	RESERVED		ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	RESERVED		ns	
4000AN	14.000	14.000	28	tCK(AVG)	0.500	<0.555	RESERVED						ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	14.545	14.545	32	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800AN	14.166	14.166	34	tCK(AVG)	0.416	<0.454	RESERVED						ns	
5200C	17.692	17.692	46	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	RESERVED		ns	
5200AN	14.615	14.615	38	tCK(AVG)	0.384	<0.416	RESERVED						ns	
5600C	17.857	17.500	50	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600B	16.428	16.071	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600AN	14.285	14.285	40	tCK(AVG)	0.357	<0.384	RESERVED						ns	
6000C	18.000	17.666	54	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	RESERVED		ns	
6000AN	14.000	14.000	42	tCK(AVG)	0.333	<0.357	RESERVED						ns	
6400C	17.500	17.500	56	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	16.250	16.250	52	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	RESERVED		ns	
6400AN	14.375	14.375	46	tCK(AVG)	0.312	<0.333	RESERVED						ns	
6800C	17.647	17.647	60	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	16.470	16.470	56	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	RESERVED		ns	
6800B	16.470	16.176	56	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	RESERVED		ns	
6800AN	14.117	14.117	48	tCK(AVG)	0.294	<0.312	RESERVED						ns	
7200C	17.777	17.500	64	tCK(AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200BN,B	16.111	16.111	58	tCK(AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	RESERVED		ns	
7200AN	14.444	14.444	52	tCK(AVG)	0.277	<0.294	RESERVED						ns	
7600C	17.894	17.631	68	tCK(AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	0.263	<0.277	ns	
7600BN	16.315	16.315	62	tCK(AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	RESERVED		ns	
7600B	16.315	16.052	62	tCK(AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	RESERVED		ns	
7600AN	14.210	14.210	54	tCK(AVG)	0.263	<0.277	RESERVED						ns	
8000C	17.500	17.500	70	tCK(AVG)	0.250	<0.263	0.250	<0.263	0.250	<0.263	0.250	<0.263	ns	
8000BN,B	16.000	16.000	64	tCK(AVG)	0.250	<0.263	0.250	<0.263	0.250	<0.263	RESERVED		ns	
8000AN	14.000	14.000	56	tCK(AVG)	0.250	<0.263	RESERVED						ns	
Supported CL					22,24,26,28,30,32, 34,36,38,40,42,46, 48,50,52,54,56,58, 60,62,64,68,70		22,26,28,30,32,36, 40,42,46,48,50,52, 54,56,58,60,62,64, 68,70		22,26,28,30,32,36, 40,42,46,48,50,52, 54,56,58,60,62,64, 68,70		22,28,32,36,40,42, 46,50,54,56,60,64, 68,70		nCK	12

10.14 DDR5-8400 Speed Bins and Operations

Table 296 — DDR5-8400 Speed Bins and Operations

Speed Bin					DDR5-8400AN		DDR5-8400B		DDR5-8400BN		DDR5-8400C		Unit	Note
CL-nRCD-nRP					60-60-60		68-68-68		68-68-68		74-74-74			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	14.285	-	16.000	-	16.190	-	17.500	-	ns	12
Activate to Read or Write command delay time				tRCD	14.285	-	16.000	-	16.190	-	17.500	-	ns	7
Row Precharge time				tRP	14.285	-	16.000	-	16.190	-	17.500		ns	7
Activate to Precharge command period				tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7, 13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.285	-	48.000	-	48.190	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	RESERVED		ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED								ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	14.545	14.545	32	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800AN	14.166	14.166	34	tCK(AVG)	RESERVED								ns	
5200C	17.692	17.692	46	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	tCK(AVG)	0.384	<0.416	0.384	<0.416	RESERVED				ns	
5200AN	14.615	14.615	38	tCK(AVG)	0.384	<0.416	RESERVED						ns	
5600C	17.857	17.500	50	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600B	16.428	16.071	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600AN	14.285	14.285	40	tCK(AVG)	0.357	<0.384	RESERVED						ns	
6000C	18.000	17.666	54	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	tCK(AVG)	0.333	<0.357	0.333	<0.357	RESERVED				ns	
6000AN	14.000	14.000	42	tCK(AVG)	RESERVED								ns	
6400C	17.500	17.500	56	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	16.250	16.250	52	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	RESERVED		ns	
6400AN	14.375	14.375	46	tCK(AVG)	0.312	<0.333	RESERVED						ns	
6800C	17.647	17.647	60	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	16.470	16.470	56	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	RESERVED		ns	
6800B	16.470	16.176	56	tCK(AVG)	0.294	<0.312	0.294	<0.312	RESERVED				ns	
6800AN	14.117	14.117	48	tCK(AVG)	RESERVED								ns	
7200C	17.777	17.500	64	tCK(AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200BN,B	16.111	16.111	58	tCK(AVG)	0.277	<0.294	0.277	<0.294	RESERVED				ns	
7200AN	14.444	14.444	52	tCK(AVG)	0.277	<0.294	RESERVED						ns	
7600C	17.894	17.631	68	tCK(AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	0.263	<0.277	ns	
7600BN	16.315	16.315	62	tCK(AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	RESERVED		ns	
7600B	16.315	16.052	62	tCK(AVG)	0.263	<0.277	0.263	<0.277	RESERVED				ns	
7600AN	14.210	14.210	54	tCK(AVG)	RESERVED								ns	
8000C	17.500	17.500	70	tCK(AVG)	0.250	<0.263	0.250	<0.263	0.250	<0.263	0.250	<0.263	ns	
8000BN,B	16.000	16.000	64	tCK(AVG)	0.250	<0.263	0.250	<0.263	RESERVED				ns	
8000AN	14.000	14.000	56	tCK(AVG)	RESERVED								ns	
8400C	17.619	17.619	74	tCK(AVG)	0.238	<0.250	0.238	<0.250	0.238	<0.250	0.238	<0.250	ns	
8400BN,B	16.190	16.190	68	tCK(AVG)	0.238	<0.250	0.238	<0.250	0.238	<0.250	RESERVED		ns	
8400AN	14.285	14.285	60	tCK(AVG)	0.238	<0.250	RESERVED						ns	
Supported CL					22,24,26,28,30,32, 36,38,40,42,46,48, 50,52,54,56,58,60, 62,64,68,70,74		22,26,28,30,32,36, 40,42,46,48,50,52, 54,56,58,60,62,64, 68,70,74		22,26,28,30,32,36, 40,42,46,50,52,54, 56,60,62,64,68,70, 74		22,28,32,36,40,42, 46,50,54,56,60,64, 68,70,74		nCK	12

10.15 DDR5-8800 Speed Bins and Operations

Table 297 — DDR5-8800 Speed Bins and Operations

Speed Bin					DDR5-8800AN		DDR5-8800B		DDR5-8800BN		DDR5-8800C		Unit	Note
CL-nRCD-nRP					62-62-62		72-71-71		72-72-72		78-77-77			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	14.090	-	16.000	-	16.363	-	17.500	-	ns	12
Activate to Read or Write command delay time				tRCD	14.090	-	16.000	-	16.363	-	17.500	-	ns	7
Row Precharge time				tRP	14.090	-	16.000	-	16.363	-	17.500		ns	7
Activate to Precharge command period				tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7, 13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.090	-	48.000	-	48.363	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED								ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	14.545	14.545	32	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	14.166	14.166	34	tCK(AVG)	0.416	<0.454	RESERVED						ns	
5200C	17.692	17.692	46	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	tCK(AVG)	0.384	<0.416	0.384	<0.416	RESERVED				ns	
5200AN	14.615	14.615	38	tCK(AVG)	0.384	<0.416	RESERVED						ns	
5600C	17.857	17.500	50	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600B	16.428	16.071	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600AN	14.285	14.285	40	tCK(AVG)	0.357	<0.384	RESERVED						ns	
6000C	18.000	17.666	54	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	tCK(AVG)	0.333	<0.357	0.333	<0.357	RESERVED				ns	
6000AN	14.000	14.000	42	tCK(AVG)	RESERVED								ns	
6400C	17.500	17.500	56	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	16.250	16.250	52	tCK(AVG)	0.312	<0.333	0.312	<0.333	RESERVED				ns	
6400AN	14.375	14.375	46	tCK(AVG)	0.312	<0.333	RESERVED						ns	
6800C	17.647	17.647	60	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	16.470	16.470	56	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	RESERVED		ns	
6800B	16.470	16.176	56	tCK(AVG)	0.294	<0.312	0.294	<0.312	RESERVED				ns	
6800AN	14.117	14.117	48	tCK(AVG)	0.294	<0.312	RESERVED						ns	
7200C	17.777	17.500	64	tCK(AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200BN,B	16.111	16.111	58	tCK(AVG)	0.277	<0.294	0.277	<0.294	RESERVED				ns	
7200AN	14.444	14.444	52	tCK(AVG)	0.277	<0.294	RESERVED						ns	
7600C	17.894	17.631	68	tCK(AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	0.263	<0.277	ns	

Table 297 — DDR5-8800 Speed Bins and Operations (cont'd)

7600BN	16.315	16.315	62	tCK(AVG)	0.263	<0.277	0.263	<0.277	RESERVED						ns	
7600B	16.315	16.052	62	tCK(AVG)	0.263	<0.277	0.263	<0.277	RESERVED						ns	
7600AN	14.210	14.210	54	tCK(AVG)	0.263	<0.277	RESERVED								ns	
8000C	17.500	17.500	70	tCK(AVG)	0.250	<0.263	0.250	<0.263	0.250	<0.263	0.250	<0.263			ns	
8000BN,B	16.000	16.000	64	tCK(AVG)	0.250	<0.263	0.250	<0.263	RESERVED						ns	
8000AN	14.000	14.000	56	tCK(AVG)	RESERVED										ns	
8400C	17.619	17.619	74	tCK(AVG)	0.238	<0.250	0.238	<0.250	0.238	<0.250	0.238	<0.250			ns	
8400BN,B	16.190	16.190	68	tCK(AVG)	0.238	<0.250	0.238	<0.250	RESERVED						ns	
8400AN	14.285	14.285	60	tCK(AVG)	0.238	<0.250	RESERVED								ns	
8800C	17.727	17.500	78	tCK(AVG)	0.227	<0.238	0.227	<0.238	0.227	<0.238	0.227	<0.238			ns	
8800BN	16.363	16.363	72	tCK(AVG)	0.227	<0.238	0.227	<0.238	0.227	<0.238	RESERVED				ns	
8800B	16.363	16.136	72	tCK(AVG)	0.227	<0.238	0.227	<0.238	RESERVED						ns	
8800AN	14.090	14.090	62	tCK(AVG)	0.227	<0.238	RESERVED								ns	
Supported CL					22,24,26,28,30,32, 34,36,38,40,42,46, 48,50,52,54,56,58, 60,62,64,68,70,72, 74,78		22,26,28,30,32,36, 40,42,46,48,50,52, 54,56,58,60,62,64, 68,70,72,74,78		22,28,30,32,36,40, 42,46,50,54,56,60, 64,68,70,72,74,78		22,28,32,36,40,42, 46,50,54,56,60,64, 68,70,74,78				nCK	12

10.16 DDR5-9200 Speed Bins and Operations

Table 298 — DDR5-9200 Speed Bins and Operations

Speed Bin					DDR5-9200AN		DDR5-9200B		DDR5-9200BN		DDR5-9200C		Unit	Note
CL-nRCD-nRP					66-66-66		74-74-74		74-74-74		82-81-81			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	14.347	22.222	16.000	22.222	16.086	22.222	17.500	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.347	-	16.000	-	16.086	-	17.500	-	ns	7
Row Precharge time				tRP	14.347	-	16.000	-	16.086	-	17.500		ns	7
Activate to Precharge command period				tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7, 13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.347	-	48.000	-	48.086	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED								ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	14.545	14.545	32	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	14.166	14.166	34	tCK(AVG)	0.416	<0.454	RESERVED						ns	
5200C	17.692	17.692	46	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	tCK(AVG)	0.384	<0.416	0.384	<0.416	RESERVED				ns	
5200AN	14.615	14.615	38	tCK(AVG)	0.384	<0.416	RESERVED						ns	
5600C	17.857	17.500	50	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600B	16.428	16.071	46	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600AN	14.285	14.285	40	tCK(AVG)	0.357	<0.384	RESERVED						ns	
6000C	18.000	17.666	54	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	tCK(AVG)	0.333	<0.357	0.333	<0.357	RESERVED				ns	
6000AN	14.000	14.000	42	tCK(AVG)	RESERVED								ns	
6400C	17.500	17.500	56	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	16.250	16.250	52	tCK(AVG)	0.312	<0.333	0.312	<0.333	RESERVED				ns	
6400AN	14.375	14.375	46	tCK(AVG)	0.312	<0.333	RESERVED						ns	
6800C	17.647	17.647	60	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	16.470	16.470	56	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	RESERVED		ns	
6800B	16.470	16.176	56	tCK(AVG)	0.294	<0.312	0.294	<0.312	RESERVED				ns	
6800AN	14.117	14.117	48	tCK(AVG)	0.294	<0.312	RESERVED						ns	
7200C	17.777	17.500	64	tCK(AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200BN,B	16.111	16.111	58	tCK(AVG)	0.277	<0.294	0.277	<0.294	RESERVED				ns	
7200AN	14.444	14.444	52	tCK(AVG)	0.277	<0.294	RESERVED						ns	
7600C	17.894	17.631	68	tCK(AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	0.263	<0.277	ns	

Table 298 — DDR5-9200 Speed Bins and Operations (cont'd)

7600BN	16.315	16.315	62	tCK(AVG)	0.263	<0.277	0.263	<0.277	RESERVED						ns	
7600B	16.315	16.052	62	tCK(AVG)	0.263	<0.277	0.263	<0.277	RESERVED						ns	
7600AN	14.210	14.210	54	tCK(AVG)	0.263	<0.277	RESERVED								ns	
8000C	17.500	17.500	70	tCK(AVG)	0.250	<0.263	0.250	<0.263	0.250	<0.263	0.250	<0.263			ns	
8000BN,B	16.000	16.000	64	tCK(AVG)	0.250	<0.263	0.250	<0.263	RESERVED						ns	
8000AN	14.000	14.000	56	tCK(AVG)	RESERVED										ns	
8400C	17.619	17.619	74	tCK(AVG)	0.238	<0.250	0.238	<0.250	0.238	<0.250	0.238	<0.250			ns	
8400BN,B	16.190	16.190	68	tCK(AVG)	0.238	<0.250	0.238	<0.250	RESERVED						ns	
8400AN	14.285	14.285	60	tCK(AVG)	0.238	<0.250	RESERVED								ns	
8800C	17.727	17.500	78	tCK(AVG)	0.227	<0.238	0.227	<0.238	0.227	<0.238	0.227	<0.238			ns	
8800BN	16.363	16.363	72	tCK(AVG)	0.227	<0.238	0.227	<0.238	0.227	<0.238	RESERVED				ns	
8800B	16.363	16.136	72	tCK(AVG)	0.227	<0.238	0.227	<0.238	RESERVED						ns	
8800AN	14.090	14.090	62	tCK(AVG)	0.227	<0.238	RESERVED								ns	
9200C	17.826	17.608	82	tCK(AVG)	0.217	<0.227	0.217	<0.227	0.217	<0.227	0.217	<0.227			ns	
9200BN,B	16.086	16.086	74	tCK(AVG)	0.217	<0.227	0.217	<0.227	0.217	<0.227	RESERVED				ns	
9200AN	14.347	14.347	66	tCK(AVG)	0.217	<0.227	RESERVED								ns	
Supported CL					22,24,26,28,30,32, 34,36,38,40,42,46, 48,50,52,54,56,58, 60,62,64,68,70,72, 74,78,82		22,26,28,30,32,36, 40,42,46,48,50,52, 54,56,58,60,62,64, 68,70,72,74,78,82		22,28,30,32,36,40, 42,46,50,54,56,60, 64,68,70,72,74,78,82		22,28,32,36,40,42, 46,50,54,56,60,64, 68,70,74,78,82				nCK	12

DDR5 Speed Bin Table Notes:

1. Minimum timing parameters are defined according to the rules in the Rounding Definitions and Algorithms section.
2. The translation of all timing parameters from ns values to nCK values shall follow the Rounding Algorithm. The translation of tAA to CL shall follow the explicit combinations listed in the Speed Bin Tables.
3. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When selecting tCK(avg), requirements from the CL setting as well as requirements from the CWL setting shall be fulfilled.
4. 'Reserved' settings are not allowed. The user shall program a different value.
5. This column shows the intended native speed bin timings to be replaced and supported when down clocking. This column does not necessarily show the actual minimum speed bin timings allowed and supported when down clocking because the timings could be faster according to the Rounding Algorithm, depending on the specific speed bin and down clock frequency combination.
6. DDR5-3200 AC timings apply if the DRAM operates slower than the 2933 MT/s data rate. This is not limited to only the Speed Bin Table timings.
7. Parameters apply from tCK(avg)min to tCK(avg)max.
8. tRC(min) shall always be greater than or equal to tRAS(min) + tRP(min), and when using the appropriate rounding algorithms, nRC(min) shall always be greater than or equal to nRAS(min) + nRP(min).
9. tCK(avg).max of 1.010 ns (1980 MT/s data rate) is defined to allow for 1% SSC down-spreading at a data rate of 2000 MT/s according to JESD404-1.
10. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC standard. The JEDEC standard does not require support for all speed bins within a given speed. The JEDEC standard requires meeting the parameters for a least one of the listed speed bins.
11. Any speed bin also supports functional operation at slower frequencies as shown in the table which are not subject to Production Tests but are verified by Design/Characterization.
12. The CL Algorithm can be used to mathematically determine the valid CAS Latencies listed in the Speed Bin Tables. The CL Algorithm calculates supported CAS Latencies by rounding the operating frequency up to the next faster native speed bin (i.e., 3200 MT/s, 3600 MT/s...). Using the resulting tCK(AVG)min, and the bin target timings, the CL Algorithm then uses the Rounding Algorithm to calculate the valid CAS Latency. Because the DDR5 SDRAM specification only supports even CAS Latencies, odd CAS Latencies are rounded up to the next even CAS Latency. The 1980-2100 MT/s data rate always uses CL22. If tAA (corrected) or tRCDtRP(corrected) are violated, the CL Algorithm uses a slower combination of tAA(target) and tRCDtRP(target) to return slower valid CAS Latencies. The DDR5 SDRAM can support up to four valid CAS Latencies, CL(AN), CL(B), CL(BN), and CL(C), for a given frequency. tAA(corrected) and tRCDtRP(corrected) are calculated by reducing tAA(min), tRCD(min), and tRP(min) by the Rounding Algorithm correction factor. The proper setting of CL shall be determined by the memory controller, either by using the Speed Bin Tables, or by using the CL Algorithm, or by some other means. Refer to the Rounding Definitions and Algorithm section for more information. When Read CRC is enabled, CL is increased according to the Read CRC Latency Adder. When Write CRC is enabled, there is no Write CRC Latency Adder.

DDR5 Speed Bin Table Notes: (cont'd)

```
// Variables already defined in other areas of the DDR5 SDRAM specification
CorrFact       = 0.30                                          // (%)   Rounding Algorithm correction factor
ScaledCorrFact = 997                                           //       Scaled correction factor (1000*(1-0.30%))
tCKreal        =1011-952, 682-217                             // (ps)  Real application tCK(AVG) (1980-2100MT/s, 2933-9200MT/s)
tAAmin         MONO=14000-17500, 3DS=16000-20000               // (ps)  From Speed Bin Tables and DIMM SPD bytes 30-31
tRCDtRPmin     MONO=14000-17500, 3DS=14000-17500               // (ps)  From Speed Bin Tables and DIMM SPD bytes 32-33 (tRCD=tRP)
tAAcorr        = TRUNC(tAAmin*ScaledCorrFactor/1000)           // (ps)  Corrected tAA(min) per the Rounding Algorithm rules
tRCDtRPcorr    = TRUNC(tRCDtRPmin*ScaledCorrFactor/1000)       // (ps)  Corrected tRCD(min), tRP(min) per the Rounding Algorithm
FUNC[RA(targ)] = TRUNC((targ*ScaledCorrFact/tCKstd+1000)/1000) // (nCK) Use Rounding Algorithm to convert bin target timing to nCK

// Round tCKreal down to the next faster standard frequency (tCK in ps)
IF (TRUNC(2000000/(2000*99%))>=TRUNC(tCKreal)>=TRUNC(2000000/(2000*105%)))            // Check for  1980-2100 nominal data rates
   tCKstd=TRUNC(2000000/2000)                                                         // Assign standard 2000 tCK (ps)
ELSE IF (TRUNC(2000000/(2000+7*(133+1/3)))>=TRUNC(tCKreal)>=TRUNC(2000000/3200))      // Check for  2933-3200 nominal data rates
   tCKstd=TRUNC(2000000/3200)                                                         // Assign standard 3200 tCK (ps)
ELSE
   FOR (DataRateNom=3200; DataRateNom<=9200; DataRateNom=DataRateNom+400)             // Check for >3200-9200 nominal data rates
      IF (TRUNC(2000000/DataRateNom)>TRUNC(tCKreal)>=TRUNC(2000000/(DataRateNom+400)))
         tCKstd=TRUNC(2000000/(DataRateNom+400))                                      // Assign standard 3600-9200 tCK (ps)
      ELSE
         tCKstd=RESERVED                                                              // No valid data rate found

// Timing targets (ps) that have been used to define the Speed Bin Tables
// MONO targets            3DS targets
   BinAN_tAAtarg     = 14000 BinAN_tAAtarg     = 16000         // tAA target for AN bins
   BinB__tAAtarg     = 16000 BinB__tAAtarg     = 18500         // tAA target for AN, B bins
   BinBN_tAAtarg     = 16000 BinBN_tAAtarg     = 18500         // tAA target for AN, B, BN bins
   BinC__tAAtarg     = 17500 BinC__tAAtarg     = 20000         // tAA target for AN, B, BN, C bins
   BinAN_tRCDtRPtarg = 14000 BinAN_tRCDtRPtarg = 14000         // tRCD, tRP target for AN bins
   BinBN_tRCDtRPtarg = 16000 BinBN_tRCDtRPtarg = 16000         // tRCD, tRP target for AN, B, BN bins
   BinC__tRCDtRPtarg = 17500 BinC__tRCDtRPtarg = 17500         // tRCD, tRP target for AN, B, BN, C bins
IF (TRUNC(2000000/3600)>tCKstd)                                // tRCD, tRP target for B bins is frequency dependent
   BinB__tRCDtRPtarg = 16000 BinB__tRCDtRPtarg = 16000         // tRCD, tRP target for AN, B bins data rates faster than 3600
ELSE
   // 16250=(2000000/3200)*EVEN(TRUNC((BinB__tRCDtRPtarg*ScaledCorrFact/(2000000/3200)+1000)/1000))
   BinB__tRCDtRPtarg = 16250 BinB__tRCDtRPtarg = 16250         // tRCD, tRP target for AN, B bins for data rates 3600 and slower

// CL Algorithm using variables defined above
// Up to four valid CL's can be returned for a specific freq: CL(AN), CL(B), CL(BN), CL(C), depending on tAAmin, tRCDmin, tRPmin
// The B and BN bins return the same CL
// Only even CL's (not odd CL's) are valid per the DDR5 SDRAM specification
// nRCD, nRP are only even at standard native frequencies for the AN, BN bins (can be even or odd at intermediate frequencies)
// nRCD, nRP may be even or odd at standard native frequencies for the B, C bins (can be even or odd at intermediate frequencies)
IF (TRUNC(2000000/2000)=tCKstd)                                // CL22 is the only valid CL for 1980-2100 data rates
   CL(AN)=22                                                   // Valid even CL for AN bins
   CL(B )=22                                                   // Valid even CL for AN, B, bins
   CL(BN)=22                                                   // Valid even CL for AN, B, BN bins
   CL(C )=22                                                   // Valid even CL for AN, B, BN, C bins
ELSE IF (TRUNC(2000000/3200)>=tCKstd>=TRUNC(2000000/8800))     // Valid CL for 2933-9200 data rates
   IF      ((EVEN(RA(BinAN_tAAtarg))*tCKstd>=tAAcorr)AND(EVEN(RA(BinAN_tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even only
      CL(AN)=EVEN(RA(BinAN_tAAtarg))                           // Valid even CL for AN bins
      CL(B )=EVEN(RA(BinB__tAAtarg))                           // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                           // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                           // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinB__tAAtarg))*tCKstd>=tAAcorr)AND(    (RA(BinB__tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even, odd
      CL(AN)=RESERVED                                          // Valid even CL for AN bins
      CL(B )=EVEN(RA(BinB__tAAtarg))                           // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                           // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                           // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinBN_tAAtarg))*tCKstd>=tAAcorr)AND(EVEN(RA(BinBN_tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even only
      CL(AN)=RESERVED                                          // Valid even CL for AN bins
      CL(B )=RESERVED                                          // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                           // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                           // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinC__tAAtarg))*tCKstd>=tAAcorr)AND(    (RA(BinC__tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even, odd
      CL(AN)=RESERVED                                          // Valid even CL for AN bins
      CL(B )=RESERVED                                          // Valid even CL for AN, B bins
      CL(BN)=RESERVED                                          // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                           // Valid even CL for AN, B, BN, C bins
   ELSE                                                        // No valid CL found (tAAmin, tRCDmin, tRPmin are too slow)
      CL(AN)=RESERVED                                          // Valid even CL for AN bins
      CL(B )=RESERVED                                          // Valid even CL for AN, B bins
      CL(BN)=RESERVED                                          // Valid even CL for AN, B, BN bins
      CL(C )=RESERVED                                          // Valid even CL for AN, B, BN, C bins
ELSE                                                           // No valid data rate found
   CL(AN)=RESERVED                                             // Valid even CL for AN bins
   CL(B )=RESERVED                                             // Valid even CL for AN, B bins
   CL(BN)=RESERVED                                             // Valid even CL for AN, B, BN bins
   CL(C )=RESERVED                                             // Valid even CL for AN, B, BN, C bins
```

13. tRAS(max) shall always be less than or equal to 5*tREFI1(max) during Normal Refresh Mode and less than or equal to 9*tREFI2(max) during Fine Granularity Refresh Mode, and when using the rounding algorithms, nRAS(max) shall always be less than or equal to 5*nREFI1(max) during Normal Refresh Mode and less than or equal to 9*nREFI2(max) during Fine Granularity Refresh Mode.

10.17 3DS DDR5-3200 Speed Bins and Operations

Table 299 — 3DS DDR5-3200 Speed Bins and Operations

Speed Bin				DDR5-3200AN 3DS		DDR5-3200B 3DS		DDR5-3200BN 3DS		DDR5-3200C 3DS		Unit	NOTE
CL-nRCD-nRP				26-24-24		30-26-26		30-26-26		32-28-28			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data			tAA	16.250	22.222	18.750	22.222	18.750	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time			tRCD	15.000	-	16.250	-	16.250	-	17.500	-	ns	7
Row Precharge time			tRP	15.000	-	16.250	-	16.250	-	17.500	-	ns	7
Activate to Precharge command period			tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7
Activate to Activate or Refresh command period			tRC (tRAS +tRP)	47.000	-	48.250	-	48.250	-	49.500	-	ns	7,8
CAS Write Latency			CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins									
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	RESERVED		ns	
3200AN	16.250	15.000	26	tCK(AVG)	0.625	0.681	RESERVED						ns	
Supported CL					22,26,30,32		22,30,32		22,30,32		22,32		nCK	12

10.18 3DS DDR5-3600 Speed Bins and Operations

Table 300 — 3DS DDR5-3600 Speed Bins and Operations

Speed Bin				DDR5-3600AN 3DS		DDR5-3600B 3DS		DDR5-3600BN 3DS		DDR5-3600C 3DS		Unit	NOTE
CL-nRCD-nRP				30-26-26		34-30-30		34-30-30		36-32-32			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data			tAA	16.666	22.222	18.750	22.222	18.888	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time			tRCD	14.444	-	16.250	-	16.666	-	17.500	-	ns	7
Row Precharge time			tRP	14.444	-	16.250	-	16.666	-	17.500	-	ns	7
Activate to Precharge command period			tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period			tRC (tRAS +tRP)	46.444	-	48.250	-	48.666	-	49.500	-	ns	7, 8
CAS Write Latency			CWL	CL-2								nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins									
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	16.250	15.000	26	tCK(AVG)	RESERVED								ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	16.666	14.444	30	tCK(AVG)	0.555	<0.625	RESERVED						ns	
Supported CL					22,30,32,34,36		22,30,32,34,36		22,32,34,36		22,32,36		nCK	

10.19 3DS DDR5-4000 Speed Bins and Operations

Table 301 — 3DS DDR5-4000 Speed Bins and Operations

Speed Bin					DDR5-4000AN 3DS		DDR5-4000B 3DS		DDR5-4000BN 3DS		DDR5-4000C 3DS		Unit	NOTE
CL-nRCD-nRP					32-28-28		38-32-32		38-32-32		40-35-35			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	16.000	22.222	18.750	22.222	19.000	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.000	-	16.000	-	16.000	-	17.500	-	ns	7
Row Precharge time				tRP	14.000	-	16.000	-	16.000	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.000	-	48.000	-	48.000	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	16.250	15.000	26	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	RESERVED				ns	
3600AN	16.666	14.444	30	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	RESERVED		ns	
4000AN	16.000	14.000	32	tCK(AVG)	0.500	<0.555	RESERVED						ns	
Supported CL					22,26,30,32,34,36,38, 40		22,30,32,34,36,38, 40		22,32,36,38,40		22,32,36,40		nCK	

10.20 3DS DDR5-4400 Speed Bins and Operations

Table 302 — 3DS DDR5-4400 Speed Bins and Operations

Speed Bin					DDR5-4400AN 3DS		DDR5-4400B 3DS		DDR5-4400BN 3DS		DDR5-4400C 3DS		Unit	NOTE
CL-nRCD-nRP					36-32-32		42-36-36		42-36-36		44-39-39			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	16.363	22.222	18.750	22.222	19.090	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.545	-	16.000	-	16.363	-	17.500	-	ns	7
Row Precharge time				tRP	14.545	-	16.000	-	16.363	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.545	-	48.000	-	48.363	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	16.250	15.000	26	tCK(AVG)	RESERVED								ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	RESERVED				ns	
3600AN	16.666	14.444	30	tCK(AVG)	RESERVED								ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	16.000	14.000	32	tCK(AVG)	RESERVED								ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	16.363	14.545	36	tCK(AVG)	0.454	<0.500	RESERVED						ns	
Supported CL					22,30,32,34,36,38,40, 42,44		22,30,32,34,36,38,40, 42,44		22,32,36,40,42,44		22,32,36,40,44		nCK	

10.21 3DS DDR5-4800 Speed Bins and Operations

Table 303 — 3DS DDR5-4800 Speed Bins and Operations

Speed Bin					DDR5-4800AN 3DS		DDR5-4800B 3DS		DDR5-4800BN 3DS		DDR5-4800C 3DS		Unit	NOTE
CL-nRCD-nRP					40-34-34		46-39-39		46-40-40		48-42-42			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	16.666	22.222	18.750	22.222	19.166	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.166	-	16.000	-	16.666	-	17.500	-	ns	7
Row Precharge time				tRP	14.166	-	16.000	-	16.666	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.166	-	48.000	-	48.666	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	16.250	15.000	26	tCK(AVG)	RESERVED								ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	RESERVED				ns	
3600AN	16.666	14.444	30	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	16.000	14.000	32	tCK(AVG)	RESERVED								ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	0.454	<0.500	RESERVED				ns	
4400AN	16.363	14.545	36	tCK(AVG)	RESERVED								ns	
4800C	20.000	17.500	48	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	19.166	16.250	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	16.666	14.166	40	tCK(AVG)	0.416	<0.454	RESERVED						ns	
Supported CL					22,30,32,34,36,38,40, 42,44,46,48		22,30,32,34,36,38,40, 42,44,46,48		22,32,36,40,44,46,48		22,32,36,40,44,48		nCK	

10.22 3DS DDR5-5200 Speed Bins and Operations

Table 304 — 3DS DDR5-5200 Speed Bins and Operations

Speed Bin					DDR5-5200AN 3DS		DDR5-5200B 3DS		DDR5-5200BN 3DS		DDR5-5200C 3DS		Unit	NOTE
CL-nRCD-nRP					42-38-38		50-42-42		50-42-42		52-46-46			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	16.153	22.222	18.750	22.222	19.230	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.615	-	16.000	-	16.153	-	17.500	-	ns	7
Row Precharge time				tRP	14.615	-	16.000	-	16.153	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.615	-	48.000	-	48.153	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	16.250	15.000	26	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	RESERVED				ns	
3600AN	16.666	14.444	30	tCK(AVG)	RESERVED								ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	16.000	14.000	32	tCK(AVG)	RESERVED								ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	0.454	<0.500	RESERVED				ns	
4400AN	16.363	14.545	36	tCK(AVG)	RESERVED								ns	
4800C	20.000	17.500	48	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800B	19.166	16.250	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	16.666	14.166	40	tCK(AVG)	RESERVED								ns	
5200C	20.000	17.692	52	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	50	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	RESERVED		ns	
5200AN	16.153	14.615	42	tCK(AVG)	0.384	<0.416	RESERVED						ns	
Supported CL					22,26,30,32,34,36,38, 40,42,44,46,48,50,52		22,30,32,34,36,38, 40,42,44,46,48,50,52		22,32,36,40,44,48,50, 52		22,32,36,40,44,48,52		nCK	

10.23 3DS DDR5-5600 Speed Bins and Operations

Table 305 — 3DS DDR5-5600 Speed Bins and Operations

Speed Bin					DDR5-5600AN 3DS		DDR5-5600B 3DS		DDR5-5600BN 3DS		DDR5-5600C 3DS		Unit	NOTE
CL-nRCD-nRP					46-40-40		52-45-45		52-46-46		56-49-49			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	16.428	22.222	18.571	22.222	18.571	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.285	-	16.000	-	16.428	-	17.500	-	ns	7
Row Precharge time				tRP	14.285	-	16.000	-	16.4228	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.285	-	48.000	-	48.428	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	16.250	15.000	26	tCK(AVG)	RESERVED								ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	16.666	14.444	30	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	16.000	14.000	32	tCK(AVG)	RESERVED								ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	0.454	<0.500	RESERVED				ns	
4400AN	16.363	14.545	36	tCK(AVG)	RESERVED								ns	
4800C	20.000	17.500	48	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	19.166	16.250	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	16.666	14.166	40	tCK(AVG)	RESERVED								ns	
5200C	20.000	17.692	52	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	50	tCK(AVG)	0.384	<0.416	0.384	<0.416	RESERVED				ns	
5200AN	16.153	14.615	42	tCK(AVG)	RESERVED								ns	
5600C	20.000	17.500	56	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600B	18.571	16.071	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600AN	16.428	14.285	46	tCK(AVG)	0.357	<0.384	RESERVED						ns	
Supported CL					22,30,32,34,36,38,40, 42,44,46,48,50,52,56		22,30,32,34,36,38,40, 42,44,46,48,50,52,56		22,32,34,36,40,44,46, 48,52,56		22,32,36,40,44,48,52, 56		nCK	

10.24 3DS DDR5-6000 Speed Bins and Operations

Table 306 — 3DS DDR5-6000 Speed Bins and Operations

Speed Bin					DDR5-6000AN 3DS		DDR5-6000B 3DS		DDR5-6000BN 3DS		DDR5-6000C 3DS		Unit	NOTE
CL-nRCD-nRP					48-42-42		56-48-48		56-48-48		60-53-53			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	16.000	22.222	18.571	22.222	18.666	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.000	-	16.000	-	16.000	-	17.500	-	ns	7
Row Precharge time				tRP	14.000	-	16.000	-	16.000	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.000	-	48.000	-	48.000	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	<0.681	RESERVED		ns	
3200AN	16.250	15.000	26	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	16.666	14.444	30	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	RESERVED		ns	
4000AN	16.000	14.000	32	tCK(AVG)	0.500	<0.555	RESERVED						ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	16.363	14.545	36	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	20.000	17.500	48	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	19.166	16.250	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800AN	16.666	14.166	40	tCK(AVG)	0.416	<0.454	RESERVED						ns	
5200C	20.000	17.692	52	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	50	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	RESERVED		ns	
5200AN	16.153	14.615	42	tCK(AVG)	0.384	<0.416	RESERVED						ns	
5600C	20.000	17.500	56	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600B	18.571	16.071	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600AN	16.428	14.285	46	tCK(AVG)	0.357	<0.384	RESERVED						ns	
6000C	20.000	17.666	60	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	18.666	16.000	56	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	RESERVED		ns	
6000AN	16.600	14.000	48	tCK(AVG)	0.333	<0.357	RESERVED						ns	
Supported CL					22,26,30,32,34,36,38, 40,42,44,46,48,50,52, 56,60		22,30,32,34,36,38,40, 42,44,46,48),50,52,56, 60		22,30,32,34,36,38,40, 42,44,46,48,50,52,56, 60		22,32,36,40,44,48,52, 56,60		nCK	

10.25 3DS DDR5-6400 Speed Bins and Operations

Table 307 — 3DS DDR5-6400 Speed Bins and Operations

Speed Bin					DDR5-6400AN 3DS		DDR5-6400B 3DS		DDR5-6400BN 3DS		DDR5-6400C 3DS		Unit	NOTE
CL-nRCD-nRP					52-46-46		60-52-52		60-52-52		64-56-56			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	16.250	22.222	18.571	22.222	18.750	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.375	-	16.000	-	16.250	-	17.500	-	ns	7
Row Precharge time				tRP	14.375	-	16.000	-	16.250	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.375	-	48.000	-	48.250	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	RESERVED		ns	
3200AN	16.250	15.000	26	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	16.666	14.444	30	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	16.000	14.000	32	tCK(AVG)	RESERVED								ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	16.363	14.545	36	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	20.000	17.500	48	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	19.166	16.250	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800AN	16.666	14.166	40	tCK(AVG)	RESERVED								ns	
5200C	20.000	17.692	52	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	50	tCK(AVG)	0.384	<0.416	0.384	<0.416	RESERVED				ns	
5200AN	16.153	14.615	42	tCK(AVG)	RESERVED								ns	
5600C	20.000	17.500	56	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600B	18.571	16.071	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600AN	16.428	14.285	46	tCK(AVG)	RESERVED								ns	
6000C	20.000	17.666	60	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	18.666	16.000	56	tCK(AVG)	0.333	<0.357	0.333	<0.357	RESERVED				ns	
6000AN	16.600	14.000	48	tCK(AVG)	RESERVED								ns	
6400C	20.000	17.500	64	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	18.750	16.250	60	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	RESERVED		ns	
6400AN	16.250	14.375	52	tCK(AVG)	0.312	<0.333	RESERVED						ns	
Supported CL					22,26,30,32,34,36,38, 40,42,44,46,48,50,52, 56,60,64		22,30,32,34,36,38,40, 42,44,46,48,50,52,56, 60,64		22,30,32,34,36,40,42, 44,46,48,52,56,60,64		22,32,36,40,44,48,52, 56,60,64		nCK	

10.26 3DS DDR5-6800 Speed Bins and Operations

Table 308 — 3DS DDR5-6800 Speed Bins and Operations

Speed Bin					DDR5-6800AN 3DS		DDR5-6800B 3DS		DDR5-6800BN 3DS		DDR5-6800C 3DS		Unit	Note
CL-nRCD-nRP					56-48-48		64-55-55		64-56-56		68-60-60			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	16.470	22.222	18.571	22.222	18.823	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.117	-	16.000	-	16.470	-	17.500	-	ns	7
Row Precharge time				tRP	14.117	-	16.000	-	16.470	-	17.500		ns	7
Activate to Precharge command period				tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7, 13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.117	-	48.000	-	48.000		49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	16.250	15.000	26	tCK(AVG)	RESERVED								ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	16.666	14.444	30	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	16.000	14.000	32	tCK(AVG)	RESERVED								ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	0.454	<0.500	RESERVED				ns	
4400AN	16.363	14.545	36	tCK(AVG)	RESERVED								ns	
4800C	20.000	17.500	48	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	19.166	16.250	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	16.666	14.166	40	tCK(AVG)	0.416	<0.454	RESERVED						ns	
5200C	20.000	17.692	52	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	50	tCK(AVG)	0.384	<0.416	0.384	<0.416	RESERVED				ns	
5200AN	16.153	14.615	42	tCK(AVG)	RESERVED								ns	
5600C	20.000	17.500	56	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600B	18.571	16.071	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600AN	16.428	14.285	46	tCK(AVG)	RESERVED								ns	
6000C	20.000	17.666	60	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	18.666	16.000	56	tCK(AVG)	0.333	<0.357	0.333	<0.357	RESERVED				ns	
6000AN	16.000	14.000	48	tCK(AVG)	RESERVED								ns	
6400C	20.000	17.500	64	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	18.750	16.250	60	tCK(AVG)	0.312	<0.333	0.312	<0.333	RESERVED				ns	
6400AN	16.250	14.375	52	tCK(AVG)	RESERVED								ns	
6800C	20.000	17.647	68	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	18.823	16.470	64	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	RESERVED		ns	
6800B	18.823	16.176	64	tCK(AVG)	0.294	<0.312	0.294	<0.312	RESERVED				ns	
6800AN	16.470	14.117	56	tCK(AVG)	0.294	<0.312	RESERVED						ns	
Supported CL					22,30,32,34,36,38, 40,42,44,46,48,50, 52,56,60,64,68		22,30,32,34,36,38, 40,42,44,46,48,50, 52,56,60,64,68		22,32,34,36,40,44, 46,48,56,60,64, 68		22,32,36,40,44,48, 52,56,60,64,68		nCK	12

10.27 3DS DDR5-7200 Speed Bins and Operations

Table 309 — 3DS DDR5-7200 Speed Bins and Operations

Speed Bin					DDR5-7200AN 3DS		DDR5-7200B 3DS		DDR5-7200BN 3DS		DDR5-7200C 3DS		Unit	Note
CL-nRCD-nRP					58-52-52		68-58-58		68-58-58		72-63-63			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	16.111	22.222	18.571	22.222	18.888	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.444	-	16.000	-	16.111	-	17.500	-	ns	7
Row Precharge Ttime				tRP	14.444	-	16.000	-	16.111	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7,13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.444	-	48.000	-	48.111	-	49.500	-	ns	7,8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	16.250	15.000	26	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	16.666	14.444	30	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	16.000	14.000	32	tCK(AVG)	RESERVED								ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	16.363	14.545	36	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	20.000	17.500	48	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	19.166	16.250	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800AN	16.666	14.166	40	tCK(AVG)	RESERVED								ns	
5200C	20.000	17.692	52	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	50	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	RESERVED		ns	
5200AN	16.153	14.615	42	tCK(AVG)	0.384	<0.416	RESERVED						ns	
5600C	20.000	17.500	56	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600B	18.571	16.071	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600AN	16.428	14.285	46	tCK(AVG)	RESERVED								ns	
6000C	20.000	17.666	60	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	18.666	16.000	56	tCK(AVG)	0.333	<0.357	0.333	<0.357	RESERVED				ns	
6000AN	16.000	14.000	48	tCK(AVG)	RESERVED								ns	
6400C	20.000	17.500	64	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	18.750	16.250	60	tCK(AVG)	0.312	<0.333	0.312	<0.333	RESERVED				ns	
6400AN	16.250	14.375	52	tCK(AVG)	RESERVED								ns	
6800C	20.000	17.647	68	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	18.823	16.470	64	tCK(AVG)	0.294	<0.312	0.294	<0.312	RESERVED				ns	
6800B	18.823	16.176	64	tCK(AVG)	0.294	<0.312	0.294	<0.312	RESERVED				ns	
6800AN	16.470	14.117	56	tCK(AVG)	RESERVED								ns	
7200C	20.000	17.500	72	tCK(AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200BN,B	18.888	16.111	68	tCK(AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	RESERVED		ns	
7200AN	16.111	14.444	58	tCK(AVG)	0.277	<0.294	RESERVED						ns	
Supported CL					22,26,30,32,34,36, 38,40,42,44,46,48, 50,52,56,58,60,64, 68,72		22,30,32,34,36,38, 40,42,44,46,48,50, 52,56,60,64,68,72		22,32,34,36,40,42, 44,46,48,50,52,56, 60,64,68,72		22,32,36,40,44,48, 52,56,60,64,68,72		nCK	12

10.28 3DS DDR5-7600 Speed Bins and Operations

Table 310 — 3DS DDR5-7600 Speed Bins and Operations

Speed Bin					DDR5-7600AN 3DS		DDR5-7600B 3DS		DDR5-7600BN 3DS		DDR5-7600C 3DS		Unit	Note
CL-nRCD-nRP					62-54-54		72-61-61		72-62-62		76-67-67			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	16.315	22.222	18.571	22.222	18.947	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.210	-	16.000	-	16.315	-	17.500	-	ns	7
Row Precharge time				tRP	14.210	-	16.000	-	16.315	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7, 13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.210	-	48.000	-	48.315	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	16.250	15.000	26	tCK(AVG)	RESERVED								ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	16.666	14.444	30	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	16.000	14.000	32	tCK(AVG)	RESERVED								ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	16.363	14.545	36	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	20.000	17.500	48	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	19.166	16.250	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	16.666	14.166	40	tCK(AVG)	RESERVED								ns	
5200C	20.000	17.692	52	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	50	tCK(AVG)	0.384	<0.416	0.384	<0.416	RESERVED				ns	
5200AN	16.153	14.615	42	tCK(AVG)	RESERVED								ns	
5600C	20.000	17.500	56	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600B	18.571	16.071	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600AN	16.428	14.285	46	tCK(AVG)	0.357	<0.384	RESERVED						ns	
6000C	20.000	17.666	60	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	18.666	16.000	56	tCK(AVG)	0.333	<0.357	0.333	<0.357	RESERVED				ns	
6000AN	16.000	14.000	48	tCK(AVG)	RESERVED								ns	
6400C	20.000	17.500	64	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	18.750	16.250	60	tCK(AVG)	0.312	<0.333	0.312	<0.333	RESERVED				ns	
6400AN	16.250	14.375	52	tCK(AVG)	RESERVED								ns	
6800C	20.000	17.647	68	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	18.823	16.470	64	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	RESERVED		ns	
6800B	18.823	16.176	64	tCK(AVG)	0.294	<0.312	0.294	<0.312	RESERVED				ns	
6800AN	16.470	14.117	56	tCK(AVG)	RESERVED								ns	
7200C	20.000	17.500	72	tCK(AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200BN,B	18.888	16.111	68	tCK(AVG)	0.277	<0.294	0.277	<0.294	RESERVED				ns	
7200AN	16.111	14.444	58	tCK(AVG)	RESERVED								ns	
7600C	20.000	17.631	76	tCK(AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	0.263	<0.277	ns	
7600BN	18.347	16.315	72	tCK(AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	RESERVED		ns	
7600B	18.347	16.052	72	tCK(AVG)	0.263	<0.277	0.263	<0.277	RESERVED				ns	
7600AN	16.315	14.210	62	tCK(AVG)	0.263	<0.277	RESERVED						ns	
Supported CL					22,30,32,34,36,38, 40,42,44,46,48,50, 52,56,60,62,64,68, 72,76		22,30,32,34,36,38, 40,42,44,46,48,50, 52,56,60,64,68,72, 76		22,32,34,36,40,42, 44,46,48,52,56,60, 64,68,72,76		22,32,36,40,44,48, 52,56,60,64,68,72, 76		nCK	12

10.29 3DS DDR5-8000 Speed Bins and Operations

Table 311 — 3DS DDR5-8000 Speed Bins and Operations

Speed Bin					DDR5-8000AN 3DS		DDR5-8000B 3DS		DDR5-8000BN 3DS		DDR5-8000C 3DS		Unit	Note
CL-nRCD-nRP					64-56-56		74-64-64		74-64-64		80-70-70			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	16.000	22.222	18.500	22.222	18.500	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.000	-	16.000	-	16.000	-	17.500	-	ns	7
Row Precharge time				tRP	14.000	-	16.000	-	16.000	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7,13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.000	-	48.000	-	48.000	-	49.500	-	ns	7,8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	RESERVED		ns	
3200AN	16.250	15.000	26	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	16.666	14.444	30	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	RESERVED		ns	
4000AN	16.000	14.000	32	tCK(AVG)	0.500	<0.555	RESERVED						ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	16.363	14.545	36	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	20.000	17.500	48	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	19.166	16.250	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800AN	16.666	14.166	40	tCK(AVG)	0.416	<0.454	RESERVED						ns	
5200C	20.000	17.692	52	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	50	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	RESERVED		ns	
5200AN	16.153	14.615	42	tCK(AVG)	0.384	<0.416	RESERVED						ns	
5600C	20.000	17.500	56	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600B	18.571	16.071	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600AN	16.428	14.285	46	tCK(AVG)	0.357	<0.384	RESERVED						ns	
6000C	20.000	17.666	60	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	18.666	16.000	56	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	RESERVED		ns	
6000AN	16.000	14.000	48	tCK(AVG)	0.333	<0.357	RESERVED						ns	
6400C	20.000	17.500	64	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	18.750	16.250	60	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	RESERVED		ns	
6400AN	16.250	14.375	52	tCK(AVG)	0.312	<0.333	RESERVED						ns	
6800C	20.000	17.647	68	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	18.823	16.470	64	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	RESERVED		ns	
6800B	18.823	16.176	64	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	RESERVED		ns	
6800AN	16.470	14.117	56	tCK(AVG)	0.294	<0.312	RESERVED						ns	
7200C	20.000	17.500	72	tCK(AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200BN,B	18.888	16.111	68	tCK(AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	RESERVED		ns	
7200AN	16.111	14.444	58	tCK(AVG)	0.277	<0.294	RESERVED						ns	
7600C	20.000	17.631	76	tCK(AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	0.263	<0.277	ns	
7600BN	18.347	16.315	72	tCK(AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	RESERVED		ns	
7600B	18.347	16.052	72	tCK(AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	RESERVED		ns	
7600AN	16.315	14.210	62	tCK(AVG)	0.263	<0.277	RESERVED						ns	
8000C	20.000	17.500	80	tCK(AVG)	0.250	<0.263	0.250	<0.263	0.250	<0.263	0.250	<0.263	ns	
8000BN,B	18.500	16.000	74	tCK(AVG)	0.250	<0.263	0.250	<0.263	0.250	<0.263	RESERVED		ns	
8000AN	16.000	14.000	64	tCK(AVG)	0.250	<0.263	RESERVED						ns	
Supported CL					22,26,30,32,34,36, 38,40,42,44,46,48, 50,52,56,58,60,62, 64,68,72,74,76,80		22,30,32,34,36,38, 40,42,44,46,48,50, 52,56,60,64,68,72, 74,76,80		22,30,32,34,36,38, 40,42,44,46,48,50, 52,56,60,64,68,72, 74,76,80		22,32,36,40,44,48, 52,56,60,64,68,72, 76,80		nCK	12

10.30 3DS DDR5-8400 Speed Bins and Operations

Table 312 — 3DS DDR5-8400 Speed Bins and Operations

Speed Bin					DDR5-8400AN 3DS		DDR5-8400B 3DS		DDR5-8400BN 3DS		DDR5-8400C 3DS		Unit	Note
CL-nRCD-nRP					68-60-60		78-68-68		78-68-68		84-74-74			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	16.190	22.222	18.500	22.222	18.571	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.285	-	16.000	-	16.190	-	17.500	-	ns	7
Row Precharge time				tRP	14.285	-	16.000	-	16.190	-	17.500		ns	7
Activate to Precharge command period				tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7, 13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.285	-	48.000	-	48.190	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	RESERVED		ns	
3200AN	16.250	15.000	26	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	16.666	14.444	30	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	16.000	14.000	32	tCK(AVG)	RESERVED								ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	16.363	14.545	36	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	20.000	17.500	48	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	19.166	16.250	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	16.666	14.166	40	tCK(AVG)	RESERVED								ns	
5200C	20.000	17.692	52	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	50	tCK(AVG)	0.384	<0.416	0.384	<0.416	RESERVED				ns	
5200AN	16.153	14.615	42	tCK(AVG)	RESERVED								ns	
5600C	20.000	17.500	56	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	RESERVED		ns	
5600B	18.571	16.071	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600AN	16.428	14.285	46	tCK(AVG)	0.357	<0.384	RESERVED						ns	
6000C	20.000	17.666	60	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	18.666	16.000	56	tCK(AVG)	0.333	<0.357	0.333	<0.357	RESERVED				ns	
6000AN	16.000	14.000	48	tCK(AVG)	RESERVED								ns	
6400C	20.000	17.500	64	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	18.750	16.250	60	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	RESERVED		ns	
6400AN	16.250	14.375	52	tCK(AVG)	0.312	<0.333	RESERVED						ns	
6800C	20.000	17.647	68	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	18.823	16.470	64	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	RESERVED		ns	
6800B	18.823	16.176	64	tCK(AVG)	0.294	<0.312	0.294	<0.312	RESERVED				ns	
6800AN	16.470	14.117	56	tCK(AVG)	RESERVED								ns	
7200C	20.000	17.500	72	tCK(AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200BN,B	18.888	16.111	68	tCK(AVG)	0.277	<0.294	0.277	<0.294	RESERVED				ns	
7200AN	16.111	14.444	58	tCK(AVG)	RESERVED								ns	
7600C	20.000	17.631	76	tCK(AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	0.263	<0.277	ns	
7600BN	18.347	16.315	72	tCK(AVG)	0.263	<0.277	0.263	<0.277	RESERVED				ns	
7600B	18.347	16.052	72	tCK(AVG)	0.263	<0.277	0.263	<0.277	RESERVED				ns	
7600AN	16.315	14.210	62	tCK(AVG)	RESERVED								ns	
8000C	20.000	17.500	80	tCK(AVG)	0.250	<0.263	0.250	<0.263	0.250	<0.263	0.250	<0.263	ns	
8000BN,B	18.500	16.000	74	tCK(AVG)	0.250	<0.263	0.250	<0.263	RESERVED				ns	
8000AN	16.000	14.000	64	tCK(AVG)	RESERVED								ns	
8400C	20.000	17.619	84	tCK(AVG)	0.238	<0.250	0.238	<0.250	0.238	<0.250	0.238	<0.250	ns	
8400BN,B	18.571	16.190	78	tCK(AVG)	0.238	<0.250	0.238	<0.250	0.238	<0.250	RESERVED		ns	
8400AN	16.190	14.285	68	tCK(AVG)	0.238	<0.250	RESERVED						ns	
Supported CL					22,26,30,32,34,36, 38,40,42,44,46,48, 50,52,56,60,64,68, 72,74,76,78,80,84		22,30,32,34,36,38, 40,42,44,46,48,50, 52,56,60,64,68,72, 74,76,78,80,84		22,30,32,34,36,40, 42,44,46,48,52,56, 60,64,68,72,76,78, 80,84		22,32,36,40,44,48, 52,56,60,64,68,72, 76,80,84		nCK	12

10.31 3DS DDR5-8800 Speed Bins and Operations

Table 313 — 3DS DDR5-8800 Speed Bins and Operations

Speed Bin					DDR5-8800AN 3DS		DDR5-8800B 3DS		DDR5-8800BN 3DS		DDR5-8800C 3DS		Unit	Note
CL-nRCD-nRP					72-62-62		82-71-71		82-72-72		88-77-77			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	16.363	22.222	18.500	22.222	18.636	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.090	-	16.000	-	16.363	-	17.500	-	ns	7
Row Precharge time				tRP	14.090	-	16.000	-	16.363	-	17.500		ns	7
Activate to Precharge command period				tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7, 13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.090	-	48.000	-	48.363	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	16.250	15.000	26	tCK(AVG)	RESERVED								ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	16.666	14.444	30	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	16.000	14.000	32	tCK(AVG)	RESERVED								ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	16.363	14.545	36	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	20.000	17.500	48	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	19.166	16.250	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	16.666	14.166	40	tCK(AVG)	0.416	<0.454	RESERVED						ns	
5200C	20.000	17.692	52	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	50	tCK(AVG)	0.384	<0.416	0.384	<0.416	RESERVED				ns	
5200AN	16.153	14.615	42	tCK(AVG)			RESERVED						ns	
5600C	20.000	17.500	56	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600B	18.571	16.071	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600AN	16.428	14.285	46	tCK(AVG)	0.357	<0.384	RESERVED						ns	
6000C	20.000	17.666	60	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	18.666	16.000	56	tCK(AVG)	0.333	<0.357	0.333	<0.357	RESERVED				ns	
6000AN	16.000	14.000	48	tCK(AVG)	RESERVED								ns	
6400C	20.000	17.500	64	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	18.750	16.250	60	tCK(AVG)	0.312	<0.333	0.312	<0.333	RESERVED				ns	
6400AN	16.250	14.375	52	tCK(AVG)	RESERVED								ns	
6800C	20.000	17.647	68	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	18.823	16.470	64	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	RESERVED		ns	
6800B	18.823	16.176	64	tCK(AVG)	0.294	<0.312	0.294	<0.312	RESERVED				ns	
6800AN	16.470	14.117	56	tCK(AVG)	0.294	<0.312	RESERVED						ns	
7200C	20.000	17.500	72	tCK(AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200BN,B	18.888	16.111	68	tCK(AVG)	0.277	<0.294	0.277	<0.294	RESERVED				ns	
7200AN	16.111	14.444	58	tCK(AVG)	RESERVED								ns	

Table 313 — 3DS DDR5-8800 Speed Bins and Operations (cont'd)

7600C	20.000	17.631	76	tCK(AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	0.263	<0.277	ns	
7600BN	18.347	16.315	72	tCK(AVG)	0.263	<0.277	0.263	<0.277	RESERVED				ns	
7600B	18.347	16.052	72	tCK(AVG)	0.263	<0.277	0.263	<0.277	RESERVED				ns	
7600AN	16.315	14.210	62	tCK(AVG)	RESERVED								ns	
8000C	20.000	17.500	80	tCK(AVG)	0.250	<0.263	0.250	<0.263	0.250	<0.263	0.250	<0.263	ns	
8000BN,B	18.500	16.000	74	tCK(AVG)	0.250	<0.263	0.250	<0.263	RESERVED				ns	
8000AN	16.000	14.000	64	tCK(AVG)	RESERVED								ns	
8400C	20.000	17.619	84	tCK(AVG)	0.238	<0.250	0.238	<0.250	0.238	<0.250	0.238	<0.250	ns	
8400BN,B	18.571	16.190	78	tCK(AVG)	0.238	<0.250	0.238	<0.250	RESERVED				ns	
8400AN	16.190	14.285	68	tCK(AVG)	RESERVED								ns	
8800C	20.000	17.500	88	tCK(AVG)	0.227	<0.238	0.227	<0.238	0.227	<0.238	0.227	<0.238	ns	
8800BN	18.636	16.363	82	tCK(AVG)	0.227	<0.238	0.227	<0.238	0.227	<0.238	RESERVED		ns	
8800B	18.636	16.136	82	tCK(AVG)	0.227	<0.238	0.227	<0.238	RESERVED				ns	
8800AN	16.363	14.090	72	tCK(AVG)	0.227	<0.238	RESERVED						ns	
Supported CL					22,30,32,34,36,38, 40,42,44,46,48,50, 52,56,60,64,68,72, 74,76,78,80,82,84, 88		22,30,32,34,36,38, 40,42,44,46,48,50, 52,56,60,64,68,72, 74,76,78,80,82,84, 88		22,32,34,36,40,42, 44,46,48,52,56,60, 64,68,72,76,80,82, 84,88		22,32,36,40,44,48, 52,56,60,64,68,72, 76,80,84,88		nCK	12

10.32 3DS DDR5-9200 Speed Bins and Operations

Table 314 — 3DS DDR5-9200 Speed Bins and Operations

Speed Bin					DDR5-9200AN 3DS		DDR5-9200B 3DS		DDR5-9200BN 3DS		DDR5-9200C 3DS		Unit	Note
CL-nRCD-nRP					74-66-66		86-74-74		86-74-74		92-81-81			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Read command to first data				tAA	16.086	22.222	18.500	22.222	18.695	22.222	20.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.347	-	16.000	-	16.086	-	17.500	-	ns	7
Row Precharge time				tRP	14.347	-	16.000	-	16.086	-	17.500		ns	7
Activate to Precharge command period				tRAS	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	32.000	5 * tREFI1 (Norm) 9 * tREFI2 (FGR)	ns	7, 13
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.347	-	48.000	-	48.086	-	49.500	-	ns	7, 8
CAS Write Latency				CWL	CL-2								nCK	12
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Table										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6, 9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	16.250	15.000	26	tCK(AVG)	RESERVED								ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	16.666	14.444	30	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	16.000	14.000	32	tCK(AVG)	RESERVED								ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	16.363	14.545	36	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	20.000	17.500	48	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	19.166	16.250	46	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	16.666	14.166	40	tCK(AVG)	0.416	<0.454	RESERVED						ns	
5200C	20.000	17.692	52	tCK(AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	50	tCK(AVG)	0.384	<0.416	0.384	<0.416	RESERVED				ns	
5200AN	16.153	14.615	42	tCK(AVG)			RESERVED						ns	
5600C	20.000	17.500	56	tCK(AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600B	18.571	16.071	52	tCK(AVG)	0.357	<0.384	0.357	<0.384	RESERVED				ns	
5600AN	16.428	14.285	46	tCK(AVG)	0.357	<0.384	RESERVED						ns	
6000C	20.000	17.666	60	tCK(AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	18.666	16.000	56	tCK(AVG)	0.333	<0.357	0.333	<0.357	RESERVED				ns	
6000AN	16.000	14.000	48	tCK(AVG)	RESERVED								ns	
6400C	20.000	17.500	64	tCK(AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	18.750	16.250	60	tCK(AVG)	0.312	<0.333	0.312	<0.333	RESERVED				ns	
6400AN	16.250	14.375	52	tCK(AVG)	RESERVED								ns	
6800C	20.000	17.647	68	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	18.823	16.470	64	tCK(AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	RESERVED		ns	
6800B	18.823	16.176	64	tCK(AVG)	0.294	<0.312	0.294	<0.312	RESERVED				ns	
6800AN	16.470	14.117	56	tCK(AVG)	0.294	<0.312	RESERVED						ns	
7200C	20.000	17.500	72	tCK(AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200BN,B	18.888	16.111	68	tCK(AVG)	0.277	<0.294	0.277	<0.294	RESERVED				ns	
7200AN	16.111	14.444	58	tCK(AVG)	RESERVED								ns	
7600C	20.000	17.631	76	tCK(AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	0.263	<0.277	ns	

Table 314 — 3DS DDR5-9200 Speed Bins and Operations (cont'd)

7600BN	18.347	16.315	72	tCK(AVG)	0.263	<0.277	0.263	<0.277	RESERVED				ns	
7600B	18.347	16.052	72	tCK(AVG)	0.263	<0.277	0.263	<0.277	RESERVED				ns	
7600AN	16.315	14.210	62	tCK(AVG)	RESERVED								ns	
8000C	20.000	17.500	80	tCK(AVG)	0.250	<0.263	0.250	<0.263	0.250	<0.263	0.250	<0.263	ns	
8000BN,B	18.500	16.000	74	tCK(AVG)	0.250	<0.263	0.250	<0.263	RESERVED				ns	
8000AN	16.000	14.000	64	tCK(AVG)	RESERVED								ns	
8400C	20.000	17.619	84	tCK(AVG)	0.238	<0.250	0.238	<0.250	0.238	<0.250	0.238	<0.250	ns	
8400BN,B	18.571	16.190	78	tCK(AVG)	0.238	<0.250	0.238	<0.250	RESERVED				ns	
8400AN	16.190	14.285	68	tCK(AVG)	RESERVED								ns	
8800C	20.000	17.500	88	tCK(AVG)	0.227	<0.238	0.227	<0.238	0.227	<0.238	0.227	<0.238	ns	
8800BN	18.636	16.363	82	tCK(AVG)	0.227	<0.238	0.227	<0.238	0.227	<0.238	RESERVED		ns	
8800B	18.636	16.136	82	tCK(AVG)	0.227	<0.238	0.227	<0.238	RESERVED				ns	
8800AN	16.363	14.090	72	tCK(AVG)	0.227	<0.238	RESERVED						ns	
9200C	20.000	17.608	92	tCK(AVG)	0.217	<0.227	0.217	<0.227	0.217	<0.227	0.217	<0.227	ns	
9200BN,B	18.695	16.086	86	tCK(AVG)	0.217	<0.227	0.217	<0.227	0.217	<0.227	RESERVED		ns	
9200AN	16.086	14.347	74	tCK(AVG)	0.217	<0.227	RESERVED						ns	
Supported CL					22,30,32,34,36,38, 40,42,44,46,48,50, 52,56,60,64,68,72, 74,76,78,80,82,84, 88,92		22,30,32,34,36,38, 40,42,44,46,48,50, 52,56,60,64,68,72, 74,76,78,80,82,84, 88,92		22,32,34,36,40,42, 44,46,48,52,56,60, 64,68,72,76,80,82, 84,88,92		22,32,36,40,44,48, 52,56,60,64,68,72, 76,80,84,88,92		nCK	12

DDR5 Speed Bin Table Notes:

1. Minimum timing parameters are defined according to the rules in the Rounding Definitions and Algorithms section.
2. The translation of all timing parameters from ns values to nCK values shall follow the Rounding Algorithm. The translation of tAA to CL shall follow the explicit combinations listed in the Speed Bin Tables.
3. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When selecting tCK(avg), requirements from the CL setting as well as requirements from the CWL setting shall be fulfilled.
4. 'Reserved' settings are not allowed. The user shall program a different value.
5. This column shows the intended native speed bin timings to be replaced and supported when down clocking. This column does not necessarily show the actual minimum speed bin timings allowed and supported when down clocking because the timings could be faster according to the Rounding Algorithm, depending on the specific speed bin and down clock frequency combination.
6. DDR5-3200 AC timings apply if the DRAM operates slower than the 2933 MT/s data rate. This is not limited to only the Speed Bin Table timings.
7. Parameters apply from tCK(avg)min to tCK(avg)max.
8. tRC(min) shall always be greater than or equal to tRAS(min) + tRP(min), and when using the appropriate rounding algorithms, nRC(min) shall always be greater than or equal to nRAS(min) + nRP(min).
9. tCK(avg).max of 1.010 ns (1980 MT/s data rate) is defined to allow for 1% SSC down-spreading at a data rate of 2000 MT/s according to JESD404-1.
10. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC standard. The JEDEC standard does not require support for all speed bins within a given speed. The JEDEC standard requires meeting the parameters for a least one of the listed speed bins.
11. Any speed bin also supports functional operation at slower frequencies as shown in the table which are not subject to Production Tests but are verified by Design/Characterization.
12. The CL Algorithm can be used to mathematically determine the valid CAS Latencies listed in the Speed Bin Tables. The CL Algorithm calculates supported CAS Latencies by rounding the operating frequency up to the next faster native speed bin (i.e., 3200 MT/s, 3600 MT/s...). Using the resulting tCK(AVG)min, and the bin target timings, the CL Algorithm then uses the Rounding Algorithm to calculate the valid CAS Latency. Because the DDR5 SDRAM specification only supports even CAS Latencies, odd CAS Latencies are rounded up to the next even CAS Latency. The 1980-2100 MT/s data rate always uses CL22. If tAA(corrected) or tRCDtRP(corrected) are violated, the CL Algorithm uses a slower combination of tAA(target) and tRCDtRP(target) to return slower valid CAS Latencies. The DDR5 SDRAM can support up to four valid CAS Latencies, CL(AN), CL(B), CL(BN), and CL(C), for a given frequency. tAA(corrected) and tRCDtRP(corrected) are calculated by reducing tAA(min), tRCD(min), and tRP(min) by the Rounding Algorithm correction factor. The proper setting of CL shall be determined by the memory controller, either by using the Speed Bin Tables, or by using the CL Algorithm, or by some other means. Refer to the Rounding Definitions and Algorithm section for more information. When Read CRC is enabled, CL is increased according to the Read CRC Latency Adder. When Write CRC is enabled, there is no Write CRC Latency Adder.

DDR5 Speed Bin Table Notes (cont'd):

```
// Variables already defined in other areas of the DDR5 SDRAM specification
CorrFact       = 0.30                                          // (%)   Rounding Algorithm correction factor
ScaledCorrFact = 997                                           //       Scaled correction factor (1000*(1-0.30%))
tCKreal        =1011-952, 682-217                              // (ps)  Real application tCK(AVG) (1980-2100MT/s, 2933-9200MT/s)
tAAmin         MONO=14000-17500, 3DS=16000-20000               // (ps)  From Speed Bin Tables and DIMM SPD bytes 30-31
tRCDtRPmin     MONO=14000-17500, 3DS=14000-17500               // (ps)  From Speed Bin Tables and DIMM SPD bytes 32-33 (tRCD=tRP)
tAAcorr        = TRUNC(tAAmin*ScaledCorrFactor/1000)           // (ps)  Corrected tAA(min) per the Rounding Algorithm rules
tRCDtRPcorr    = TRUNC(tRCDtRPmin*ScaledCorrFactor/1000)       // (ps)  Corrected tRCD(min), tRP(min) per the Rounding Algorithm
FUNC[RA(targ)] = TRUNC((targ*ScaledCorrFact/tCKstd+1000)/1000) // (nCK) Use Rounding Algorithm to convert bin target timing to nCK
// Round tCKreal down to the next faster standard frequency (tCK in ps)
IF (TRUNC(2000000/(2000*99%))>=TRUNC(tCKreal)>=TRUNC(2000000/(2000*105%)))             // Check for  1980-2100 nominal data rates
   tCKstd=TRUNC(2000000/2000)                                                          // Assign standard 2000 tCK (ps)
ELSE IF (TRUNC(2000000/(2000+7*(133+1/3)))>=TRUNC(tCKreal)>=TRUNC(2000000/3200))       // Check for  2933-3200 nominal data rates
   tCKstd=TRUNC(2000000/3200)                                                          // Assign standard 3200 tCK (ps)
ELSE
   FOR (DataRateNom=3200; DataRateNom<=8800; DataRateNom=DataRateNom+400)              // Check for >3200-9200 nominal data rates
      IF (TRUNC(2000000/DataRateNom)>TRUNC(tCKreal)>=TRUNC(2000000/(DataRateNom+400)))
         tCKstd=TRUNC(2000000/(DataRateNom+400))                                       // Assign standard 3600-9200 tCK (ps)
      ELSE
         tCKstd=RESERVED                                                             // No valid data rate found

// Timing targets (ps) that have been used to define the Speed Bin Tables
// MONO targets             3DS targets
   BinAN_tAAtarg     = 14000 BinAN_tAAtarg     = 16000         // tAA target for AN bins
   BinB__tAAtarg     = 16000 BinB__tAAtarg     = 18500         // tAA target for AN, B bins
   BinBN_tAAtarg     = 16000 BinBN_tAAtarg     = 18500         // tAA target for AN, B, BN bins
   BinC__tAAtarg     = 17500 BinC__tAAtarg     = 20000         // tAA target for AN, B, BN, C bins
   BinAN_tRCDtRPtarg = 14000 BinAN_tRCDtRPtarg = 14000         // tRCD, tRP target for AN bins
   BinBN_tRCDtRPtarg = 16000 BinBN_tRCDtRPtarg = 16000         // tRCD, tRP target for AN, B, BN bins
   BinC__tRCDtRPtarg = 17500 BinC__tRCDtRPtarg = 17500         // tRCD, tRP target for AN, B, BN, C bins
IF (TRUNC(2000000/3600)>tCKstd)                                // tRCD, tRP target for B bins is frequency dependent
   BinB__tRCDtRPtarg = 16000 BinB__tRCDtRPtarg = 16000         // tRCD, tRP target for AN, B bins data rates faster than 3600
ELSE
   // 16250=(2000000/3200)*EVEN(TRUNC((BinB__tRCDtRPtarg*ScaledCorrFact/(2000000/3200)+1000)/1000))
   BinB__tRCDtRPtarg = 16250 BinB__tRCDtRPtarg = 16250         // tRCD, tRP target for AN, B bins for data rates 3600 and slower

// CL Algorithm using variables defined above
// Up to four valid CL's can be returned for a specific freq: CL(AN), CL(B), CL(BN), CL(C), depending on tAAmin, tRCDmin, tRPmin
// The B and BN bins return the same CL
// Only even CL's (not odd CL's) are valid per the DDR5 SDRAM specification
// nRCD, nRP are only even at standard native frequencies for the AN, BN bins (can be even or odd at intermediate frequencies)
// nRCD, nRP may be even or odd at standard native frequencies for the B, C bins (can be even or odd at intermediate frequencies)
IF (TRUNC(2000000/2000)=tCKstd)                                // CL22 is the only valid CL for 1980-2100 data rates
   CL(AN)=22                                                   // Valid even CL for AN bins
   CL(B )=22                                                   // Valid even CL for AN, B, bins
   CL(BN)=22                                                   // Valid even CL for AN, B, BN bins
   CL(C )=22                                                   // Valid even CL for AN, B, BN, C bins
ELSE IF (TRUNC(2000000/3200)>=tCKstd>=TRUNC(2000000/8800))     // Valid CL for 2933-9200 data rates
   IF      ((EVEN(RA(BinAN_tAAtarg))*tCKstd>=tAAcorr)AND(EVEN(RA(BinAN_tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even only
      CL(AN)=EVEN(RA(BinAN_tAAtarg))                           // Valid even CL for AN bins
      CL(B )=EVEN(RA(BinB__tAAtarg))                           // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                           // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                           // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinB__tAAtarg))*tCKstd>=tAAcorr)AND(    (RA(BinB__tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even, odd
      CL(AN)=RESERVED                                          // Valid even CL for AN bins
      CL(B )=EVEN(RA(BinB__tAAtarg))                           // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                           // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                           // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinBN_tAAtarg))*tCKstd>=tAAcorr)AND(EVEN(RA(BinBN_tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even only
      CL(AN)=RESERVED                                          // Valid even CL for AN bins
      CL(B )=RESERVED                                          // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                           // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                           // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinC__tAAtarg))*tCKstd>=tAAcorr)AND(    (RA(BinC__tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even, odd
      CL(AN)=RESERVED                                          // Valid even CL for AN bins
      CL(B )=RESERVED                                          // Valid even CL for AN, B bins
      CL(BN)=RESERVED                                          // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                           // Valid even CL for AN, B, BN, C bins
   ELSE                                                        // No valid CL found (tAAmin, tRCDmin, tRPmin are too slow)
      CL(AN)=RESERVED                                          // Valid even CL for AN bins
      CL(B )=RESERVED                                          // Valid even CL for AN, B bins
      CL(BN)=RESERVED                                          // Valid even CL for AN, B, BN bins
      CL(C )=RESERVED                                          // Valid even CL for AN, B, BN, C bins
ELSE                                                           // No valid data rate found
   CL(AN)=RESERVED                                             // Valid even CL for AN bins
   CL(B )=RESERVED                                             // Valid even CL for AN, B bins
   CL(BN)=RESERVED                                             // Valid even CL for AN, B, BN bins
   CL(C )=RESERVED                                             // Valid even CL for AN, B, BN, C bins
```

13. tRAS(max) shall always be less than or equal to 5*tREFI1(max) during Normal Refresh Mode and less than or equal to 9*tREFI2(max) during Fine Granularity Refresh Mode, and when using the rounding algorithms, nRAS(max) shall always be less than or equal to 5*nREFI1(max) during Normal Refresh Mode and less than or equal to 9*nREFI2(max) during Fine Granularity Refresh Mode.

11 IDD, IDDQ, and IPP Specification Parameters and Test Conditions

11.1 IDD, IPP, and IDDQ Measurement Conditions

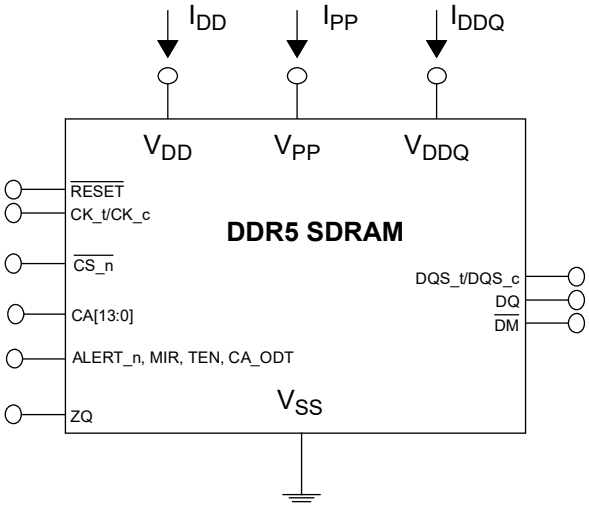
In this chapter, IDD, IPP, and IDDQ measurement conditions such as test load and patterns are defined. Figure 254 shows the setup and test load for IDD, IPP, and IDDQ measurements.

- IDD currents (such as IDD0, IDDQ0, IPP0, IDD0F, IDDQ0F, IPP0F, IDD2N, IDDQ2N, IPP2N, IDD2NT, IDDQ2NT, IPP2NT, IDD2P, IDDQ2P, IPP2P, IDD3N, IDDQ3N, IPP3N, IDD3P, IDDQ3P, IPP3P, IDD4R, IDDQ4R, IPP4R, IDD4RC, IDD4W, IDDQ4W, IPP4W, IDD4WC, IDD5F, IDDQ5F, IPP5F, IDD5B, IDDQ5B, IPP5B, IDD5C, IDDQ5C, IPP5C, IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD7, IDDQ7, IPP7, IDD8, IDDQ8, IPP8 and IDD9, IDDQ9, IPP9) are measured as time-averaged currents with all VDD balls of the DDR5 SDRAM under test tied together. Any IDDQ or IPP current is not included in IDD currents.
- IDDQ currents are measured as time-averaged currents with all VDDQ balls of the DDR5 SDRAM under test tied together. Any IDD or IPP current is not included in IDDQ currents.
- IPP currents are measured as time-averaged currents with all VPP balls of the DDR5 SDRAM under test tied together. Any IDD or IDDQ current is not included in IPP currents.

Attention: IDDQ values cannot be directly used to calculate IO power of the DDR5 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 255.

For IDD, IPP, and IDDQ measurements, the following definitions apply:

- “0” and “LOW” is defined as VIN <= VILAC(max).
- “1” and “HIGH” is defined as VIN >= VIHAC(min).
- “MID-LEVEL” is defined as inputs are VREF = 0.75 * VDDQ.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table 315.
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in Chapter 11.2 through Chapter 11.11.
- IDD Measurements are done after properly initializing and training the DDR5 SDRAM. This includes but is not limited to setting
  TDQS_t disabled in MR5;
  CRC disabled in MR50;
  DM disabled in MR5;
  1N mode enabled and set CS assertion duration (MR2:OP[4]) as 1_B in MR2, unless otherwise specified in the IDD, IDDQ, and IPP patterns’ conditions definitions;
- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD, IDDQ or IPP measurement is started, with the exception of IDD9 which can be measured any time after the DRAM has entered MBIST mode.
- T_{CASE} defined as 0 - 95 °C, unless stated in the specific condition definition Table 315.
- For all IDD, IDDQ and IPP measurement loop timing parameters, refer to the timing parameters defined in the spec to calculate the nCK required.



NOTES:
1. DIMM level Output test load condition may be different from above

Figure 254 — Measurement Setup and Test Load for IDD, IPP, and IDDQ Measurements

11.1 IDD, IPP, and IDDQ Measurement Conditions (cont'd)

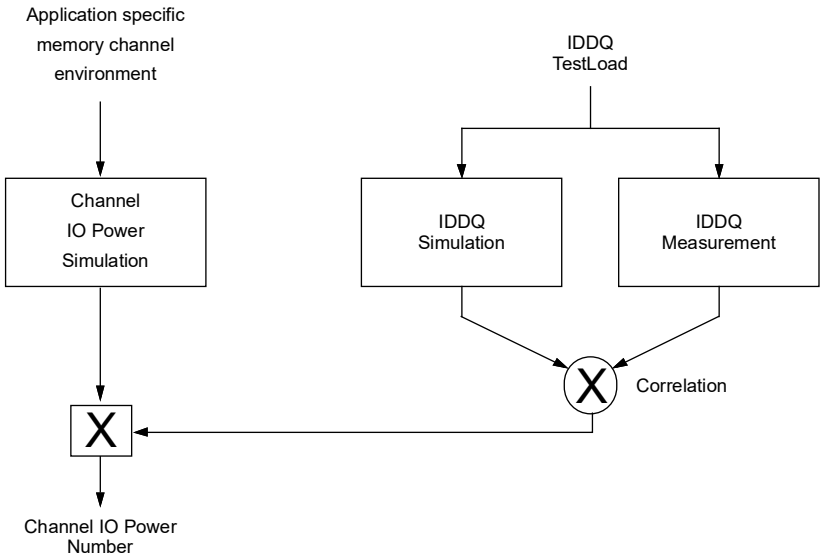


Figure 255 — Correlation from Simulated Channel IO Power to Actual Channel IO Power Supported by IDDQ Measurement

Table 315 — Basic IDD, IDDQ, and IPP Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current** **External clock:** On; **tCK, nRC, nRAS, nRP, nRRD**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n:** High between ACT and PRE; **CA Inputs:** partially toggling according to Table 316; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 316); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 316
IDDQ0	**Operating One Bank Active-Precharge IDDQ Current** **Same condition with IDD0,** however measuring IDDQ current instead of IDD current
IPP0	**Operating One Bank Active-Precharge IPP Current** **Same condition with IDD0,** however measuring IPP current instead of IDD current
IDD0F	**Operating Four Bank Active-Precharge Current** **External clock:** On; **tCK, nRC, nRAS, nRP, nRRD**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n:** High between ACT and PRE; **CA Inputs:** partially toggling according to Table 317; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with four bank active at a time: (see Table 317); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 317
IDDQ0F	**Operating Four Bank Active-Precharge IDDQ Current** **Same condition with IDD0F,** however measuring IDDQ current instead of IDD current
IPP0F	**Operating Four Bank Active-Precharge IPP Current** **Same condition with IDD0F,** however measuring IPP current instead of IDD current
IDD2N	**Precharge Standby Current** **External clock:** On; **tCK**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **CS_n:** stable at 1; **CA Inputs:** partially toggling according to Table 318; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 318
IDDQ2N	**Precharge Standby IDDQ Current** **Same condition with IDD2N,** however measuring IDDQ current instead of IDD current
IPP2N	**Precharge Standby IPP Current** **Same condition with IDD2N,** however measuring IPP current instead of IDD current
IDD2NT	**Precharge Standby Non-Target Command Current** **External clock:** On; **tCK**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n:** High between WRITE commands; **CS_n, CA Inputs:** partially toggling according to Table 319; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 319

Table 315 — Basic IDD, IDDQ, and IPP Measurement Conditions (cont'd)

Symbol	Description
IDDQ2NT (Optional)	**Precharge Standby Non-Target Command IDDQ Current** Same condition with IDD2NT, however measuring IDDQ current instead of IDD current
IPP2NT (Optional)	**Precharge Standby Non-Target Command IPP Current** Same condition with IDD2NT, however measuring IPP current instead of IDD current
IDD2P	**Precharge Power-Down** **Device in Precharge Power-Down, External clock:** On; **tCK**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **CS_n:** stable at 1 after Power Down Entry command; **CA Inputs:** stable at 1; CA11=H during the PDE command; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2];
IDDQ2P	**Precharge Power-Down** **Same condition with IDD2P,** however measuring IDDQ current instead of IDD current
IPP2P	**Precharge Power-Down** **Same condition with IDD2P,** however measuring IPP current instead of IDD current
IDD3N	**Active Standby Current** **External clock:** On; **tCK**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **CS_n:** stable at 1; **CA Inputs:** partially toggling according to Table 318; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 318
IDDQ3N	**Active Standby IDDQ Current** **Same condition with IDD3N,** however measuring IDDQ current instead of IDD current
IPP3N	**Active Standby IPP Current** **Same condition with IDD3N,** however measuring IPP current instead of IDD current
IDD3P	**Active Power-Down Current** **Device in Active Power-Down, External clock:** On; **tCK**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **CS_n:** stable at 1 after Power Down Entry command; **CA Inputs:** stable at 1; CA11=H during the PDE command; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2];
IDDQ3P	**Active Power-Down IDDQ Current** **Same condition with IDD3P,** however measuring IDDQ current instead of IDD current
IPP3P	**Active Power-Down IPP Current** **Same condition with IDD3P,** however measuring IPP current instead of IDD current
IDD4R	**Operating Burst Read Current** **External clock:** On; **tCK, nCCD_S, CL**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n:** High between RD; **CA Inputs:** partially toggling according to Table 320; **Data IO:** seamless read data burst with different data between one burst and the next one according to Table 320; **DM_n:** stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 320); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 320
IDD4RC	**Operating Burst Read Current with Read CRC** **Read CRC enabled[4]. Other conditions:** see IDD4R
IDDQ4R	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IPP4R	**Operating Burst Read IPP Current** **Same condition with IDD4R,** however measuring IPP current instead of IDD current
IDD4W	**Operating Burst Write Current** **External clock:** On; **tCK, nCCD_S_WR, CL**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n:** High between WR; **CA Inputs:** partially toggling according to Table 321; **Data IO:** seamless write data burst with different data between one burst and the next one according to Table 321; **DM_n:** stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 321); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 321
IDD4WC	**Operating Burst Write Current with Write CRC** **Write CRC enabled[3], Other conditions:** see IDD4W
IDDQ4W	**Operating Burst Write IDDQ Current** **Same condition with IDD4W,** however measuring IDDQ current instead of IDD current
IPP4W	**Operating Burst Write IPP Current** **Same condition with IDD4W,** however measuring IPP current instead of IDD current
IDD5B	**Burst Refresh Current (Normal Refresh Mode)** **External clock:** On; **tCK, nRFC**1: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n**: High between REF; **CA Inputs:** partially toggling according to Table 322; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC1 (see Table 322); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 322

Table 315 — Basic IDD, IDDQ, and IPP Measurement Conditions (cont'd)

Symbol	Description
IDDQ5B	**Burst Refresh IDDQ Current (Normal Refresh Mode)** **Same condition with IDD5B,** however measuring IDDQ current instead of IDD current
IPP5B	**Burst Refresh IPP Current (Normal Refresh Mode)** **Same condition with IDD5B,** however measuring IPP current instead of IDD current
IDD5F	**Burst Refresh Current (Fine Granularity Refresh Mode)** **tRFC=tRFC2, Other conditions:** see IDD5B
IDDQ5F	**Burst Refresh IDDQ Current (Fine Granularity Refresh Mode)** **Same condition with IDD5F,** however measuring IDDQ current instead of IDD current
IPP5F	**Burst Refresh IPP Current (Fine Granularity Refresh Mode)** **Same condition with IDD5F,** however measuring IPP current instead of IDD current
IDD5C	**Burst Refresh Current (Same Bank Refresh Mode)** **External clock:** On; **tCK, nRFCsb**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n**: High between REF; **CA Inputs:** partially toggling according to Table 323; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFCsb (see Table 323); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 323
IDDQ5C	**Burst Refresh IDDQPP Current (Same Bank Refresh Mode)** **Same condition with IDD5C,** however measuring IDDQ current instead of IDD current
IPP5C	**Burst Refresh IPP Current (Same Bank Refresh Mode)** **Same condition with IDD5C,** however measuring IPP current instead of IDD current
IDD6N	**Self Refresh Current: Normal Temperature Range** ***T*CASE:** 0 - 85 °C; **External clock:** Off; **CK_t and CK_c**: HIGH; **tCK, nCPDED**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n#:** low; **CA, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Disabled by the DRAM upon entry into Self-Refresh
IDDQ6N	**Self Refresh IDDQ Current: Normal Temperature Range** **Same condition with IDD6N,** however measuring IDDQ current instead of IDD current
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** **Same condition with IDD6N,** however measuring IPP current instead of IDD current
IDD6E	**Self Refresh Current: Extended Temperature Range**) ***T*CASE:** 85 - 95 °C; Extended[4]; **External clock:** Off; **CK_t and CK_c**: HIGH; **tCK, nCPDED**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n:** low; **CA, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Disabled by the DRAM upon entry into Self-Refresh
IDDQ6E	**Self Refresh IDDQ Current: Extended Temperature Range** **Same condition with IDD6E,** however measuring IDDQ current instead of IDD current
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** **Same condition with IDD6E,** however measuring IPP current instead of IDD current
IDD7	**Operating Bank Interleave Read Current** **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD_S, nFAW, tCCD_S CL**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n**: High between ACT and RDA; **CA Inputs:** partially toggling according to Table 325; **Data IO:** read data bursts with different data between one burst and the next one according to Table 325; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 325; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 325
IDDQ7	**Operating Bank Interleave Read IDDQ Current** **Same condition with IDD7,** however measuring IDDQ current instead of IDD current
IPP7	**Operating Bank Interleave Read IPP Current** **Same condition with IDD7,** however measuring IPP current instead of IDD current
IDD8	**Maximum Power Saving Deep Power Down Current** **External clock:** Off; **CK_t and CK_c**: HIGH; **tCK, nCPDED**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n#:** low; **CA:**High**, DM_n:** stable at 1; **Bank Activity:** All banks closed and device in MPSM deep power down mode5; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Patterns Details**: same as IDD6N but MPSM is enabled in mode register.
IDDQ8	**Maximum Power Saving Deep Power Down IDDQ Current** **Same condition with IDD8,** however measuring IDDQ current instead of IDD current
IPP8	**Maximum Power Saving Deep Power Down IPP Current** **Same condition with IDD8,** however measuring IPP current instead of IDD current
IDD9 (Optional)	**MBIST Current** **Device in MBIST mode, External clock:** On; **CS_n**: Stable at 1 after MBIST entry; **CA Inputs:** stable at 1; **Data IO:** VDDQ; **Bank Activity:** MBIST operation; **Output Buffer and RTT:** Enabled in Mode Registers[2];

Table 315 — Basic IDD, IDDQ, and IPP Measurement Conditions (cont'd)

Symbol	Description
IDDQ9 (Optional)	**MBIST IDDQ Current** **Same condition with IDD9,** however measuring IDDQ current instead of IDD current
IPP9 (Optional)	**MBIST IPP Current** **Same condition with IDD9,** however measuring IPP current instead of IDD current

NOTE 1 Burst Length: BL16 fixed by MR0 OP[1:0]=00.

NOTE 2 Output Buffer Enable
- set MR5 OP[0] = 0] : Qoff = Output buffer enabled
- set MR5 OP[2:1] = 00]: Pull-Up Output Driver Impedance Control = RZQ/7
- set MR5 OP[7:6] = 00]: Pull-Down Output Driver Impedance Control = RZQ/7

RTT_Nom enable
- set MR35 OP[5:0] = 110110: RTT_NOM_WR = RTT_NOM_RD = RZQ/6

RTT_WR enable
- set MR34 OP[5:3] = 010 RTT_WR = RZQ/2

CA/CS/CK ODT, DQS_RTT_PART, and RTT_PARK disable
- set MR32 OP[5:0] = 000000
- set/MR33 OP[5:0] = 000000
- set MR34 OP[2:0] = 000

NOTE 3 WRITE CRC enabled
- set MR50 OP[2:1] = 11

NOTE 4 Read CRC enabled
- set MR50:OP[0]=1

NOTE 5 MPSM Deep Power Down Mode
- set MR2:OP[3]=1 if PDA Enumerate ID not equal to 15
- set MR2:OP[5]=1 if PDA Enumerate ID equal to 15

11.2 IDD0, IDDQ0, IPP0 Pattern

Executes Active and PreCharge commands with tightest timing possible while exercising all Bank and Bank Group addresses. Note 2 applies to the entire table.

Table 316 — IDD0, IDDQ0, IPP0

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0	0	ACT	L H	-	0x00000	0x0	0x00	0x0	
	1	DES	H	Toggling[1]					Repeat sequence to satisfy tRAS(min), truncate if required
	2	PREpb	L	-		0x0	0x00	0x0	
	3	DES	H	Toggling[1]					Repeat sequence to satisfy tRP(min), truncate if required
	4	ACT	L H	-	0x03FFF	0x0	0x00	0x0	
	5	DES	H	Toggling[1]					Repeat sequence to satisfy tRAS(min), truncate if required
	6	PREpb	L	-		0x0	0x00	0x0	
	7	DES	H	Toggling[1]					Repeat sequence to satisfy tRP(min), truncate if required
1	8-15	Repeat sub-loop 0, use BG[2:0]=0x1 instead							
2	16-23	Repeat sub-loop 0, use BG[2:0]=0x2 instead							
3	24-31	Repeat sub-loop 0, use BG[2:0]=0x3 instead							
4	32-39	Repeat sub-loop 0, use BG[2:0]=0x4 instead							skip for x16
5	40-47	Repeat sub-loop 0, use BG[2:0]=0x5 instead							skip for x16
6	48-55	Repeat sub-loop 0, use BG[2:0]=0x6 instead							skip for x16
7	56-63	Repeat sub-loop 0, use BG[2:0]=0x7 instead							skip for x16
8-15	64-127	Repeat sub loops 0-7, use BA[1:0]=0x1 instead							
16-23	128-191	Repeat sub loops 0-7, use BA[1:0]=0x2 instead							
24-31	192-255	Repeat sub loops 0-7, use BA[1:0]=0x3 instead							
...	...	Repeat sub loops 0-31 for each 3DS logical rank, if applicable							CID[2:0]=0x1-0x7

NOTE 1 Utilize DESELECTs between commands while toggling all C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
NOTE 2 For 3DS, all banks of all “non-target” logical ranks are Idd2N condition.

11.3 IDD0F, IDDQ0F, IPP0F Pattern

Executes a rolling four bank group Active and PreCharge commands per tRC time while exercising all Bank, Bank, Group and CID addresses. Note 2 applies to the entire table.

Table 317 — IDD0F, IDDQ0F, IPP0F

Sub-Loop	Sequence	Command	CS	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0	0	ACT	L H		0x00000	0x0	0x00	0x0	
	1	DES	H	Toggling[1]					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	2	ACT	L H		0x00000	0x0	0x01	0x0	
	3	DES	H	Toggling[1]					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	4	ACT	L H		0x00000	0x0	0x02	0x0	
	5	DES	H	Toggling[1]					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	6	ACT	L H		0x00000	0x0	0x03	0x0	
	7	DES	H	Toggling[1]					Repeat to satisfy tRAS(min) from Sequence 0
	8	PREpb	L			0x0	0x00	0x0	
	9	DES	H	Toggling[1]					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	10	PREpb	L			0x0	0x01	0x0	
	11	DES	H	Toggling[1]					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	12	PREpb	L			0x0	0x02	0x0	
	13	DES	H	Toggling[1]					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	14	PREpb	L			0x0	0x03	0x0	
	15	DES	H	Toggling[1]					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	16	DES	H	Toggling[1]					Repeat for tRC(min) from Sequence 0 first ACTIVATE. This will be zero DESELECTS for speed 4000MT/s and slower.
1	17-33	Repeat sub-loop 0, use Row Address = 0x03FFF for the ACT instead							
2-3	34-67	Repeat sub-loop 0-1, use BG[2:0]=0x4,0x5,0x6,0x7 instead of 0x0,0x1,0x2,0x3							skip for x16
4-7	68-101	Repeat sub-loops 0-3, use BA[1:0]=0x1 instead							
8-11	102-135	Repeat sub-loops 0-3, use BA[1:0]=0x2 instead							
12-15	136-169	Repeat sub-loops 0-3, use BA[1:0]=0x3 instead							
...	...	Repeat sub loops 0-15 for each 3DS logical rank, if applicable							CID[2:0]=0x1-0x7

NOTE 1 Utilize DESELECTs between commands while toggling C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
NOTE 2 For 3DS, all banks of all “non-target” logical ranks are Idd2N condition.

11.4 IDD2N, IDD3N Pattern

Executes DESELECT commands while exercising all command/address pins in a predefined pattern. All notes apply to entire table.

Table 318 — IDD2N, IDDQ2N, IPP2N, IDD3N, IDDQ3N, IPP3N

Sequence	Command	CS	C/A [13:0]
0	DES	H	0x0000
1	DES	H	0x3FFF
2	DES	H	0x3FFF
3	DES	H	0x3FFF

NOTE 1 Data is pulled to VDDQ
NOTE 2 DQS_t and DQS_c are pulled to VDDQ
NOTE 3 Command / Address ODT is disabled
NOTE 4 Repeat sequence 0 through 3.
NOTE 5 All banks of all logical ranks mimic the same test condition.

11.5 IDD2NT, IDDQ2NT, IPP2NT Pattern

Executes Non-Target WRITE commands simulating Rank to Rank timing while exercising all C/A bits. Notes 3-6 apply to entire table.

Table 319 — IDD2NT, IDDQ2NT, IPP2NT

Sequence	Command	CS_n	C/A [13:0]	Special Instructions
0	WRITE [1]	L	0x002D	All valid C/A inputs to VSS
		L	0x0000	
1	DES	H	Toggling [2]	Repeat sequence to meet 1*tCCD_S_WR (min), truncate if required
2	WRITE[1]	L	0x3FED	All valid C/A inputs to VDDQ
		L	0x3FFF	
3	DES	H	Toggling [2]	Repeat sequence to meet 1*tCCD_S_WR (min), truncate if required

NOTE 1 WRITE with CS_n=L on both cycles indicated a non-target WRITE.
NOTE 2 Utilize DESELECTs between commands while toggling C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
NOTE 3 Time between Non-Target WRITEs reflect 1 * tCCD_S_WR (min) for one ranks.
NOTE 4 DQ signals are VDDQ.
NOTE 5 DQS_t, DQS_c are VDDQ.
NOTE 6 Repeat 0 through 3.

11.6 IDD4R, IDDQ4R, IPP4R Pattern

Executes READ commands with tightest timing possible while exercising all Bank, Bank Group and CID addresses. Notes 2-9 apply to entire table

Table 320 — IDD4R, IDDQ4R, IPP4R

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [3:0]	Data Burst (BL=16)	Special Instructions
0	0	READ	L H	-	0x000	0x00	0x0	0x0	Pattern A	All “Valid” inputs = VDDQ
	1	DES	H	Toggling[1]	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
1	2	READ	L H	-	0x3F0	0x00	0x1	0x0	Pattern B	All “Valid” inputs = VDDQ
	3	DES	H	Toggling[1]	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead								
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead								
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead								skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead								skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead								skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead								skip for x16
8	16	READ	L H	-	0x3F0	0x00	0x0	0x0	Pattern B	All “Valid” inputs = VDDQ
	17	DES	H	Toggling[1]						Repeat sequence to satisfy tCCD_S(min), truncate if required
9	18	READ	L H	-	0x000	0x00	0x1	0x0	Pattern A	All “Valid” inputs = VDDQ
	19	DES	H	Toggling[1]						Repeat sequence to satisfy tCCD_S(min), truncate if required
10	20-21	Repeat sub-loop 8, use BG[2:0]=0x2 instead								
11	22-23	Repeat sub-loop 9, use BG[2:0]=0x3 instead								
12	24-25	Repeat sub-loop 8, use BG[2:0]=0x4 instead								skip for x16
13	26-27	Repeat sub-loop 9, use BG[2:0]=0x5 instead								skip for x16
14	28-29	Repeat sub-loop 8, use BG[2:0]=0x6 instead								skip for x16
15	30-31	Repeat sub-loop 9, use BG[2:0]=0x7 instead								skip for x16
16-31	32-33	Repeat sub-loops 0-15, use BA[1:0]=0x1 instead								
32-47	34-35	Repeat sub-loops 0-15, use BA[1:0]=0x2 instead								
48-63	36-37	Repeat sub-loops 0-15, use BA[1:0]=0x3 instead								
...	...	Repeat sub-loops 0-63 for each 3DS logical rank, if applicable								CID[2:0]=0x1-0x7

NOTE 1 Utilize DESELECTs between commands while toggling all C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
NOTE 2 READs performed with Auto Precharge = H, Burst Chop = H.
NOTE 3 Row address is set to 0x0000
NOTE 4 Data reflects burst length of 16.
NOTE 5 Data Pattern A for x4: 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0x0, 0xF.
NOTE 6 Data Pattern B for x4: 0xF, 0x0, 0x0, 0xF, 0xF, 0x0, 0xF, 0x0, 0x0, 0xF, 0xF, 0x0, 0xF, 0x0, 0xF, 0x0.
NOTE 7 Data Pattern for x8 each beat will reflect two like nibbles (Data Pattern A = 0x00, 0xFF, 0xFF...).
NOTE 8 Data Pattern for x16 each beat will reflect two like bytes (Data Pattern A = 0x0000, 0xFFFF, 0xFFFF...).
NOTE 9 Where C/A column is not populated, refer to command truth table, column address, BA, BG, and CID for the C/A state

11.7 IDD4W, IDDQ4W, IPP4W Pattern

Executes WRITE commands with tightest timing possible while exercising all Bank, Bank Group and ~~CDI~~ CID addresses. Notes 2-6 apply to entire table.

Table 321 — IDD4W, IDDQ4W, IPP4W

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [3:0]	Data Burst (BL=16)	Special Instructions
0	0	WRITE	L H	-	0x000	0x00	0x0	0x0	Pattern A	All “Valid” inputs = VDDQ
	1	DES	H	Toggling[1]	-					Repeat sequence to satisfy tCCD_S_WR (min), truncate if required
1	2	WRITE	L H	-	0x3F0	0x00	0x1	0x0	Pattern B	All “Valid” inputs = VDDQ
	3	DES	H	Toggling[1]	-					Repeat sequence to satisfy tCCD_S_WR (min), truncate if required
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead								
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead								
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead								skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead								skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead								skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead								skip for x16
8	16	WRITE	L H	-	0x3F0	0x00	0x0	0x0	Pattern B	All “Valid” inputs = VDDQ
	17	DES	H	Toggling[1]						Repeat sequence to satisfy tCCD_S_WR (min), truncate if required
9	18	WRITE	L H	-	0x000	0x00	0x1	0x0	Pattern A	All “Valid” inputs = VDDQ
	19	DES	H	Toggling[1]						Repeat sequence to satisfy tCCD_S_WR (min), truncate if required
10	20-21	Repeat sub-loop 8, use BG[2:0]=0x2 instead								
11	22-23	Repeat sub-loop 9, use BG[2:0]=0x3 instead								
12	24-25	Repeat sub-loop 8, use BG[2:0]=0x4 instead								skip for x16
13	26-27	Repeat sub-loop 9, use BG[2:0]=0x5 instead								skip for x16
14	28-29	Repeat sub-loop 8, use BG[2:0]=0x6 instead								skip for x16
15	30-31	Repeat sub-loop 9, use BG[2:0]=0x7 instead								skip for x16
16-31	32-33	Repeat sub-loops 0-15, use BA[1:0]=0x1 instead								
32-47	34-35	Repeat sub-loops 0-15, use BA[1:0]=0x2 instead								
48-63	36-37	Repeat sub-loops 0-15, use BA[1:0]=0x3 instead								
...	...	Repeat sub-loops 0-63 for each 3DS logical rank, if applicable								CID[2:0]=0x1-0x7

NOTE 1 Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
NOTE 2 WRITEs performed with Auto Precharge = H, Burst Chop = H.
NOTE 3 Row address is set to 0x0000.
NOTE 4 Data reflects burst length of 16.
NOTE 5 Refer to IDD4R measurement loop table for data pattern definition.
NOTE 6 Where C/A column is not populated, refer to command truth table, column address, BA, BG, and CID for the C/A state.

11.8 IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F Pattern

Executes Refresh (all Banks) command at minimum tRFC. Notes 3-6 apply to entire table.

Table 322 — IDD5B, IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F

Sequence	Command	CS	C/A [13:0]	CA[9:8]	CID [2:0]	Special Instructions
0	REFab	L	-	H	0x0	All “valid” inputs = VDDQ
1	DES	H	Toggling[1]	-	-	Repeat sequence to satisfy tRFC(min)2, truncate if required
2	REFab	L	-	H	0x0	All “valid” inputs = VDDQ
3	DES	H	Toggling[1]	-	-	Repeat sequence to satisfy tRFC(min)2, truncate if required
...	Repeat sequence 0-3 for each 3DS logical rank, if applicable					CID[2:0]=0x1-0x7

NOTE 1 Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
NOTE 2 For IDD5B, use tRFC1(min). For IDD5F, use tRFC2(min).
NOTE 3 DQ signals are VDDQ.
NOTE 4 All banks of all “non-target” logical ranks are Idd2N condition.
NOTE 5 Where C/A[13:0] column is not populated, refer to command truth table, CA[9:8], and CID columns for the C/A state.
NOTE 6 Must set CA8=H on REFab commands to indicate 1X refresh rate on devices that support RIR.

11.9 IDD5C, IDDQ5C and IPP5C Patterns

Executes Refresh (Same Bank) command at minimum tRFCsb. Notes 2-5 apply to entire table.

Table 323 — IDD5C, IDDQ5C, IPP5C

Sequence	Command	CS	C/A [13:0]	CA[9:8]	BA [1:0]	CID [2:0]	Special Instructions
0	REFsb	L	-	H	0x0	0x0	
1	DES	H	Toggling[1]	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
2	REFsb	L	-	H	0x1	0x0	
3	DES	H	Toggling[1]	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
4	REFsb	L	-	H	0x2	0x0	
5	DES	H	Toggling[1]	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
6	REFsb	L	-	H	0x3	0x0	
7	DES	H	Toggling[1]	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
...	Repeat sequence 0-7 for each 3DS logical rank, if applicable						CID[2:0]=0x1-0x7

NOTE 1 Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
NOTE 2 DQ signals are VDDQ.
NOTE 3 All banks of all “non-target” logical ranks are Idd2N condition.
NOTE 4 Where C/A[13:0] column is not populated, refer to command truth table, CA[9:8], and CID columns for the C/A state.
NOTE 5 All banks of all “non-target” logical ranks are Idd2N condition.

11.10 IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD6R, IDDQ6R, IPP6R Pattern

All notes apply to entire table.

Table 324 — IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E

Sequence	Command	Clock	CS	C/A [13:0]	Special Instructions
0	SRE	Valid	L	0x3BF7	Clocks must be valid tCKLCS(min) time
1	DES	Valid	H	0x3FFF	Repeat sequence to satisfy tCPDED(min), truncate if required
2	All C/A=H	Valid	L	0x3FFF	
3	All C/A = H	CK_t = CK_c = H	L	0x3FFF	Repeat sequence indefinitely

NOTE 1 Data is pulled to VDDQ
NOTE 2 DQS_t and DQS_c are pulled to VDDQ
NOTE 3 For 3DS, all banks of all logical ranks mimic the same test condition.

11.11 IDD7, IDDQ7, and IPP7 Patterns

Executes ACTVATE, READ/A commands with tightest timing possible while exercising all Bank, Bank Group and CID addresses. Notes 2-6 apply to entire table.

Table 325 — IDD7, IDD7Q, IPP7

Sub-Loop	Sequence	Command	CS	C/A [13:0]	Row Address [17:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
0	0	ACT	L H	-	0x00000	-	0x0	0x0	0x0	-	
	1	DES	H	Toggling[1]							Repeat sequence to satisfy tRRD_S(min), tFAW(min), and tRCD(min). Truncate if required.
1	2	ACT	L H	-	0x03FFF	-	0x0	0x1	0x0	-	
	3	DES	H	Toggling[1]							Repeat sequence to satisfy tRRD_S(min), tFAW(min), and tRCD(min). Truncate if required.
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead									
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead									
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead									skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead									skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead									skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead									skip for x16
8	16	RDA	L H	-	-	0x3F0	0x0	0x0	0x0	Pattern A	
	17	ACT	L H	-	0x00000	-	0x1	0x0	0x0	-	
	18	DES	H	Toggling[1]							Repeat sequence to satisfy tCCD_S(min), tFAW(min), and tRCD(min). Truncate if required.
9	19	RDA	L H	-	-	0x000	0x0	0x1	0x0	Pattern B	
	20	ACT	L H	-	0x03FFF	-	0x1	0x1	0x0	-	
	21	DES	H	Toggling[1]							Repeat sequence to satisfy tCCD_S(min), tFAW(min), and tRCD(min). Truncate if required.
10	22-24	Repeat sub-loop 8, use BG[2:0]=0x2 instead									
11	25-27	Repeat sub-loop 9, use BG[2:0]=0x3 instead									
12	28-30	Repeat sub-loop 8, use BG[2:0]=0x4 instead									skip for x16
13	31-33	Repeat sub-loop 9, use BG[2:0]=0x5 instead									skip for x16
14	34-36	Repeat sub-loop 8, use BG[2:0]=0x6 instead									skip for x16
15	37-39	Repeat sub-loop 9, use BG[2:0]=0x7 instead									skip for x16
16-23	40-64	Repeat sub-loops 8-15, use BA[1:0]=0x1 for the RDA and BA[1:0]=0x2 for the ACT									
24-31	65-89	Repeat sub-loops 8-15, use BA[1:0]=0x2 for the RDA and BA[1:0]=0x3 for the ACT									
32-39	90-114	Repeat sub-loops 8-15, use BA[1:0]=0x3 for the RDA and BA[1:0]=0x0 for the ACT									
...	...	Repeat sub-loops 0-18 for each 3DS logical rank, if applicable									CID[2:0]=0x1-0x7

NOTE 1 Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
NOTE 2 READs performed with Auto Precharge = L, Burst Chop = H.
NOTE 3 x8 or x16 may have different Bank or Bank Group Address.
NOTE 4 Data reflects burst length of 16.
NOTE 5 Refer to IDD4R measurement loop table for data pattern definition
NOTE 6 For 3DS, all banks of all “non-target” logical ranks are Idd2N condition

12 Input/Output Capacitance

Table 326 — Silicon Pad I/O Capacitance DDR5-3200 to DDR5-6400

Symbol	Parameter	DDR5-3200/ 3600/4000		DDR5-4400/ 4800		DDR5-5200/5600		DDR5-6000/6400		Unit	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max		
C_{IO}	Input/output capacitance (DQ, DM_n, DQS_t, DQS_c, TDQS_t, TDQS_c)	0.25	0.9	0.25	0.9	0.25	0.85	0.25	0.8	pF	1, 2
C_{DIO}	Input/output capacitance delta (DQ, DM_c)	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1, 2, 8
C_{DDQS}	Input/output capacitance delta (DQS_t and DQS_c)		0.04		0.04		0.04		0.04	pF	1, 2, 4
C_{CK}	Input capacitance (CK_t and CK_c)	0.2	0.7	0.2	0.6	0.2	0.55	0.2	0.5	pF	1, 2
C_{DCK}	Input capacitance delta (CK_t and CK_c)		0.05		0.05		0.05		0.05	pF	1, 2, 3
C_I	Input capacitance (CS_n & CA[13:0] pins only)	0.2	0.7	0.2	0.6	0.2	(C_I Option1) 0.55 (C_I Option2) 0.5	0.2	0.5	pF	1, 2, 5, 12
$C_{DI_CS_n}$	Input capacitance delta (CS_n pin only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1, 2, 6
C_{DI_CA}	Input capacitance delta (CA[13:0] pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1, 2, 7
C_{ALERT}	Input/output capacitance of ALERT	0.3	1.5	0.3	1.5	0.3	1.5	0.3	1.5	pF	1, 2
$C_{Loopback}$	Input/output capacitance of Loopback (LBDQ, LBDQS)	0.25	1.0	0.25	1.0	0.25	1.0	0.25	1.0	pF	1, 2
C_{TEN}	Input capacitance of TEN	0.2	2.3	0.2	2.3	0.2	2.3	0.2	2.3	pF	1, 2, 9
C_{ZQ}	Input capacitance of ZQ	-	5	-	5	-	5	-	5	pF	1, 2, 11
C_{STRAP}	Input capacitance of MIR, CAI, CA_ODT pins	-	10	-	10	-	10	-	10	pF	1, 2, 10

NOTE 1 This parameter is not subject to production test. This parameter is measured by using vendor specific measurement methodology.

NOTE 2 This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here

NOTE 3 Absolute value CIO(CK_t)-CIO(CK_c)

NOTE 4 Absolute value of CIO(DQS_t)-CIO(DQS_c)

NOTE 5 CI applies to CS_n and CA[13:0]

NOTE 6 CDI_CS_n = CI(CS_n)-0.5*(CI(CK_t)+CI(CK_c))

NOTE 7 CDI_CA = CI(CA[13:0])-0.5*(CI(CK_t)+CI(CK_c))

NOTE 8 CDIO = CIO(DQ,DM)-Avg(CIO(DQ,DM))

NOTE 9 TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.

NOTE 10 MIR, CAI, and CA_ODT are strap pins used to configure module or point to point use cases depending on power, signal integrity, and termination requirements. No active AC signaling requirements defined for these pins.

NOTE 11 Maximum external load capacitance on ZQ pin: 25 pF. The ZQ functionality / accuracy with the max capacitive load is characterized.

NOTE 12 CI Options are incorporated VclVW in Table 200 in Section 8.2.

12 Input/Output Capacitance (cont'd)

Table 327 — Silicon Pad I/O Capacitance DDR5-6800 to DDR5-9200

Symbol	Parameter	DDR5-6800/ 7200		DDR5-7600/ 8000		DDR5-8400/ 8800		DDR5-9200		Unit	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max		
C_{IO}	Input/output capacitance (DQ, DM_n, DQS_t, DQS_c, TDQS_t, TDQS_c)	0.25	0.8	0.25	0.75	0.25	0.70	0.25	0.65	pF	1, 2
C_{DIO}	Input/output capacitance delta (DQ, DM_c)	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1, 2, 8
C_{DDQS}	Input/output capacitance delta (DQS_t and DQS_c)		0.04		0.04		0.04		0.04	pF	1, 2, 4
C_{CK}	Input capacitance (CK_t and CK_c)	0.2	0.5	0.2	0.45	0.2	0.40	0.2	0.4	pF	1, 2
C_{DCK}	Input capacitance delta (CK_t and CK_c)		0.05		0.05		0.05		0.05	pF	1, 2, 3
C_{I}	Input capacitance (CS_n & CA[13:0] pins only)	0.2	0.5	0.2	0.45	0.2	0.40	0.2	0.4	pF	1, 2, 5
$C_{DI_CS_n}$	Input capacitance delta (CS_n pin only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1, 2, 6
C_{DI_CA}	Input capacitance delta (CA[13:0] pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1, 2, 7
C_{ALERT}	Input/output capacitance of ALERT	0.3	1.5	0.3	1.5	0.3	1.5	0.3	1.5	pF	1, 2
$C_{Loopback}$	Input/output capacitance of Loop-back (LBDQ, LBDQS)	0.25	1.0	0.25	1.0	0.25	1.0	0.25	1.0	pF	1, 2
C_{TEN}	Input capacitance of TEN	0.2	2.3	0.2	2.3	0.2	2.3	0.2	2.3	pF	1, 2, 9
C_{ZQ}	Input capacitance of ZQ	-	5	-	5	-	5	-	5	pF	1, 2, 11
C_{STRAP}	Input capacitance of MIR, CAI, CA_ODT pins	-	10	-	10	-	10	-	10	pF	1, 2, 10

NOTE 1 This parameter is not subject to production test. This parameter is measured by using vendor specific measurement methodology.

NOTE 2 This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here

NOTE 3 Absolute value CIO(CK_t)-CIO(CK_c)

NOTE 4 Absolute value of CIO(DQS_t)-CIO(DQS_c)

NOTE 5 CI applies to CS_n and CA[13:0]

NOTE 6 CDI_CS_n = CI(CS_n)-0.5*(CI(CK_t)+CI(CK_c))

NOTE 7 CDI_CA = CI(CA[13:0])-0.5*(CI(CK_t)+CI(CK_c))

NOTE 8 CDIO = CIO(DQ,DM)-Avg(CIO(DQ,DM))

NOTE 9 TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.

NOTE 10 MIR, CAI, and CA_ODT are strap pins used to configure module or point to point use cases depending on power, signal integrity, and termination requirements. No active AC signaling requirements defined for these pins.

NOTE 11 Maximum external load capacitance on ZQ pin: 25 pF. The ZQ functionality / accuracy with the max capacitive load is characterized.

12 Input/Output Capacitance (cont'd)

Table 328 — Silicon Pad I/O Capacitance DDR5 DDP 3200 to 6400

Symbol	Parameter	DDR5-3200/ 3600/4000 DDP		DDR5-4400/ 4800 DDP		DDR5-5200/5600 DDP		DDR5-6000/6400 DDP		Unit	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max		
C_{IO}	Input/output capacitance (DQ, DM_n, DQS_t, DQS_c, TDQS_t, TDQS_c)	0.6	1.8	0.6	1.8	0.6	1.7	0.6	1.6	pF	1, 2
C_{DIO}	Input/output capacitance delta (DQ, DM_c)	-0.2	0.2	-0.2	0.2	-0.2	0.2	-0.2	0.2	pF	1, 2, 9
C_{DDQS}	Input/output capacitance delta (DQS_t and DQS_c)		0.08		0.08		0.08		0.08	pF	1, 2, 4
C_{CK}	Input capacitance (CK_t and CK_c)	0.4	1.4	0.4	1.2	0.4	1.1	0.4	1.0	pF	1, 2
C_{DCK}	Input capacitance delta (CK_t and CK_c)		0.1		0.1		0.1		0.1	pF	1, 2, 3
C_{I_CA}	Input capacitance (CA[13:0] pins)	0.4	1.4	0.4	1.2	0.4	1.1	0.4	1.0	pF	1, 2, 5, 12
$C_{I_CS_n}$	Input capacitance (CS_n pin)	0.2	0.7	0.2	0.6	0.2	0.55	0.2	0.5	pF	1, 2, 6, 12
$C_{DI_CS_n}$	Input capacitance delta (CS_n pin only)	-0.2	0.2	-0.2	0.2	-0.2	0.2	-0.2	0.2	pF	1, 2, 7
C_{DI_CA}	Input capacitance delta (CA[13:0] pins only)	-0.2	0.2	-0.2	0.2	-0.2	0.2	-0.2	0.2	pF	1, 2, 8
C_{ALERT}	Input/output capacitance of ALERT	0.6	3.0	0.6	3.0	0.6	3.0	0.6	3.0	pF	1, 2
$C_{Loopback}$	Input/output capacitance of Loopback (LBDQ, LBDQS)	0.6	2.0	0.6	2.0	0.6	2.0	0.6	2.0	pF	1, 2
C_{ZQ}	Input capacitance of ZQ	-	5	-	5	-	5	-	5	pF	1, 2, 11, 13
C_{STRAP}	Input capacitance of MIR, CAI, CA_ODT pins	-	20	-	20	-	20	-	20	pF	1, 2, 10

NOTE 1 This parameter is not subject to production test. This parameter is measured by using vendor specific measurement methodology.
NOTE 2 This parameter applies to DDP only, but does not include RDL layer portion. RDL layer portion is covered in package electrical specification.
NOTE 3 Absolute value $C_{CK}(CK_t)$-$C_{CK}(CK_c)$.
NOTE 4 Absolute value of $C_{IO}(DQS_t)$-$C_{IO}(DQS_c)$.
NOTE 5 C_{I_CA} applies to CA[13:0] pins.
NOTE 6 $C_{I_CS_n}$ applies to CS_n pin and CS1_n pin individually.
NOTE 7 $C_{DI_CS_n} = 2*C_{I_CS_n}-0.5*(C_{CK}(CK_t)+C_{CK}(CK_c))$.
NOTE 8 $C_{DI_CA} = C_{I_CA[13:0]}-0.5*(C_{CK}(CK_t)+C_{CK}(CK_c))$.
NOTE 9 $C_{DIO} = C_{IO}(DQ,DM)-Avg(C_{IO}(DQ,DM))$.
NOTE 10 MIR and CA_ODT are strap pins used to configure module or point to point use cases depending on power, signal integrity, and termination requirements. No active AC signaling requirements defined for these pins.
NOTE 11 Maximum external load capacitance on ZQ pin: 25 pF. The ZQ functionality / accuracy with the max capacitive load is characterized.
NOTE 12 C_{I_CA}, $C_{I_CS_n}$ Options are incorporated VcIVW in Section 8.2.
NOTE 13 C_{ZQ} applies to ZQ pin and ZQ1 pin individually.

12 Input/Output Capacitance (cont'd)

Table 329 — DRAM Package Electrical Specifications (x4/x8)

Parameter	Symbol	DDR5-3200 to DDR5-4800		DDR5-5200 to DDR5-6400		DDR5-6800 to 9200		Unit	NOTE
		Min	Max	Min	Max	Min	Max		
Input/output Zpkg	Z_{pkg_DQ}	45	75	50	75	50	75	Ω	1, 2, 4, 5, 10
Input/output Pkg Delay	$T_{pkg_delay_DQ}$	10	35	10	32	10	32	ps	1, 3, 4, 5, 10
DQS_t, DQS_c Zpkg	Z_{pkg_DQS}	45	75	50	75	50	75	Ω	1, 2, 5,10, 12
DQS_t, DQS_c Pkg Delay	$T_{pkg_delay_DQS}$	10	35	10	32	10	32	ps	1, 3, 5, 10, 12
Delta Zpkg DQS_t, DQS_c	DZ_{pkg_DQS}	-	5	-	5	-	5	Ω	1, 2, 5, 7, 10
Delta Delay DQS_t, DQS_c	$DT_{pkg_delay_DQS}$	-	2	-	2	-	2	ps	1, 3, 5, 7, 10
Input- CTRL pins Zpkg	Z_{pkg_CTRL}	45	75	45	75	45	75	Ω	1, 2, 5, 9, 10
Input- CTRL pins Pkg Delay	$T_{pkg_delay_CTRL}$	10	35	10	28	10	28	ps	1, 3, 5, 9, 10
Input- CMD ADD pins Zpkg	Z_{pkg_CA}	45	75	45	75	45	75	Ω	1, 2, 5, 8, 10
Input- CMD ADD pins Pkg Delay	$T_{pkg_delay_CA}$	10	35	10	(Option 1) 35 (Option 2) 32 (Option 3) 29	10	(Option 1) 35 (Option 2) 32 (Option 3) 29	ps	1, 3, 5, 8, 10
CK_t & CK_c Zpkg	Z_{pkg_CK}	45	75	45	75	45	75	Ω	1, 2, 5, 10
CK_t & CK_c Pkg Delay	$T_{pkg_delay_CK}$	10	30	10	25	10	25	ps	1, 3, 5, 10
Delta Zpkg CK_t & CK_c	$DZ_{pkg_delay_CK}$	-	5	-	5	-	5	Ω	1, 2, 5, 6, 10
Delta Delay CK_t & CK_c	$DT_{pkg_delay_CK}$	-	2	-	2	-	2	ps	1, 3, 5, 6, 10
ALERT Zpkg	Z_{pkg_ALERT}	45	75	45	75	45	75	Ω	1, 2, 5, 10
ALERT Delay	$T_{pkg_delay_ALERT}$	10	60	10	60	10	60	ps	1, 3, 5, 10
Loopback Zpkg	$Z_{pkg_Loopback}$	45	75	45	75	45	75	Ω	1, 2, 5, 10, 11
Loopback Delay	$T_{pkg_delay_Loopback}$	10	60	10	60	10	60	ps	1, 3, 5, 10, 11

NOTE 1 This parameter is not subject to production test.

NOTE 2 This parameter is measured by using vendor specific measurement methodology to calculate the average Z_{pkg_xx} over the interval $T_{pkg_delay_xx}$

NOTE 3 This parameter is measured by using vendor specific measurement methodology.

NOTE 4 Z_{pkg_DQ} and $T_{pkg_delay_DQ}$ applies to DQ, DM

NOTE 5 This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here

NOTE 6 Absolute value of $Z_{pkg_CK_t}$ - $Z_{pkg_CK_c}$ for impedance(Z) or absolute value of $T_{pkg_delay_CK_t}$ - $T_{pkg_delay_CK_c}$ for delay (T_{pkg_delay}).

NOTE 7 Absolute value of Z_{pkg}(DQS_t)-Z_{pkg}(DQS_c) for impedance(Z) or absolute value of $T_{pkg_delay_DQS_t}$ - $T_{pkg_delay_DQS_c}$ for delay (T_{pkg_delay})

NOTE 8 Z_{pkg_CA} and $T_{pkg_delay_CA}$ applies to CA[13:0]

NOTE 9 Z_{pkg_CTRL} and $T_{pkg_delay_CTRL}$ applies to CS_n

NOTE 10 Package implementations shall meet spec if the designed Z_{pkg} and T_{pkg_delay} fall within the ranges shown.

NOTE 11 $Z_{pkg_Loopback}$ and $T_{pkg_delay_Loopback}$ applies to LBDQ and LBDQS.

NOTE 12 Z_{pkg_DQS} and $T_{pkg_delay_DQS}$ applies to DQS_t & DQS_c, TDQS_t and TDQS_c.

12 Input/Output Capacitance (cont'd)

Table 330 — DRAM Package Electrical Specifications (x16)

Parameter	Symbol	DDR5-3200 to DDR5-4800		DDR5-5200 to DDR5-9200		Unit	NOTE
		Min	Max	Min	Max		
Input/output Zpkg	Z_{pkg_DQ}	45	75	45	75	Ω	1, 2, 4, 5, 10
Input/output Pkg Delay	$T_{pkg_delay_DQ}$	10	40	10	38	ps	1, 3, 4, 5, 10
DQS_t, DQS_c Zpkg	Z_{pkg_DQS}	45	75	45	75	Ω	1, 2, 5, 10, 12
DQS_t, DQS_c Pkg Delay	$T_{pkg_delay_DQS}$	10	40	10	38	ps	1, 3, 5, 10, 12
Delta Zpkg DQS_t, DQS_c	DZ_{pkg_DQS}	-	5	-	5	Ω	1, 2, 5, 7, 10
Delta Delay DQS_t, DQS_c	$DT_{pkg_delay_DQS}$	-	2	-	2	ps	1, 3, 5, 7, 10
Input- CTRL pins Zpkg	Z_{pkg_CTRL}	45	75	45	75	Ω	1, 2, 5, 9, 10
Input- CTRL pins Pkg Delay	$T_{pkg_delay_CTRL}$	10	40	10	40	ps	1, 3, 5, 9, 10
Input- CMD ADD pins Zpkg	Z_{pkg_CA}	45	75	45	75	Ω	1, 2, 5, 8, 10
Input- CMD ADD pins Pkg Delay	$T_{pkg_delay_CA}$	10	45	10	44	ps	1, 3, 5, 8, 10
CK_t & CK_c Zpkg	Z_{pkg_CK}	45	75	45	75	Ω	1, 2, 5, 10
CK_t & CK_c Pkg Delay	$T_{pkg_delay_CK}$	10	45	10	43	ps	1, 3, 5, 10
Delta Zpkg CK_t & CK_c	$DZ_{pkg_delay_CK}$	-	5	-	5	Ω	1, 2, 5, 6, 10
Delta Delay CK_t & CK_c	$DT_{pkg_delay_CK}$	-	2	-	2	ps	1, 3, 5, 6, 10
ALERT Zpkg	Z_{pkg_ALERT}	45	75	45	75	Ω	1, 2, 5, 10
ALERT Delay	$T_{pkg_delay_ALERT}$	10	60	10	60	ps	1, 3, 5, 10
Loopback Zpkg	$Z_{pkg_Loopback}$	45	75	45	75	Ω	1, 2, 5, 10, 11
Loopback Delay	$T_{pkg_delay_Loopback}$	10	60	10	60	ps	1, 3, 5, 10, 11

NOTE 1 This parameter is not subject to production test.
NOTE 2 This parameter is measured by using vendor specific measurement methodology.
NOTE 3 This parameter is measured by using vendor specific measurement methodology.
NOTE 4 Z_{pkg_DQ} and $T_{pkg_delay_DQ}$ applies to DQ, DM.
NOTE 5 This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
NOTE 6 Absolute value of $Z_{pkg_CK_t}$ - $Z_{pkg_CK_c}$ for impedance(Z) or absolute value of $T_{pkg_delay_CK_t}$ - $T_{pkg_delay_CK_c}$ for delay (T_{pkg_delay}).
NOTE 7 Absolute value of Z_{pkg}(DQS_t)-Z_{pkg}(DQS_c) for impedance(Z) or absolute value of $T_{pkg_delay_DQS_t}$ - $T_{pkg_delay_DQS_c}$ for delay (T_{pkg_delay})
NOTE 8 Z_{pkg_CA} and $T_{pkg_delay_CA}$ applies to CA[13:0]
NOTE 9 Z_{pkg_CA} and $T_{pkg_delay_CTRL}$ applies to CS_n
NOTE 10 Package implementations shall meet spec if the designed Z_{pkg} and T_{pkg_delay} fall within the ranges shown.
NOTE 11 $Z_{pkg_Loopback}$ and $T_{pkg_delay_Loopback}$ applies to LBDQ and LBDQS.
NOTE 12 Z_{pkg_DQS} and $T_{pkg_delay_DQS}$ applies to DQS_t & DQS_c, TDQS_t & TDQS_c.

12 Input/Output Capacitance (cont'd)

Table 331 — DRAM DDP Package Electrical Specifications (x4/x8)

Parameter	Symbol	DDR5-3200 to DDR5-6400		Unit	NOTE
		Min	Max		
Input/output Zpkg	Z_{pkg_DQ}	20	75	Ω	1, 2, 3, 4, 9
Input/output Pkg Delay	$T_{pkg_delay_DQ}$	25	100	ps	1, 2, 3, 4, 9
DQS_t, DQS_c Zpkg	Z_{pkg_DQS}	20	75	Ω	1, 2, 4, 9, 11
DQS_t, DQS_c Pkg Delay	$T_{pkg_delay_DQS}$	25	100	ps	1, 2, 4, 9, 11
Delta Zpkg DQS_t, DQS_c	DZ_{pkg_DQS}	-	5	Ω	1, 2, 4, 6, 9
Delta Delay DQS_t, DQS_c	$DT_{pkg_delay_DQS}$	-	2	ps	1, 2, 4, 6, 9
Input- CTRL pins Zpkg	Z_{pkg_CTRL}	20	75	Ω	1, 2, 4, 8, 9
Input- CTRL pins Pkg Delay	$T_{pkg_delay_CTRL}$	25	100	ps	1, 2, 4, 8, 9
Input- CMD ADD pins Zpkg	Z_{pkg_CA}	20	75	Ω	1, 2, 4, 7, 9
Input- CMD ADD pins Pkg Delay	$T_{pkg_delay_CA}$	25	100	ps	1, 2, 4, 7, 9
CK_t & CK_c Zpkg	Z_{pkg_CK}	20	75	Ω	1, 2, 4, 9
CK_t & CK_c Pkg Delay	$T_{pkg_delay_CK}$	25	100	ps	1, 2, 4, 9
Delta Zpkg CK_t & CK_c	$DZ_{pkg_delay_CK}$	-	5	Ω	1, 2, 4, 5, 9
Delta Delay CK_t & CK_c	$DT_{pkg_delay_CK}$	-	2	ps	1, 2, 4, 5, 9
ALERT Zpkg	Z_{pkg_ALERT}	20	75	Ω	1, 2, 4, 9
ALERT Delay	$T_{pkg_delay_ALERT}$	25	100	ps	1, 2, 4, 9
Loopback Zpkg	$Z_{pkg_Loopback}$	20	75	Ω	1, 2, 4, 9, 10
Loopback Delay	$T_{pkg_delay_Loopback}$	25	100	ps	1, 2, 4, 9, 10

NOTE 1 This parameter is not subject to production test.
NOTE 2 This parameter is verified by design.
NOTE 3 Z_{pkg_DQ} and $T_{pkg_delay_DQ}$ applies to DQ, DM
NOTE 4 This parameter applies to DDPonly.
NOTE 5 Absolute value of $Z_{pkg_CK_t}$ - $Z_{pkg_CK_c}$ for impedance(Z) or absolute value of $T_{pkg_delay_CK_t}$ - $T_{pkg_delay_CK_c}$ for delay (T_{pkg_delay}).
NOTE 6 Absolute value of Z_{pkg}(DQS_t)-Z_{pkg}(DQS_c) for impedance(Z) or absolute value of $T_{pkg_delay_DQS_t}$ - $T_{pkg_delay_DQS_c}$ for delay (T_{pkg_delay})
NOTE 7 Z_{pkg_CA} and $T_{pkg_delay_CA}$ applies to CA[13:0]
NOTE 8 Z_{pkg_CTRL} and $T_{pkg_delay_CTRL}$ applies to CS_n and CS1_n
NOTE 9 Package implementations shall meet spec if the designed Z_{pkg} and T_{pkg_delay} fall within the ranges shown.
NOTE 10 $Z_{pkg_Loopback}$ and $T_{pkg_delay_Loopback}$ applies to LBDQ and LBDQS.
NOTE 11 Z_{pkg_DQS} and $T_{pkg_delay_DQS}$ applies to DQS_t & DQS_c, TDQS_t & TDQS_c.

12.1 Electrostatic Discharge Sensitivity Characteristics

Table 332 — Electrostatic Discharge Sensitivity Characteristics

Parameter [1]	Symbol	Min	Max	Unit	Notes
Human body model (HBM)	ESDHBM	1000	-	V	2
Charged-device model (CDM)	ESD_{CDM}	250	-	V	3

NOTE 1 State-of-the-art basic ESD control measures have to be in place when handling devices
NOTE 2 Refer to ESDA / JEDEC Joint Standard JS-001 for measurement procedures.
NOTE 3 Refer to ESDA / JEDEC Joint Standard JS-002 f for measurement procedures

13 Electrical Characteristics and AC Timing

13.1 Reference Load for AC Timing and Output Slew Rate - No Ballot

Figure 256 represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

Ron nominal of DQ, DQS_t and DQS_c drivers uses 34 ohms to specify the relevant AC timing parameter values of the device.

The maximum DC High level of Output signal = 1.0 * VDDQ,

The minimum DC Low level of Output signal = { 34 /(34 + 50) } *VDDQ = 0.4* VDDQ

The nominal reference level of an Output signal can be approximated by the following:

The center of maximum DC High and minimum DC Low = { (1 + 0.4) / 2 } * VDDQ = 0.7 * VDDQ

The actual reference level of Output signal might vary with driver Ron and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye. Prior to measuring AC parameters, the reference level of the verification tool should be set to an appropriate level.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

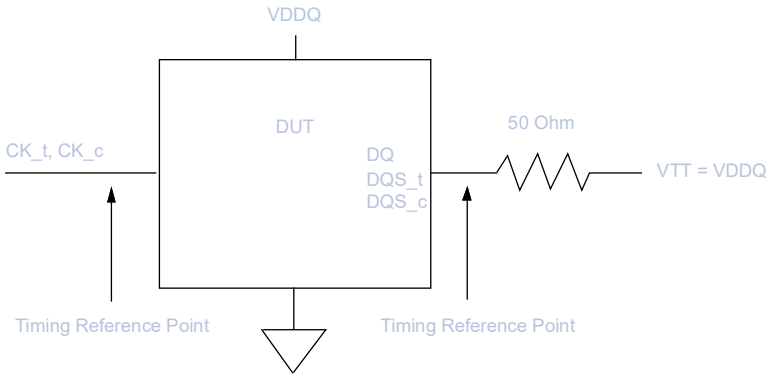


Figure 256 — Reference Load for AC Timing and Output Slew Rate

13.2 Rounding Definitions and Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 2200 MHz (4400 MT/s) for the DDR5-4400 speed bin, which mathematically yields a nominal clock period tCK(AVG) of 0.454545... ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be used. The DDR5 SDRAM specification establishes a minimum granularity for timing parameters of 1 ps.

Rules for rounding must be defined to allow optimization of device performance without violating device parameters. All timing parameters specified in the time domain (ns, ps, etc.) which must then be converted to the clock domain (nCK units) shall be defined to align with these rules. The key point is, minimum and maximum timing parameter values shall generally use the same rounding rules used to define tCK(AVG)min and tCK(AVG)max. The resulting rounding algorithms rely on results that are within correction factors of device testing and specification to avoid losing performance due to rounding errors.

These rules are:

- DEFINING TIMING PARAMETER VALUES: Minimum and maximum timing parameter values, including tCK(AVG)min and tCK(AVG)max, are rounded down and to be defined to 1 ps of accuracy in the DDR5 SDRAM specification based on the non-rounded nominal tCK(AVG) for a given speed bin. If the nominal timing parameter values require more than 1 ps of accuracy, they can be rounded down (faster) to the next 1 ps according to the rounding algorithms, and the DDR5 SDRAM is responsible for absorbing the resulting small parameter extensions. In other words, the DDR5 SDRAM specification only lists the nominal parameter values rounded down to the next 1 ps. For example, this extends the DDR5-4400 tCK(AVG)min definition to be exactly 0.454 ns which is slightly smaller (faster) than the nominal memory clock period of 0.454545... ns by less than 1 ps.
- CALCULATING THE REAL MINIMUM TIMING PARAMETER VALUES: For minimum timing parameters, other than tCK(AVG)min, to avoid losing performance due to additional erroneous nCKs and to calculate the true real minimum values, their nominal values listed in the DDR5 SDRAM specification must be reduced (faster) by the maximum %error (correction factor) used to define tCK(AVG)min. The DDR5 SDRAM is responsible for absorbing the resulting small parameter extensions. For example, tWRmin has a nominal value of 30.000 ns, however, applying the 0.30% correction factor allows a more aggressive timing (for example, 29.910 ns) to be supported, which allows the intended smaller (faster) nCK value to be maintained when rounding tCK(AVG)min down to the next 1 ps. Note, parameter values defined to be 0 ps do not need to be reduced by a correction factor, and therefore don't require these rounding algorithms.
- CALCULATING THE REAL MAXIMUM TIMING PARAMETER VALUES: For maximum timing parameters, including tCK(AVG)max, to avoid losing performance due to excluding erroneous nCKs and to calculate the true real maximum values, their nominal values listed in the DDR5 SDRAM specification must be increased (slower) by the maximum %error caused by rounding tCK(AVG) down to the next 1 ps. The DDR5 SDRAM is responsible for absorbing the resulting small parameter extensions. For example, tREFImax has a nominal value of 3.9 µs. And the DDR5-8400 speed bin mathematically yields a nominal clock period tCK(AVG) of 0.238095... ns, resulting in a theoretical maximum %error of 0.42% (0.239 ns/0.238 ns-100%). So the true real tREFImax value is 3.916386... µs (3.9 µs*0.239 ns/ 0.238 ns) for the DDR5-8400 speed bin.
- ROUNDING ALGORITHM FOR MINIMUM TIMING PARAMETER VALUES: Round down only integer number math is commonly used in the industry to calculate nCK values. This rounding algorithm for minimum timing parameters uses scaling by 1000 to allow use of integer math. Nominal minimum timing parameters like tWRmin, tRCDmin, etc. which are programmed in systems in numbers of clocks (nCK) but expressed in units of time(ps), are rounded down to the next 1ps, multiplied by the scaled inverse correction factor (1000-3=997) prior to division by the application memory clock period rounded down to the next 1ps, and adding 1 scaled by 1000 to that result effectively adds 1nCK. Division by 1000 undoes the scaling effects, resulting in a number of clocks as the final answer which has been effectively rounded up to the next 1 nCK by adding 1nCK in the previous step and then rounding down to the next 1 nCK. The caveat is, effectively adding 1 prior to rounding down is mostly equivalent to rounding up except when the result is equal to an integer, in which case the result won't be rounded down as intended, and therefore performance would be lost. To address this, the maximum 0.28% correction factor needed for 3600 MHz (0.277ns/0.2777777...ns-100%) operation has been increased slightly to 0.30% in this rounding algorithms. This accounts for all integer boundary conditions, except for the specific case when the nominal minimum timing parameter value is defined to be 0 ps. No rounding is required for parameter values equal to 0 ps. This rounding algorithm is not optimized for parameter values that are less than or equal to 0ps, and may result in unintended lost performance if used for parameter values that are less than or equal to 0 ps.

$$nCK = truncate\left[\frac{\left(\frac{truncate[\text{parameter_nominal_in_ps}] \times 997}{truncate[\text{tCK(AVG)_real_in_ps}]}\right) + 1000}{1000}\right]$$

13.2 Rounding Definitions and Algorithms (cont'd)

- ROUNDING ALGORITHM FOR MAXIMUM TIMING PARAMETER VALUES: Round down only integer number math is commonly used in the industry to calculate nCK values. This rounding algorithm is used for maximum timing parameters. Nominal maximum timing parameters like tREFImax, etc., which programmed in systems in numbers of clocks (nCK) but expressed in units of time (ps), are rounded down to the next 1 ps prior to division by the application memory clock period rounded down to the next 1 ps, resulting in a number of clocks as the final answer which is rounded down to the next 1 nCK. No rounding is required for parameter values equal to 0 ps, but this rounding algorithm can still be used for parameter values equal to 0ps and no performance will be lost. This rounding algorithm is not optimized for parameter values that are less than 0 ps (negative parameter values), and may result in violating the parameter specification if used for parameter values that are less than 0 ps.

$$nCK = truncate\left[\frac{truncate[\text{parameter_nominal_in_ps}]}{truncate[tCKAVG)]}\right]$$

- CL ALGORITHM FOR STANDARD SPEED BINS: The math rounding algorithms shall be used for all timing parameters when converting from the time domain (ns, ps, etc.) to the clock domain (nCK units), except for when converting tAA to CL. If these rounding algorithms are used to convert tAA to CL, they'll return invalid CL's for some cases when down clocking (and the DIMM SPD CL Mask doesn't protect against all of these cases). The proper setting of CL shall be determined by the memory controller, either by using the speed bin tables, or by using the CL algorithm, or by some other means. Refer to the Speed Bins and Operations section for more information. Note, the CL algorithm replaces the need to use the DIMM SPD CL Mask.
- CL ALGORITHM FOR CUSTOM SPEED BINS: If the DDR5 SDRAM supports non-standard tCK, tAA, tRCD, and tRP speed bin timings, the CL algorithm will still only return valid CL's as defined in the speed bin tables, which may not be the intended CL's for non-standard speed bins. In these cases, the rounding algorithms may need to be used to convert tAA to CL, instead of the CL algorithm. The CL returned by the rounding algorithms shall be incremented up to the next supported CL according to the DIMM SPD CL Mask. Consult the memory vendor for more information.

13.2.1 Example 1, Using Integer Math to Convert $t_{WR(min)}$ from ns to nCK

```
// This algorithm reduces the nominal minimum timing parameter value by a 0.30% correction factor,
// rounds tCK(AVG) down, calculates nCK, adds 1 nCK, and rounds nCK down to the next integer value

int TwrMin, Correction, ClockPeriod, TempTwr, TempNck, TwrInNck;

TwrMin      = 30000;                        // tWRmin in ps
Correction  = 3                             // 0.30% per the rounding algorithm
ClockPeriod = ApplicationTck;               // Clock period in ps is application specific
TempTwr     = TwrMin * (1000 - Correction); // Apply correction factor, scaled by 1000
TempNck     = TempTwr / ClockPeriod ;       // Initial nCK calculation, scaled by 1000
TempNck     = TempNck + 1000;               // Add 1, scaled by 1000, to effectively round up
TwrInNck    = (int)(TempNck / 1000);        // Round down to next integer
```

Table 333 — Example 1, Using Round Down only Integer Number Math

DDR5 Device Operating at Standard Application Frequencies Timing Parameter: tWR(min) = 30.000 ns = 30000 ps					
Application Speed Grade	**Device tWR**	**Application tCK**	**Device tWR / Application tCK**	**Device tWR * (1000 - Correction) / Application tCK + 1000**	**Truncate Corrected nCK / 1000**
MT/s	**ps**	**ps**	**nCK (real)**	**scaled nCK (corrected)**	**nCK (integer)**
3200	30000	625	48.00	48856	48
3600	30000	555	54.05	54891	54
4000	30000	500	60.00	60820	60
4400	30000	454	66.08	66881	66
4800	30000	416	72.12	72899	72

13.3 Timing Parameters by Speed Grade

The analog timing parameters in this section have been defined based on nominal tCA(avg)min according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

13.3.1 Timing Parameters for DDR5-3200 to DDR5-4000

Table 334 — Timing Parameters for DDR5-3200 to DDR5-4000

Speed		DDR5-3200		DDR5-3600		DDR5-4000		Units	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock Timing									
Average Clock Period	tCK(avg)	0.625	-	0.555	-	0.500	-	ns	1
Command and Address Timing									
Read to Read command delay for same bank in same bank group	tCCD_L	Max(RBL/2, 5ns)						nCK,ns	8
Write to Write command delay for same bank in same bank group	tCCD_L_WR	Max(32nCK, 20ns)						nCK,ns	8
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	Max(16nCK, 10ns)						nCK,ns	8
Read to Write command delay for same bank group	tCCD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3, 5, 6, 8
Write to Read command delay for same bank in same bank group	tCCD_L_WTR	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4, 6, 8
Read to Read command delay for different bank in same bank group	tCCD_M	tCCD_L						nCK,ns	8
Write to Write command delay for different bank in same bank group	tCCD_M_WR	tCCD_L_WR						nCK,ns	8
Write to Read command delay for different bank in same bank group	tCCD_M_WTR	tCCD_L_WTR						nCK,ns	4, 6, 8
Read to Read command delay for different bank group	tCCD_S	RBL/2						nCK	8
Write to Write command delay for different bank group	tCCD_S_WR	WBL/2						nCK	8
Read to Write command delay for different bank group	tCCD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3, 5, 6, 8
Write to Read command delay for different bank group	tCCD_S_WTR	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4, 6, 8
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA	CWL + WBL/2 + tWR - tRTP						nCK,ns	2, 4, 6, 8
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(8nCK, 5ns)						nCK,ns	8
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(8nCK, 5ns)						nCK,ns	8
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8						nCK	8
Activate to Activate command delay to different bank group for 2 KB page size	tRRD_S(2K)	8						nCK	8
Four activate window for 1 KB page size	tFAW (1K)	Max(32nCK, 20.000ns)	-	Max(32nCK, 17.777ns)	-	Max(32nCK, 16.000ns)	-	nCK, ns	
Four activate window for 2 KB page size	tFAW (2K)	Max(40nCK, 25.000ns)	-	Max(40nCK, 22.222ns)	-	Max(40nCK, 20.000ns)	-	nCK, ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)						nCK,ns	8
Precharge to Precharge command delay	tPPD	2						nCK	7, 8
Write recovery time	tWR	30						ns	8

13.3.2 Timing Parameters for DDR-4400 to DDR5-5200

The analog timing parameters in this section have been defined based on nominal tCK(avg)min according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 335 — Timing Parameters for DDR5-4400 to DDR5-5200

Speed		DDR5-4400		DDR5-4800		DDR5-5200		Units	NOTE
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock Timing									
Average Clock Period	tCK(avg)	0.454	-	0.416	-	0.384	-	ns	1
Command and Address Timing									
Read to Read command delay for same bank in same bank group	tCCD_L	Max(RBL/2, 5ns)						nCK,ns	8
Write to Write command delay for same bank in same bank group	tCCD_L_WR	Max(32nCK, 20ns)						nCK,ns	8
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	Max(16nCK, 10ns)						nCK,ns	8
Read to Write command delay for same bank group	tCCD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3, 5, 6, 8
Write to Read command delay for same bank in same bank group	tCCD_L_WTR	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4, 6, 8
Read to Read command delay for different bank in same bank group	tCCD_M	tCCD_L						nCK,ns	8
Write to Write command delay for different bank in same bank group	tCCD_M_WR	tCCD_L_WR						nCK,ns	8
Write to Read command delay for different bank in same bank group	tCCD_M_WTR	tCCD_L_WTR						nCK,ns	4, 6, 8
Read to Read command delay for different bank group	tCCD_S	RBL/2						nCK	8
Write to Write command delay for different bank group	tCCD_S_WR	WBL/2						nCK	8
Read to Write command delay for different bank group	tCCD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3, 5, 6, 8
Write to Read command delay for different bank group	tCCD_S_WTR	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4, 6, 8
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA	CWL + WBL/2 + tWR - tRTP						nCK,ns	2, 4, 6, 8
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(8nCK, 5ns)						nCK,ns	8
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(8nCK, 5ns)						nCK,ns	8
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8						nCK	8
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8						nCK	8
Four activate window for 1 KB page size	tFAW (1K)	Max(32nCK, 14.545ns)	-	Max(32nCK, 13.333ns)	-	Max(32nCK, 12.307ns)	-	nCK, ns	
Four activate window for 2 KB page size	tFAW (2K)	Max(40nCK, 18.181ns)	-	Max(40nCK, 16.666ns)	-	Max(40nCK, 15.384ns)	-	nCK, ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)						nCK,ns	8
Precharge to Precharge command delay	tPPD	2						nCK	7, 8
Write recovery time	tWR	30						ns	8

13.3.3 Timing Parameters for DDR-5600 to DDR5-6400

Analog timing parameters in this section have been defined on nominal tCK(avg)min according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 336 — Timing Parameters for DDR5-5600 to DDR5-6400

Speed		DDR5-5600		DDR5-6000		DDR5-6400		Units	NOTE
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock Timing									
Average Clock Period	tCK(avg)	0.357	-	0.333	-	0.312	-	ns	1
Command and Address Timing									
Read to Read command delay for same bank in same bank group	tCCD_L	Max(RBL/2, 5ns)						nCK,ns	8
Write to Write command delay for same bank in same bank group	tCCD_L_WR	Max(32nCK, 20ns)						nCK,ns	8
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	Max(16nCK, 10ns)						nCK,ns	8
Read to Write command delay for same bank group	tCCD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3, 5, 6, 8
Write to Read command delay for same bank in same bank group	tCCD_L_WTR	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4, 6, 8
Read to Read command delay for different bank in same bank group	tCCD_M	tCCD_L						nCK,ns	8
Write to Write command delay for different bank in same bank group	tCCD_M_WR	tCCD_L_WR						nCK,ns	8
Write to Read command delay for different bank in same bank group	tCCD_M_WTR	tCCD_L_WTR						nCK,ns	4, 6, 8
Read to Read command delay for different bank group	tCCD_S	RBL/2						nCK	8
Write to Write command delay for different bank group	tCCD_S_WR	WBL/2						nCK	8
Read to Write command delay for different bank group	tCCD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3, 5, 6, 8
Write to Read command delay for different bank group	tCCD_S_WTR	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4, 6, 8
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA	CWL + WBL/2 + tWR - tRTP						nCK,ns	2, 4, 6, 8
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(8nCK, 5ns)						nCK,ns	8
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(8nCK, 5ns)						nCK,ns	8
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8						nCK	8
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8						nCK	8
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK, 11.428ns)	-	Max(32nCK, 10.666ns)	-	Max(32nCK, 10.000ns)	-	nCK, ns	
Four activate window for 2KB page size	tFAW (2K)	Max(40nCK, 14.285ns)	-	Max(40nCK, 13.333ns)	-	Max(40nCK, 12.500ns)	-	nCK, ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)						nCK,ns	8
Precharge to Precharge command delay	tPPD	2						nCK	7, 8
Write recovery time	tWR	30						ns	8

13.3.4 Timing Parameters for DDR-6800 to DDR5-7600

The analog timing parameters in this section have been defined based on nominal tCK(avg)min according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 337 — Timing Parameters for DDR5-6800 to DDR5-7600

Speed		DDR5-6800		DDR5-7200		DDR5-7600		Units	NOTE
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Average Clock Period	tCK(avg)	0.294	-	0.277	-	0.263	-	ns	1
Command and Address Timing									
Read to Read command delay for same bank in same bank group	tCCD_L	max(RBL/2,5ns)				max(RBL/2,5ns)		nCK,ns	8
Write to Write command delay for same bank in same bank group	tCCD_L_WR	max(32nCK,20ns)				max(32nCK,20ns)		nCK,ns	8
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	Max(16nCK,10ns)				Max(16nCK,10ns)		nCK,ns	8
Read to Write command delay for same bank group	tCCD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE				CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE		nCK,ns	3, 5, 6, 8
Write to Read command delay for same bank in same bank group	tCCD_L_WTR	CWL + WBL/2 + Max(16nCK,10ns)				CWL + WBL/2 + Max(16nCK,10ns)		nCK,ns	4, 6, 8
Read to Read command delay for different bank in same bank group	tCCD_M	max(8nCK, 4.705ns)	-	max(8nCK, 4.444ns)	-	max(8nCK, 4.210ns)	-	nCK,ns	
Write to Write command delay for different bank in same bank group	tCCD_M_WR	max(32nCK, 18.823ns)	-	max(32nCK, 17.777ns)	-	max(32nCK, 16.842ns)	-	nCK,ns	
Write to Read command delay for different bank in same bank group	tCCD_M_WTR	CWL+WBL/2 +Max(16nCK, 9.411ns)	-	CWL+WBL/2 +Max(16nCK, 8.888ns)	-	CWL+WBL/2 +Max(16nCK, 8.421ns)	-	nCK,ns	4, 6
Read to Read command delay for different bank group	tCCD_S	RBL/2						nCK	8
Write to Write command delay for different bank group	tCCD_S_WR	WBL/2						nCK	8
Read to Write command delay for different bank group	tCCD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE				CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE		nCK,ns	3, 5, 6, 8
Write to Read command delay for different bank group	tCCD_S_WTR	CWL+WBL/2 +Max(4nCK, 2.352ns)	-	CWL+WBL/2 +Max(4nCK, 2.222ns)	-	CWL+WBL/2 +Max(4nCK, 2.105ns)	-	nCK,ns	4, 6
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA	CWL + WBL/2 + tWR - tRTP				CWL + WBL/2 + tWR - tRTP		nCK,ns	2, 4, 6, 8
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	max(8nCK, 4.705ns)	-	max(8nCK, 4.444ns)	-	max(8nCK, 4.210ns)	-	nCK,ns	
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	max(8nCK, 4.705ns)	-	max(8nCK, 4.444ns)	-	max(8nCK, 4.210ns)	-	nCK,ns	
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8				8		nCK	8
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8				8		nCK	8
Four activate window for 1KB page size	tFAW(1K)	Max(32nCK, 9.411ns)	-	Max(32nCK, 8.888ns)	-	Max(32nCK, 8.421ns)	-	nCK,ns	
Four activate window for 2KB page size	tFAW(2K)	Max(40nCK, 11.764ns)	-	Max(40nCK, 11.111ns)	-	Max(40nCK, 10.526ns)	-	nCK,ns	
Read to Precharge command delay	tRTP	Max(12nCK,7.5ns)				Max(12nCK,7.5ns)		nCK,ns	8
Precharge to Precharge command delay	tPPD	2				4		nCK	7, 8
Write recovery time	tWR	30				30		ns	8

13.3.5 Timing Parameters for DDR-8000 to DDR5-8800

The analog timing parameters in this section have been defined based on nominal tCK(avg)min according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 338 — Timing Parameters for DDR5-8000 to DDR5-8800

Speed		DDR5-8000		DDR5-8400		DDR5-8800		Units	NOTE
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Average Clock Period	**tCK(avg)**	**0.250**	**-**	**0.238**	**-**	**0.227**	**-**	ns	1
Command and Address Timing									
Read to Read command delay for same bank in same bank group	tCCD_L	Max(RBL/2, 5ns)						nCK,ns	8
Write to Write command delay for same bank in same bank group	tCCD_L_WR	Max(32nCK, 20ns)						nCK,ns	8
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	Max(16nCK, 10ns)						nCK,ns	8
Read to Write command delay for same bank group	tCCD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3, 5, 6, 8
Write to Read command delay for same bank in same bank group	tCCD_L_ WTR	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4, 6, 8
Read to Read command delay for different bank in same bank group	tCCD_M	max(8nCK, 4.000ns)	-	max(8nCK, 4.000ns)	-	max(8nCK, 3.863ns)	-	nCK,ns	
Write to Write command delay for different bank in same bank group	tCCD_M_WR	max(32nCK, 16.000ns)	-	max(32nCK, 15.238ns)	-	max(32nCK, 14.545ns)	-	nCK,ns	
Write to Read command delay for different bank in same bank group	tCCD_M_WTR	CWL+WBL/ 2+Max(16nCK, 8.000ns)	-	CWL+WBL/ 2+Max(16nCK, 7.619ns)	-	CWL+WBL/ 2+Max(16nCK, 7.272ns)	-	nCK,ns	4, 6, 8
Read to Read command delay for different bank group	tCCD_S	RBL/2						nCK	8
Write to Write command delay for different bank group	tCCD_S_WR	WBL/2						nCK	8
Read to Write command delay for different bank group	tCCD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3, 5, 6, 8
Write to Read command delay for different bank group	tCCD_S_ WTR	CWL + WBL/2 + Max(4nCK, 2.000ns)	-	CWL + WBL/2 + Max(4nCK, 1.904ns)	-	CWL + WBL/2 + Max(4nCK, 1.818ns)	-	nCK,ns	4, 6, 8
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA	CWL + WBL/2 + tWR - tRTP						nCK,ns	2, 4, 6, 8
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(8nCK, 4.000ns)	-	max(8nCK, 4.000ns)	-	max(8nCK, 3.863ns)	-	nCK,ns	
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(8nCK, 4.000ns)	-	max(8nCK, 4.000ns)	-	max(8nCK, 3.863ns)	-	nCK,ns	
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8						nCK	8
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8						nCK	8
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK, 8.000ns)	-	Max(32nCK, 7.619ns)	-	Max(32nCK, 7.272ns)	-	nCK, ns	
Four activate window for 2KB page size	tFAW (2K)	Max(40nCK, 10.000ns)	-	Max(40nCK, 9.523ns)	-	Max(40nCK, 9.090ns)	-	nCK, ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)						nCK,ns	8
Precharge to Precharge command delay	tPPD	4						nCK	7, 8
Write recovery time	tWR	30						ns	8

13.3.6 Timing Parameters for DDR-9200

The analog timing parameters in this section have been defined based on nominal tCK(avg)min according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 339 — Timing Parameters for DDR5-9200

Speed		DDR5-9200		Units	NOTE
Parameter	Symbol	Min	Max		
Average Clock Period	**tCK(avg)**	**0.217**	**-**	ns	1
Command and Address Timing					
Read to Read command delay for same bank in same bank group	tCCD_L	max(RBL/2,5ns)		nCK,ns	8
Write to Write command delay for same bank in same bank group	tCCD_L_WR	max(32nCK,20ns)		nCK,ns	8
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	max(16nCK,10ns)		nCK,ns	8
Read to Write command delay for same bank group	tCCD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE		nCK,ns	3, 5, 6, 8
Write to Read command delay for same bank in same bank group	tCCD_L_ WTR	CWL + WBL/2 + Max(16nCK,10ns)		nCK,ns	4, 6, 8
Read to Read command delay for different bank in same bank group	tCCD_M	max(8nCK, 3.863ns)	-	nCK,ns	
Write to Write command delay for different bank in same bank group	tCCD_M_WR	max(32nCK, 14.782ns)	-	nCK,ns	
Write to Read command delay for different bank in same bank group	tCCD_M_WTR	CWL+WBL/2 +Max(16nCK, 6.956ns)	-	nCK,ns	4, 6, 8
Read to Read command delay for different bank group	tCCD_S	RBL/2		nCK	8
Write to Write command delay for different bank group	tCCD_S_WR	WBL/2		nCK	8
Read to Write command delay for different bank group	tCCD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE		nCK,ns	3, 5, 6, 8
Write to Read command delay for different bank group	tCCD_S_ WTR	CWL+WBL/2 +Max(4nCK, 1.739ns)	-	nCK,ns	4, 6, 8
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA	CWL + WBL/2 + tWR - tRTP		nCK,ns	2, 4, 6, 8
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	max(8nCK, 3.695ns)	-	nCK,ns	
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	max(8nCK, 3.695ns)	-	nCK,ns	
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8		nCK	8
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8		nCK	8
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK, 6.956ns)	-	nCK, ns	
Four activate window for 2KB page size	tFAW (2K)	Max(40nCK, 8.695ns)	-	nCK, ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)		nCK,ns	8
Precharge to Precharge command delay	tPPD	4		nCK	7, 8
Write recovery time	tWR	30		ns	8

Timing Parameters Table Notes for Mono DDR5-3200 to Mono-DDR5-9200:

1. tCK(avg)min listed for reference only, refer to the Speed Bins and Operations section which lists all valid tCK(avg) values.
2. tCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + tWR(min) - tRTP(min), and when using the appropriate rounding algorithms, nCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + nWR(min) - nRTP(min).
3. RBL: Read burst length associated with Read command:
   RBL = 32 (36 w/ RCRC on) for fixed BL32 and BL32 in BL32 OTF mode
   RBL = 16 (18 w/ RCRC on) for fixed BL16 and BL16 in BL32 OTF mode
   RBL = 16 (18 w/ RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
4. WBL: Write burst length associated with Write command:
   WBL = 32 (36 w/ WCRC on) for fixed BL32 and BL32 in BL32 OTF mode
   WBL = 16 (18 w/ WCRC on) for fixed BL16 and BL16 in BL32 OTF mode
   WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
5. The following is considered for tRTW equation:
   1tCK needs to be added due to tDQS2CK
   Read DQS offset timing can pull in the tRTW timing
   1tCK needs to be added when 1.5tCK postamble
6. CWL=CL-2
7. tPPD applies to any combination of precharge commands (PREab, PREsb, PREpb). tPPD also applies to any combination of precharge commands to a different die in a 3DS DDR5 SDRAM.
8. This parameter only specifies minimum values (there is no maximum value). The maximum value cells have been merged in the table to improve legibility.

13.3.7 Timing Parameters for 3DS-DDR5-3200 to 3DS-DDR5-4000 x4 2H and 4H

Analog timing parameters defined in this section are to be rounded to 1 ps of accuracy. Parameter min values which scale with tCKmin are to be defined using the tCKmin in the associated data rate.

Table 340 — Timing Parameters for x4 2H and 4H 3DS-DDR5-3200 to 3DS-DDR5-4000

Speed		DDR5-3200		DDR5-3600		DDR5-4000		Units	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock Timing									
Average Clock Period	tCK(avg)	0.625	-	0.555	-	0.500	-	ns	1
Command and Address Timing for 3DS									
Read to Read command delay for same bank group in same logical rank	tCCD_L_slr	Max(RBL/2, 5ns)						nCK,ns	15
Write to Write command delay for same bank group in same logical rank	tCCD_L_ WR_slr	Max(32nCK, 20ns)						nCK,ns	15
Write to Write command delay for same bank group in same logical rank, second write not RMW	tCCD_L_ WR2_slr	Max(16nCK, 10ns)						nCK,ns	15
Read to Write command delay for same bank group in same logical rank	tCCD_L_ RTW_slr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3, 5, 6
Write to Read command delay for same bank group in same logical rank	tCCD_L_ WTR_slr	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4, 6
Read to Read command delay for different bank in same bank group	tCCD_M_slr	tCCD_L_slr						nCK,ns	15
Write to Write command delay for different bank in same bank group	tCCD_M_WR_slr	tCCD_L_WR_slr						nCK,ns	15
Write to Read command delay for different bank in same bank group	tCCD_M_WTR_slr	tCCD_L_WTR_slr						nCK,ns	4, 6, 15
Read to Read command delay for different bank group in same logical rank	tCCD_S_slr	RBL/2						nCK	15
Write to Write command delay for different bank group in same logical rank	tCCD_S_ WR_slr	WBL/2						nCK	15
Read to Write command delay for different bank group in same logical rank	tCCD_S_ RTW_slr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3, 5, 6
Write to Read command delay for different bank group in same logical rank	tCCD_S_ WTR_slr	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4, 6
Write to Read with Auto Precharge command for same bank in same logic rank	tCCD_ WTRA_slr	CWL + WBL/2 + tWR_slr - tRTP_slr						nCK,ns	2, 4, 6
Activate to Activate command delay to same bank group in the same logical rank	tRRD_L_ slr(1K)	Max(8nCK, 5ns)						nCK,ns	15
Activate to Activate command delay to different bank group in the same logical rank	tRRD_S_ slr(1K)	8						nCK	15
Four activate window to the same logical rank	tFAW_ slr(1K)	max(32nCK, 20.000ns)	-	max(32nCK, 17.777ns)	-	max(32nCK, 16.000ns)	-	nCK, ns	9
Read command to Precharge command delay in same logical rank	tRTP_slr	Max(12nCK, 7.5ns)						nCK,ns	15
Precharge to Precharge delay in same logical rank	tPPD_slr	2						nCK	7, 15
Write recovery time in same logical rank	tWR_slr	30						ns	15
Read to Read command delay in different logical ranks	tCCD_dlr	Max(8nCK, 5.000ns)	-	Max(8nCK, 4.444ns)	-	Max(8nCK, 4.000ns)	-	nCK,ns	
Write to Write command delay in different logical ranks	tCCD_ WR_dlr	Max(8nCK, 5.000ns)	-	Max(8nCK, 4.444ns)	-	Max(8nCK, 4.000ns)	-	nCK,ns	12
Read to Write command delay in different logical ranks	tCCD_ RTW_dlr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3, 5, 6
Write to Read command delay in different logical ranks	tCCD_ WTR_dlr	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4, 6
Activate to Activate command delay to different logical ranks	tRRD_dlr	Max(4nCK, 2.500ns)	-	Max(4nCK, 2.222ns)	-	Max(4nCK, 2.000ns)	-	nCK,ns	
Four activate window to different logical ranks	tFAW_dlr	Max(16nCK, 10.000ns)	-	Max(16nCK, 8.888ns)	-	Max(16nCK, 8.000ns)	-	nCK,ns	
Precharge to Precharge delay in different logical rank	tPPD_dlr	2						nCK	7, 15
Activate window by DIMM channel	tDCAW	128						nCK	10, 11, 13, 14, 15
DIMM Channel Activate Command Count in tDCAW	nDCAC	32						ACT	10, 11, 13, 14, 16

13.3.8 Timing Parameters for 3DS-DDR5-4400 to 3DS-DDR5-5200 x4 2H and 4H

Analog timing parameters defined in this section are to be rounded to 1 ps of accuracy. Parameter min values which scale with tCKmin are to be defined using the tCKmin in the associated data rate.

Table 341 — Timing Parameters for x4 2H and 4H 3DS-DDR5-4400 to 3DS-DDR5-5200

Speed		DDR5-4400		DDR5-4800		DDR5-5200		Units	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock Timing									
Average Clock Period	tCK(avg)	0.454	-	0.416	-	0.384	-	ns	1
Command and Address Timing for 3DS									
Read to Read command delay for same bank group in same logical rank	tCCD_L_slr	Max(RBL/2, 5ns)						nCK,ns	15
Write to Write command delay for same bank group in same logical rank	tCCD_L_ WR_slr	Max(32nCK, 20ns)						nCK,ns	15
Write to Write command delay for same bank group in same logical rank, second write not RMW	tCCD_L_ WR2_slr	Max(16nCK, 10ns)						nCK,ns	15
Read to Write command delay for same bank group in same logical rank	tCCD_L_ RTW_slr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3, 5, 6
Write to Read command delay for same bank group in same logical rank	tCCD_L_ WTR_slr	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4, 6
Read to Read command delay for different bank in same bank group	tCCD_M_slr	tCCD_L_slr						nCK,ns	15
Write to Write command delay for different bank in same bank group	tCCD_M_WR_slr	tCCD_L_WR_slr						nCK,ns	15
Write to Read command delay for different bank in same bank group	tCCD_M_WTR_slr	tCCD_L_WTR_slr						nCK,ns	4, 6, 15
Read to Read command delay for different bank group in same logical rank	tCCD_S_slr	RBL/2						nCK	15
Write to Write command delay for different bank group in same logical rank	tCCD_S_ WR_slr	WBL/2						nCK	15
Read to Write command delay for different bank group in same logical rank	tCCD_S_ RTW_slr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3, 5, 6
Write to Read command delay for different bank group in same logical rank	tCCD_S_ WTR_slr	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4, 6
Write to Read with Auto Precharge command for same bank in same logic rank	tCCD_ WTRA_slr	CWL + WBL/2 + tWR_slr - tRTP_slr						nCK,ns	2, 4, 6
Activate to Activate command delay to same bank group in the same logical rank	tRRD_L_ slr(1K)	Max(8nCK, 5ns)						nCK,ns	15
Activate to Activate command delay to different bank group in the same logical rank	tRRD_S_ slr(1K)	8						nCK	15
Four activate window to the same logical rank	tFAW_ slr(1K)	max(32nCK, 14.545ns)	-	max(32nCK, 13.333ns)	-	max(32nCK, 12.307ns)	-	nCK, ns	9
Read command to Precharge command delay in same logical rank	tRTP_slr	Max(12nCK, 7.5ns)						nCK,ns	15
Precharge to Precharge delay in same logical rank	tPPD_slr	2						nCK	7, 15
Write recovery time in same logical rank	tWR_slr	30						ns	15
Read to Read command delay in different logical ranks	tCCD_dlr	Max(8nCK, 3.636ns)	-	Max(8nCK, 3.333ns)	-	Max(8nCK, 3.333ns)	-	nCK,ns	
Write to Write command delay in different logical ranks	tCCD_ WR_dlr	Max(8nCK, 3.636ns)	-	Max(8nCK, 3.333ns)	-	Max(8nCK, 3.333ns)	-	nCK,ns	12
Read to Write command delay in different logical ranks	tCCD_ RTW_dlr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3, 5, 6
Write to Read command delay in different logical ranks	tCCD_ WTR_dlr	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4, 6
Activate to Activate command delay to different logical ranks	tRRD_dlr	Max(4nCK, 1.818ns)	-	Max(4nCK, 1.666ns)	-	Max(4nCK, 1.666ns)	-	nCK,ns	
Four activate window to different logical ranks	tFAW_dlr	Max(16nCK, 7.272ns)	-	Max(16nCK, 6.666ns)	-	Max(16nCK, 6.666ns)	-	nCK,ns	
Precharge to Precharge delay in different logical rank	tPPD_dlr	2						nCK	7, 15
Activate window by DIMM channel	tDCAW	128						nCK	10, 11, 13, 14, 15
DIMM Channel Activate Command Count in tDCAW	nDCAC	32						ACT	10, 11, 13, 14, 16

13.3.9 Timing Parameters for 3DS-DDR5-5600 to 3DS-DDR5-6400 x4 2H and 4H

Analog timing parameters defined in this section are to be rounded to 1 ps of accuracy. Parameter min values which scale with tCKmin are to be defined using the tCKmin in the associated data rate.

Table 342 — Timing Parameters for x4 2H and 4H 3DS-DDR5-5600 to 3DS-DDR5-6400

Speed		DDR5-5600		DDR5-6000		DDR5-6400		Units	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock Timing									
Average Clock Period	tCK(avg)	0.357	-	0.333	-	0.312	-	ns	1
Command and Address Timing for 3DS									
Read to Read command delay for same bank group in same logical rank	tCCD_L_slr	Max(RBL/2, 5ns)						nCK,ns	15
Write to Write command delay for same bank group in same logical rank	tCCD_L_ WR_slr	Max(32nCK, 20ns)						nCK,ns	15
Write to Write command delay for same bank group in same logical rank, second write not RMW	tCCD_L_ WR2_slr	Max(16nCK, 10ns)						nCK,ns	15
Read to Write command delay for same bank group in same logical rank	tCCD_L_ RTW_slr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3, 5, 6
Write to Read command delay for same bank group in same logical rank	tCCD_L_ WTR_slr	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4, 6
Read to Read command delay for different bank in same bank group	tCCD_M_slr	tCCD_L_slr						nCK,ns	15
Write to Write command delay for different bank in same bank group	tCCD_M_WR_slr	tCCD_L_WR_slr						nCK,ns	15
Write to Read command delay for different bank in same bank group	tCCD_M_WTR_slr	tCCD_L_WTR_slr						nCK,ns	4, 6, 15
Read to Read command delay for different bank group in same logical rank	tCCD_S_slr	RBL/2						nCK	15
Write to Write command delay for different bank group in same logical rank	tCCD_S_ WR_slr	WBL/2						nCK	15
Read to Write command delay for different bank group in same logical rank	tCCD_S_RTW_slr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3, 5, 6
Write to Read command delay for different bank group in same logical rank	tCCD_S_WTR_slr	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4, 6
Write to Read with Auto Precharge command for same bank in same logic rank	tCCD_WTRA_slr	CWL + WBL/2 + tWR_slr - tRTP_slr						nCK,ns	2, 4, 6
Activate to Activate command delay to same bank group in the same logical rank	tRRD_L_slr(1K)	Max(8nCK, 5ns)						nCK,ns	15
Activate to Activate command delay to different bank group in the same logical rank	tRRD_S_slr(1K)	8						nCK	15
Four activate window to the same logical rank	tFAW_slr(1K)	max(32nCK, 11.428ns)	-	max(32nCK, 10.666ns)	-	max(32nCK, 10.000ns)	-	nCK, ns	9
Read command to Precharge command delay in same logical rank	tRTP_slr	Max(12nCK, 7.5ns)						nCK,ns	15
Precharge to Precharge delay in same logical rank	tPPD_slr	2						nCK	7, 15
Write recovery time in same logical rank	tWR_slr	30						ns	15
Read to Read command delay in different logical ranks	tCCD_dlr	Max(8nCK, 3.214ns)	-	Max(8nCK, 3.214ns)	-	Max(8nCK, 3.125ns)	-	nCK,ns	
Write to Write command delay in different logical ranks	tCCD_ WR_dlr	Max(8nCK, 3.214ns)	-	Max(8nCK, 3.214ns)	-	Max(8nCK, 3.125ns)	-	nCK,ns	12
Read to Write command delay in different logical ranks	tCCD_RTW_dlr	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3, 5, 6
Write to Read command delay in different logical ranks	tCCD_WTR_dlr	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4, 6
Activate to Activate command delay to different logical ranks	tRRD_dlr	Max(4nCK, 1.666ns)	-	Max(4nCK, 1.666ns)	-	Max(4nCK, 1.666ns)	-	nCK,ns	
Four activate window to different logical ranks	tFAW_dlr	Max(16nCK, 6.666ns)	-	Max(16nCK, 6.666ns)	-	Max(16nCK, 6.666ns)	-	nCK,ns	
Precharge to Precharge delay in different logical rank	tPPD_dlr	2						nCK	7, 15
Activate window by DIMM channel	tDCAW	128						nCK	10, 11, 13, 14, 15
DIMM Channel Activate Command Count in tDCAW	nDCAC	32						ACT	10, 11, 13, 14, 16

13.3.10 Timing Parameters for 3DS-DDR5-6800 to 3DS-DDR5-7600 x4 2H and 4H

Analog timing parameters defined in this section are to be rounded to 1 ps of accuracy. Parameter min values which scale with tCKmin are to be defined using the tCKmin in the associated data rate

Table 343 — Timing Parameters for x4 2H and 4H 3DS-DDR5-6800 to 3DS-DDR5-7600

Speed		DDR5-6800		DDR5-7200		DDR5-7600		Units	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock Timing									
Average Clock Period	tCK(avg)	0.294	-	0.277	-	0.263	-	ns	1
Command and Address Timing for 3DS									
Read to Read command delay for same bank group in same logical rank	tCCD_L_slr	Max(RBL/2, 5ns)						nCK,ns	15
Write to Write command delay for same bank group in same logical rank	tCCD_L_ WR_slr	Max(32nCK, 20ns)						nCK,ns	15
Write to Write command delay for same bank group in same logical rank, second write not RMW	tCCD_L_ WR2_slr	Max(16nCK, 10ns)						nCK,ns	15
Read to Write command delay for same bank group in same logical rank	tCCD_L_ RTW_slr	CL — CWL + RBL/2 + 2tCK — (Read DQS Offset) + (tRPST—0.5tCK) + tWPRE						nCK,ns	3, 5, 6, 15
Write to Read command delay for same bank group in same logical rank	tCCD_L_ WTR_slr	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4, 6, 15
Read to Read command delay for different bank in same bank group	tCCD_M_slr	Max(8nCK, 4.705ns)	-	Max(8nCK, 4.444ns)	-	Max(8nCK, 4.210ns)	-	nCK,ns	
Write to Write command delay for different bank in same bank group	tCCD_M_WR_slr	Max(32nCK, 18.823ns)	-	Max(32nCK, 17.777ns)	-	Max(32nCK, 16.842ns)	-	nCK,ns	
Write to Read command delay for different bank in same bank group	tCCD_M_WTR_slr	CWL+WBL/2 +Max(16nCK, 9.411ns)	-	CWL+WBL/2 +Max(16nCK,8. 888ns)	-	CWL+WBL/2 +Max(16nCK, 8.421ns)	-	nCK,ns	4, 6
Read to Read command delay for different bank group in same logical rank	tCCD_S_slr	RBL/2						nCK	15
Write to Write command delay for different bank group in same logical rank	tCCD_S_ WR_slr	WBL/2						nCK	15
Read to Write command delay for different bank group in same logical rank	tCCD_S_RTW_slr	CL — CWL + RBL/2 + 2tCK — (Read DQS Offset) + (tRPST—0.5tCK) + tWPRE						nCK,ns	3, 5, 6, 15
Write to Read command delay for different bank group in same logical rank	tCCD_S_WTR_slr	CWL+WBL/2 +Max(4nCK, 2.352ns)	-	CWL+WBL/2 +Max(4nCK, 2.222ns)	-	CWL+WBL/2 +Max(4nCK, 2.105ns)	-	nCK,ns	4, 6
Write to Read with Auto Precharge command for same bank in same logic rank	tCCD_WTRA_slr	CWL + WBL/2 + tWR_slr — tRTP_slr						nCK,ns	2, 4, 6, 15
Activate to Activate command delay to same bank group in the same logical rank	tRRD_L_slr(1K)	Max(8nCK, 4.705ns)	-	Max(8nCK, 4.444ns)	-	Max(8nCK, 4.210ns)	-	nCK,ns	
Activate to Activate command delay to different bank group in the same logical rank	tRRD_S_slr(1K)	8						nCK	15
Four activate window to the same logical rank	tFAW_slr(1K)	Max(32nCK, 9.411ns)	-	Max(32nCK, 8.888ns)	-	Max(32nCK, 8.421ns)	-	nCK, ns	9
Read command to Precharge command delay in same logical rank	tRTP_slr	Max(12nCK,7.5ns)						nCK,ns	15
Precharge to Precharge delay in same logical rank	tPPD_slr	2				4		nCK	7, 15
Write recovery time in same logical rank	tWR_slr	30						ns	15
Read to Read command delay in different logical ranks	tCCD_dlr	Max(8nCK, 3.125ns)	-	Max(8nCK, 3.0560ns)	-	Max(8nCK, 3.056ns)	-	nCK,ns	
Write to Write command delay in different logical ranks	tCCD_ WR_dlr	Max(8nCK, 3.125ns)	-	Max(8nCK, 3.0560ns)	-	Max(8nCK, 3.056ns)	-	nCK,ns	12
Read to Write command delay in different logical ranks	tCCD_RTW_dlr	CL — CWL + RBL/2 + 2tCK — (Read DQS Offset) + (tRPST—0.5tCK) + tWPRE						nCK,ns	3, 5, 6, 15
Write to Read command delay in different logical ranks	tCCD_WTR_dlr	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4, 6, 15
Activate to Activate command delay to different logical ranks	tRRD_dlr	Max(4nCK, 1.666ns)						nCK,ns	15
Four activate window to different logical ranks	tFAW_dlr	Max(16nCK, 6.666ns)						nCK,ns	15
Precharge to Precharge delay in different logical rank	tPPD_dlr	2				4		nCK	7, 15
Activate window by DIMM channel	tDCAW	128						nCK	10, 11, 13, 14, 15
DIMM Channel Activate Command Count in tDCAW	nDCAC	32						ACT	10, 11, 13, 14, 15, 16

13.3.11 Timing Parameters for 3DS-DDR5-8000 to 3DS-DDR5-8800 x4 2H and 4H

Analog timing parameters defined in this section are to be rounded to 1 ps of accuracy. Parameter min values which scale with tCKmin are to be defined using the tCKmin in the associated data rate.

Table 344 — Timing Parameters for x4 2H and 4H 3DS-DDR5-8000 to 3DS-DDR5-8800

Speed		DDR5-8000		DDR5-8400		DDR5-8800		Units	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock Timing									
Average Clock Period	tCK(avg)	0.250	-	0.238	-	0.227	-	ns	1
Command and Address Timing for 3DS									
Read to Read command delay for same bank group in same logical rank	tCCD_L_slr	Max(RBL/2, 5ns)						nCK,ns	15
Write to Write command delay for same bank group in same logical rank	tCCD_L_ WR_slr	Max(32nCK, 20ns)						nCK,ns	15
Write to Write command delay for same bank group in same logical rank, second write not RMW	tCCD_L_ WR2_slr	Max(16nCK, 10ns)						nCK,ns	15
Read to Write command delay for same bank group in same logical rank	tCCD_L_ RTW_slr	CL — CWL + RBL/2 + 2tCK — (Read DQS Offset) + (tRPST—0.5tCK) + tWPRE						nCK,ns	3, 5, 6, 15
Write to Read command delay for same bank group in same logical rank	tCCD_L_ WTR_slr	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4, 6, 15
Read to Read command delay for different bank in same bank group	tCCD_M_slr	Max(8nCK, 4.000ns)	-	Max(8nCK, 4.000ns)	-	Max(8nCK, 3.863ns)	-	nCK,ns	
Write to Write command delay for different bank in same bank group	tCCD_M_WR_slr	Max(32nCK, 16.000ns)	-	Max(32nCK, 15.238ns)	-	Max(32nCK, 14.545ns)	-	nCK,ns	
Write to Read command delay for different bank in same bank group	tCCD_M_WTR_slr	CWL+WBL/2 +Max(16nCK, 8.000ns)	-	CWL+WBL/2 +Max(16nCK,7 .619ns)	-	CWL+WBL/2 +Max(16nCK, 7.272ns)	-	nCK,ns	4, 6
Read to Read command delay for different bank group in same logical rank	tCCD_S_slr	RBL/2						nCK	15
Write to Write command delay for different bank group in same logical rank	tCCD_S_ WR_slr	WBL/2						nCK	15
Read to Write command delay for different bank group in same logical rank	tCCD_S_RTW_slr	CL — CWL + RBL/2 + 2tCK — (Read DQS Offset) + (tRPST—0.5tCK) + tWPRE						nCK,ns	3, 5, 6, 15
Write to Read command delay for different bank group in same logical rank	tCCD_S_WTR_slr	CWL+WBL/2 +Max(4nCK, 2.000ns)	-	CWL+WBL/2 +Max(4nCK, 1.904ns)	-	CWL+WBL/2 +Max(4nCK, 1.818ns)	-	nCK,ns	4, 6
Write to Read with Auto Precharge command for same bank in same logic rank	tCCD_WTRA_slr	CWL + WBL/2 + tWR_slr — tRTP_slr						nCK,ns	2, 4, 6, 15
Activate to Activate command delay to same bank group in the same logical rank	tRRD_L_slr(1K)	Max(8nCK, 4.000ns)	-	Max(8nCK, 4.000ns)	-	Max(8nCK, 3.863ns)	-	nCK,ns	
Activate to Activate command delay to different bank group in the same logical rank	tRRD_S_slr(1K)	8						nCK	15
Four activate window to the same logical rank	tFAW_slr(1K)	Max(32nCK, 8.000ns)	-	Max(32nCK, 7.619ns)	-	Max(32nCK, 7.272ns)	-	nCK, ns	9
Read command to Precharge command delay in same logical rank	tRTP_slr	Max(12nCK,7.5ns)						nCK,ns	15
Precharge to Precharge delay in same logical rank	tPPD_slr	4						nCK	7, 15
Write recovery time in same logical rank	tWR_slr	30						ns	15
Read to Read command delay in different logical ranks	tCCD_dlr	Max(8nCK, 3.000ns)	-	Max(8nCK, 3.0000ns)	-	Max(8nCK, 2.955ns)	-	nCK,ns	
Write to Write command delay in different logical ranks	tCCD_ WR_dlr	Max(8nCK, 3.000ns)	-	Max(8nCK, 3.000ns)	-	Max(8nCK, 2.955ns)	-	nCK,ns	12
Read to Write command delay in different logical ranks	tCCD_RTW_dlr	CL — CWL + RBL/2 + 2tCK — (Read DQS Offset) + (tRPST—0.5tCK) + tWPRE						nCK,ns	3, 5, 6, 15
Write to Read command delay in different logical ranks	tCCD_WTR_dlr	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4, 6, 15
Activate to Activate command delay to different logical ranks	tRRD_dlr	Max(4nCK, 1.666ns)						nCK,ns	15
Four activate window to different logical ranks	tFAW_dlr	Max(16nCK, 6.666ns)						nCK,ns	15
Precharge to Precharge delay in different logical rank	tPPD_dlr	4						nCK	7, 15
Activate window by DIMM channel	tDCAW	128						nCK	10, 11, 13, 14, 15
DIMM Channel Activate Command Count in tDCAW	nDCAC	32						ACT	10, 11, 13, 14, 15, 16

13.3.12 Timing Parameters for 3DS-DDR5-9200 x4 2H and 4H

Analog timing parameters defined in this section are to be rounded to 1 ps of accuracy. Parameter min values which scale with tCKmin are to be defined using the tCKmin in the associated data rate.

Table 345 — Timing Parameters for x4 2H and 4H -3DS-DDR5-9200

Speed		DDR5-8000		Units	Notes
Parameter	Symbol	Min	Max		
Clock Timing					
Average Clock Period	tCK(avg)	0.217	-	ns	1
Command and Address Timing for 3DS					
Read to Read command delay for same bank group in same logical rank	tCCD_L_slr	Max(RBL/2, 5ns)		nCK,ns	15
Write to Write command delay for same bank group in same logical rank	tCCD_L_ WR_slr	Max(32nCK, 20ns)		nCK,ns	15
Write to Write command delay for same bank group in same logical rank, second write not RMW	tCCD_L_ WR2_slr	Max(16nCK, 10ns)		nCK,ns	15
Read to Write command delay for same bank group in same logical rank	tCCD_L_ RTW_slr	CL — CWL + RBL/2 + 2tCK — (Read DQS Offset) + (tRPST—0.5tCK) + tWPRE		nCK,ns	3, 5, 6, 15
Write to Read command delay for same bank group in same logical rank	tCCD_L_ WTR_slr	CWL + WBL/2 + Max(16nCK,10ns)		nCK,ns	4, 6, 15
Read to Read command delay for different bank in same bank group	tCCD_M_slr	max(8nCK, 3.863ns)	-	nCK,ns	
Write to Write command delay for different bank in same bank group	tCCD_M_WR_slr	max(32nCK, 14.782ns)	-	nCK,ns	
Write to Read command delay for different bank in same bank group	tCCD_M_WTR_slr	CWL+WBL/ 2+Max(16nCK,6.956ns)	-	nCK,ns	4, 6
Read to Read command delay for different bank group in same logical rank	tCCD_S_slr	RBL/2		nCK	15
Write to Write command delay for different bank group in same logical rank	tCCD_S_ WR_slr	WBL/2		nCK	15
Read to Write command delay for different bank group in same logical rank	tCCD_S_RTW_slr	CL — CWL + RBL/2 + 2tCK — (Read DQS Offset) + (tRPST—0.5tCK) + tWPRE		nCK,ns	3, 5, 6, 15
Write to Read command delay for different bank group in same logical rank	tCCD_S_WTR_slr	CWL+WBL/ 2+Max(4nCK, 1.739ns)	-	nCK,ns	4, 6
Write to Read with Auto Precharge command for same bank in same logic rank	tCCD_WTRA_slr	CWL + WBL/2 + tWR_slr — tRTP_slr		nCK,ns	2, 4, 6, 15
Activate to Activate command delay to same bank group in the same logical rank	tRRD_L_slr(1K)	max(8nCK, 3.695ns)	-	nCK,ns	
Activate to Activate command delay to different bank group in the same logical rank	tRRD_S_slr(1K)	8		nCK	15
Four activate window to the same logical rank	tFAW_slr(1K)	Max(32nCK, 6.956ns)	-	nCK, ns	9
Read command to Precharge command delay in same logical rank	tRTP_slr	Max(12nCK,7.5ns)		nCK,ns	15
Precharge to Precharge delay in same logical rank	tPPD_slr	4		nCK	7, 15
Write recovery time in same logical rank	tWR_slr	30		ns	15
Read to Read command delay in different logical ranks	tCCD_dlr	Max(8nCK, 2.955ns)	-	nCK,ns	
Write to Write command delay in different logical ranks	tCCD_ WR_dlr	Max(8nCK, 2.955ns)	-	nCK,ns	12
Read to Write command delay in different logical ranks	tCCD_RTW_dlr	CL — CWL + RBL/2 + 2tCK — (Read DQS Offset) + (tRPST—0.5tCK) + tWPRE		nCK,ns	3, 5, 6, 15
Write to Read command delay in different logical ranks	tCCD_WTR_dlr	CWL + WBL/2 + Max(4nCK,2.5ns)		nCK,ns	4, 6, 15
Activate to Activate command delay to different logical ranks	tRRD_dlr	Max(4nCK, 1.666ns)		nCK,ns	15
Four activate window to different logical ranks	tFAW_dlr	Max(16nCK, 6.666ns)		nCK,ns	15
Precharge to Precharge delay in different logical rank	tPPD_dlr	4		nCK	7, 15
Activate window by DIMM channel	tDCAW	128		nCK	10, 11, 13, 14, 15
DIMM Channel Activate Command Count in tDCAW	nDCAC	32		ACT	10, 11, 13, 14, 15, 16

Timing Parameters Table Notes for 3DS-DDR5-3200 to 3DS-DDR5-9200 x4 2H and 4H:

1. tCK(avg)min listed for reference only, refer to the Speed Bins and Operations section which lists all valid tCK(avg) values.
2. tCCD_WTRA_slr(min) shall always be greater than or equal to CWL + WBL/2 + tWR_slr(min) - tRTP_slr(min), and when using the appropriate rounding algorithms, nCCD_WTRA_slr(min) shall always be greater than or equal to CWL + WBL/2 + nWR_slr(min) - nRTP_slr(min).
3. RBL: Read burst length associated with Read command

   RBL = 32 for fixed BL32 and BL32 in BL32 OTF mode

   RBL = 16 for fixed BL16 and BL16 in BL32 OTF mode

   RBL = 16 for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
4. WBL: Write burst length associated with Write command

   WBL = 32 for fixed BL32 and BL32 in BL32 OTF mode

   WBL = 16 for fixed BL16 and BL16 in BL32 OTF mode

   WBL = 16 for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
5. The following is considered for tRTW equation

   1tCK needs to be added due to tDQS2CK

   Read DQS offset timing can pull in the tRTW timing

   1tCK needs to be added when 1.5tCK postamble
6. CWL=CL-2
7. tPPD applies to any combination of precharge commands (PREab, PREsb, PREpb). tPPD also applies to any combination of precharge commands to a different die in a 3DS DDR5 SDRAM.
8. These timings contained in this table are for x4 2H and 4H 3Ds device
9. For x4 devices only.
10. Activate commands to different channels on the same DIMM may be issued on the same cycle, not requiring any stagger.
11. Activate commands to the same channel on a DIMM are subject to tDCAW. No more than nDCAC activate commands may be issued to the same channel on a DIMM within tDCAW.
12. tCCD_ WR_dlr and tCCD_ WR_dpr also apply to the WRITE PATTERN command.
13. Parameter applies to all DDP, or dual-physical-rank (36 and 40 placement) 3DS-based DIMMs built with JEDEC PMICXXXX, but may not apply to DIMMs built with higher current capacity PMICs.
14. Activate commands to a DIMM channel include all Activate commands to the same logical rank (SLR), all Activate commands to different logical ranks (DLR), and all Activate commands to different physical ranks (DPR).
15. This parameter only specifies minimum values (there is no maximum value). The maximum value cells have been merged in the table to improve legibility.
16. This parameter only specifies maximum values (there is no minimum value). The minimum value cells have been merged in the table to improve legibility.

14 DDR5 Module Rank and Channel Timings

14.1 Module Rank and Channel Limitations for DDR5 DIMMs

To achieve efficient module power supply design for JEDEC-standard DDR5 DIMMs, minimum timings as well as limitations in the number of DRAMs are provided for Refresh, and Write operations occurring on a single module. As well, since these modules are organized as two independent 36-bit or 40-bit channels (32 bits for non-ECC DIMMs), additional restrictions apply in order to limit localized power delivery noise on the module. To provide best performance, the different channels may initiate commands on the same cycle provided the rank to rank timings are met, the maximum number of DRAMs in a given activity is not exceeded, and the applicable component timings shown elsewhere in this specification are met. The timing and operational relationships for DDR5 DIMMs are shown in Table 346.

Table 346 — DDR5 Module Rank and Channel Timings for DDR5 DIMMs

DIMM Configuration	Maximum Number of DRAM Die in Simultaneous or Overlapping Activity			
	Refresh (All-Bank Refresh)		Write, Write-Pattern	
	Die per Physical Rank	Die per DIMM	Die per Channel	Die per DIMM
SR x16	No restriction			
DR x16	No restriction		2	4
SR x8	No restriction			
DR x8	No restriction		5	10
SR x4	No restriction			
DR x4	No restriction		10	20
DR x4 (2H 3DS)	No restriction	40	10	20
DR x4 (4H 3DS)	30	40	10	20
DR x4 (8H 3DS)	30	40	10	20
Notes	1, 2, 3, 4, 7, 8, 9		1, 5, 6, 7, 9	

NOTE 1 Any combination of commands with up to the maximum of die per channel and per DIMM, per condition is allowed.

NOTE 2 Refresh commands to different channels do not require stagger.

NOTE 3 tRFC_dlr must be met for refresh commands to different logical ranks within a package rank on the same channel.

NOTE 4 Any DRAM is considered to be in Refresh mode until tRFC time has been met.

NOTE 5 tCCD parameters must be met for Write and Write-Pattern commands to different logical ranks or physical ranks within the same channel. No overlapping write data bus activity is allowed on physical or logical ranks within the same channel. Write Preamble and Postamble DQS parameters (timings and amplitudes, waveforms) for each receiving device need satisfied as well.

NOTE 6 Write and Write-Pattern commands to different channels do not require stagger.

NOTE 7 Each rank consists of one group of DRAMs making up a 36 or 40 bit channel (32 bits for non-ECC DIMMs).

NOTE 8 These restrictions only apply to explicit all-banks refresh commands (REFab) and not to self-refresh entry or exit

NOTE 9 Restrictions apply to DIMMs built with JEDEC PMICXXXX, but may not apply to DIMMs built with higher current capacity PMICs

15 DDR5 System RAS Improvement

15.1 Design Guidelines for DDR5 Bounded Fault RAS Improvement

15.1.1 DDR5 Reliability Design Guidelines Overview

These DDR5 reliability design guidelines aim to bound bits impacted by certain DRAM failures. This limits the number of failure patterns seen by the memory controller such that correction of many failures can be reliably performed in DIMMs with one ECC device.

Many internal DRAM failures may impact only a portion of the data from a fetch. The likelihood of a specific component failing may also vary between process generations and DRAM vendors. These guidelines can be used by DDR5 DRAM's to bound failures from the components most likely to fail. These design guidelines can only address failures that impact a portion of the data from a 128-bit fetch. Failures that impact all the data in a 128-bit fetch from a device (e.g., device failure, bank failure) cannot be bounded as described here.

15.1.2 Reliability Design Guidelines

In a x8 device bounded failures are defined by the following qualities:

- A bounded fault will not impact more than 32 bits of data in a 128-bit fetch
- The data bits impacted by a bounded failure will be confined to at most 2 DQs (i.e. the failures will be DQ aligned)
- The DQs transmitting data impacted by the failure will both be in either the first nibble or the second nibble of a burst. That is, the impacted DQs will both be in the set of the first 4 DQs (DQ0, DQ1, DQ2, DQ3) or both in the set of the last four DQs (DQ4, DQ5, DQ6, DQ7)

Figure 257 shows examples of fault boundaries for x8 devices. Device on the left has a bounded fault in lanes DQ0 and DQ1 in the first nibble. Device on the right has a bounded fault in lanes DQ4 and DQ6 in the second nibble.

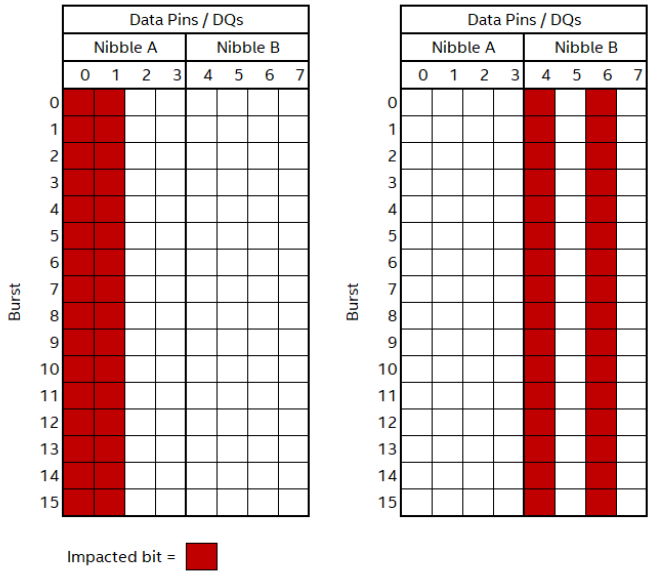


Figure 257 — Examples of x8 Fault Boundaries

An x4 device has similarly defined qualities for the failure boundaries, with the noted exception of the number of bits impacted by a bounded failure. In a DRAM device in a 9x4 configuration bounded failures should not impact more than 16 bits. However, in a 10x4 device, the bounded failure may impact up to 32 bits.

15.1.2 Reliability Design Guidelines (cont'd)

In x4 devices bounded failures are defined by the following qualities:

- A bounded failure in a DRAM device in a 9x4 configuration shall not impact more than 16 bits of data in a 128-bit prefetch.
- A bounded failure in a DRAM device in a 10x4 configuration shall not impact more than 32 bits of data in a 128-bit prefetch.
- For a device in a 9x4 configuration, the data bits impacted by a bounded failure will be confined to one DQ.
- For a device in a 10x4 configuration, the data bits impacted by a bounded failure will be confined to at most two DQs.

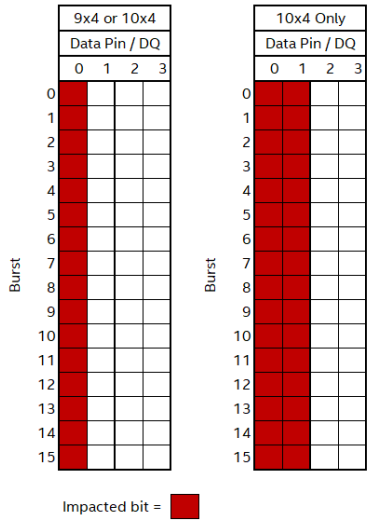


Figure 258 — Example of x4 Fault Boundary

15.2 Single Error Correction (SEC) Code Properties

To maintain the bounded fault design guidelines, miscorrections by the on-die ECC must be restricted when a bounded fault causes a multi-bit error. In devices with bounded fault it is suggested that the DRAM vendor uses an on-die ECC code that maintains the fault boundaries. That is, if an error is contained in one boundary, then the on-die ECC should not spread the error into a second boundary by miscorrection. Note that if faults are not bounded in the device, then the on-die ECC does not need to have these properties.

To restrict miscorrection in devices following bounded fault design guidelines, the data may be divided into blocks aligned with the bounded fault and miscorrection should be restricted in the case an error is contained in a single data block. The 128 data bits used to compute a set of 8 check bits may be divided into data blocks up to 32 bits in size. These data blocks are to be determined by the memory vendor to best align with internal DRAM faults. For example, a common component fault may impact 32 bits per 128 data bits, then the vendor may choose to divide the 128 data bits into four 32-bit blocks each of which correspond to the bits impacted by one of the components failing.

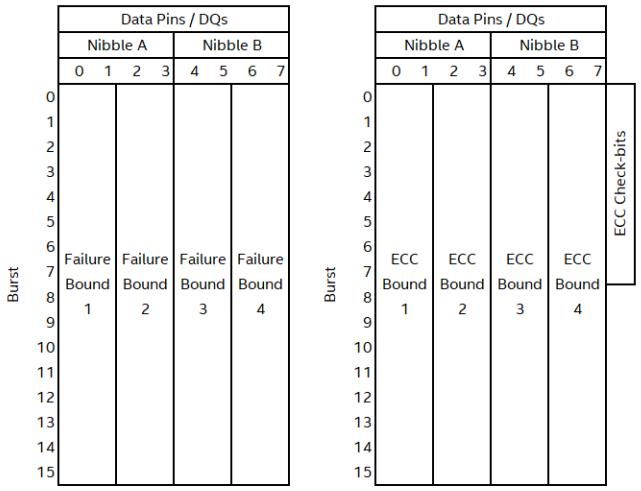


Figure 259 — Example of Fault Boundaries versus On-die ECC Data Blocks

If a multi-bit error occurs on a read and is limited to one data block, then the on-die ECC SEC code should do one of the following:

- Miscorrect a bit in the data block containing the error
- Miscorrect a bit in the on-die ECC check bits
- Detect the error (a SEC code may detect some multi-bit errors, but detection of these errors is not guaranteed)

The selection of block size and data blocks is determined by the vendor to best suit the device architecture and possible modes of fault.

15.3 Writeback of Data During ECS and x4 RMW Operations

The DRAM device may optionally support the suppressing of the writeback for ECS operations and x4 RMW Read-Modify-Write (RMW) operations. DRAM may implement the feature in MR9 or MR15. DDR5 SPD Byte 14 Bits[2:1] indicates if feature is supported and will also indicate whether to use MR9 or MR15 for enabling the modes.

If MR9 OP1=1 or MR15 OP7=1, then x4 DRAM's on writes will perform an internal 'read-modify-write' operation for BL16. BL32 mode does not requires an internal 'read modify write' operation. The DRAM will correct any single bit errors that result from the internal read of 128 bit data before merging the incoming 64 bit data and then re-compute 8 ECC Check bits. Note that ECC check bits are computed after merging of the incoming data with the corrected data from the array. DRAM will then write the incoming 64b data to the array along with recomputed 8 ECC Check bits. DRAM will suppress the writeback of 64 bit data that was fetched from the array irrespective of whether the 64 bit data needed any correction or not. Suppression of writeback (where applicable due to BC8 or DM usage) is not supported on x8/x16 devices; MR9:OP[1] or MR15:OP[7] must be set to "0_B". Suppression of writeback may or may not occur when BC8 mode is used on x4 devices.

If MR9 OP0=1 or MR15 OP6=1, then DRAM will suppress writeback of data and ECC Check bits during ECS operation for x4, x8, and x16 DDR5. DRAM will continue to count errors to provide transparency.

Table 347 — MR9 or MR15 Register Information

Function	Register Type	Operand	Data	Notes
x4 Writes	R/W	MR9:OP[1] or MR15:OP[7]	0B: Do not suppress writeback of Data during RMW (Default) 1B: Suppress writeback of Data during RMW (Optional)	1
ECS Write-back	R/W	MR9:OP[0] or MR15:OP[6]	0B: Do not suppress writeback of Data and ECC Check Bits (Default) 1B: Suppress writeback of Data and ECC Check Bits (Optional)	1
NOTE 1 DDR5 SPD Byte 14 Bits[2:1] indicates if feature is supported and will also indicate whether to use MR9 or MR15 for enabling the modes.				

DDR5 SPD Byte 14 Definition (Referenced from JESD400-5)

Byte 14 (0x00E): SDRAM Fault Handling and Temperature Sense

This byte defines support for SDRAM fault handling features and for wide on-die temperature sensing range (see MR4). This value comes from the DDR5 SDRAM specification, JESD79-5.

Table 348 — SDRAM Fault Handling and Temperature Sense

SDRAM Fault Handling Features and Temperature Sense			
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**
Reserved; must be coded as 0000			
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**
Wide Temperature Sense	**x4 RMW/ECS Writeback Suppression**	**x4 RMW/ECS Writeback Suppression MR Selector**	**Bounded Fault**
0: Wide temperature sense and reporting not supported 1: Wide temperature sense and reporting supported	0: Writeback suppression not supported 1: Writeback suppression supported	0: Writeback suppression control in MR9 1: Writeback suppression control in MR15	0: Bounded Fault not supported 1: Bounded Fault supported
NOTES: ECS = Error Check and Scrub RMW = Read-Modify-Write MR = Mode Register			

16 DDR5 Per Row Activation Counting

16.1 Introduction

Deterministic counting of row activations is an optional feature on DDR5 16Gb and higher density devices, with support indicated by MR70:OP[0]. This feature detects row activity that may adversely affect the data stored in cells on physically adjacent rows within the DRAM. As one or more rows' activation counts approach or reach a maximum activation threshold after a Refresh (REF) or Refresh Management (RFM) command, the host and DRAM may need to take action to prevent data in affected cells from flipping states.

The intended implementation for Per Row Activation Counting (PRAC) is to add Activation Counter bits to every row in the DRAM. These bits store a count associated with the number of activations received by a row since the last time it was refreshed. Activations to a row include the ACT, REF, and RFM commands, and the MPC Manual ECS function.

A DDR5 design that supports PRAC shall continue to support "legacy" methods for maintaining data integrity in DRAM cells for backward compatibility. Designs supporting PRAC shall continue to support all features and functions as defined in this specification when running with PRAC disabled.

When PRAC is enabled, (MR70:OP[1]=1_B), the following modes are disabled by the DRAM, with MR58 and MR59 retaining their access types and values and those MRs will reflect the values of any subsequent MRWs:

- RFM Required, as indicated by MR58:OP[0], is disabled internally by the DRAM and not required by the host regardless of value set in the MR
- DRFM Enable, as configured by MR59:OP[0], is disabled internally by the DRAM regardless of host write value

Functionality of the PRAC RFM command is enabled when MR70:OP[1]=1_B and replaces the command usage described in Clause 4.42 Refresh Management (RFM). If Refresh Management is not required, MR58:OP[0]=0_B, and PRAC is disabled, MR70:OP[1]=0B, CA9 is only required to be valid ("V") for a REF command, and the DRAM will treat a RFM command as a REF command. If Refresh Management is required, MR58:OP[0]=1_B, or PRAC is enabled, MR70:OP[1]=1B, a REF command requires CA9=H.

DRFM functionality of the WRPA, WRA, RDA, PREpb and DRFM commands is disabled regardless of MR59:OP[0] host write value when MR70:OP[1]=1_B. The DRFM address sampling operation is disabled for the WRPA, WRA, RDA, and PREpb commands. CA9 is only required to be valid ("V") for WRPA, WRA, and RDA commands. When CID3 is not used, CA5 is required to be Valid ("V") for RFM and PREpb commands.

The requirements for enabling and using PRAC are described in Sections 16.2-16.9. Updates to usage of the PRAC RFM command are described in Clauses 16.4 and 16.5.

On-the-fly switching between modes is not permitted. Enabling PRAC requires initialization, as described below. Disabling PRAC (re-enabling legacy) requires a DRAM Reset.

When PRAC is supported (MR70:OP[0]=1_B) but disabled (MR70:OP[1]=0_B), all associated Mode Registers can be written to and read from, however no PRAC-related behaviors will be executed until PRAC is enabled (MR70:OP[1]=1_B). Activation Counter Initialization, PRAC Testing, and Alert Verification shall be disabled prior to enabling PRAC.

16.2 Activation Counter Initialization

Upon power-up or any time that DRAM refresh requirements are violated, the Activation Counter bits may be in an unknown state, requiring an initialization to put the bits into a known state.

The default state for DDR5 Per Row Activation Counting (PRAC) is disabled (MR70:OP[1]=0_B), as this is an optional feature. Prior to initialization of the activation counter bits, the PRAC shall be enabled (MR70:OP[1]=1_B) by the host. Once the PRAC is enabled, a full array Activation Counter Initialization (ACI) shall be performed. The DRAM will not track activation counts, nor issue an Alert Back-Off (ABO), until the Activation Counter bits are initialized. Legacy mode for maintaining of data integrity will not be performed after PRAC is enabled.

To initialize the Activation Counter bits, the host sets MR70:OP[2]=1_B to indicate to the DRAM that a full array refresh will take place. Only REF , MRR, MRW w/ CW=1, NOP and NT_ODT commands are permitted during initialization. The REF commands during the initialization period may be issued by the host up to two times (2x) the normal refresh rate (Normal mode: 0.5*tREFI1; FGR mode: 0.5*tREFI2). Upon completion of a full refresh cycle, the DRAM shall indicate completion of the ACI by setting MR70:OP[3]=1_B, which the host shall then follow by setting MR70:OP[2]=0_B. The DRAM shall start counting activations from that point forward and issue the ABO as necessary.

For 3DS devices, the host shall confirm the base die ACI has been completed via MR70:OP[3]=1B, prior to changing the CID bits via MR14 to confirm completion of the ACI in the remaining die in the stack. During ACI, only the MRW to MR14 to change the CID bits is allowed, and those MRWs are only allowed once the base die ACI has completed. Once ACI complete has been confirmed in all die of the stack, the host shall then follow by setting MR70:OP[2]=0B. The DRAM shall start counting activations from that point forward and issue the ABO as necessary.

During ACI, the DRAM does not need to refresh the main array, and any data previously written may be corrupted.

If the host reenters Activation Counter Initialization by setting MR70:OP[2]=1_B, the DRAM will reset MR70:OP[3]=0_B until the initialization has been completed. Likewise, a system reset to disable PRAC (MR70:OP[1]=0_B) will also reset MR70:OP[3]=0_B.

Like normal DRAM cells, the Activation Counter bits require refresh to maintain the stored values. Any time refresh is violated during ACI or after ACI in modes like MPSM or other idle periods, the ACI shall be performed by the host to set the Activation Counter bits to a known state. Since array data is also corrupted by refresh violations, previous Activation Counter values become irrelevant.

During hPPR and MBIST/mPPR, the system does not maintain refresh to the DRAM. Therefore, the host shall perform a full array ACI before rewriting data following the hPPR and MBIST/mPPR operations.

During sPPR, the system is required to maintain refresh to DRAM. However, before the sPPR operation, the DRAM is not required to maintain data integrity (refresh) for the row element designated to be used for the repair. tPGM_Exit timing extension from tRP to tRP+tRFMsb provides sufficient time to the DRAM to update the Activation Counter value of the new row as well as proactively perform mitigation for neighboring rows of the new row before completion of sPPR operation. Likewise, for sPPR Undo, the DRAM is allowed to update the Activation Counter value of the old row as well as proactively perform mitigation for neighboring rows of the old row before completion of sPPR operation. The extended tPGM_Exit timing is applied to sPPR operation (host MRW to MR23:OP[2:1] = 01, 10) with PRAC enabled (host MRW to MR70:OP[1] = 1).

Table 349 — Per Row Activation Counting (PRAC) sPPR Timing

Parameter	Symbol	Min	Max	Unit	Notes
sPPR Exit Recognition Time	tPGM_Exit	tRP+tRFMsb	-	ns	

16.3 Per Row Activation Counting Core Timing Parameters

Per Row Activation Counting (PRAC) requires additional counter cells per row in the DRAM to store Activation (ACT) command counts. Updating the activation counter cells requires a read-modify-write to the activation counter cells, known as Activation Counter Update (ACU), resulting in a change in some of the core timing parameters, when Per Row Activation Counting is enabled (timings not noted here remain the same as when PRAC is disabled):

Table 350 — Per Row Activation Counting (PRAC) Core Timing Parameters

Parameter	Symbol	Min	Max	Unit	Notes
ACT to PRE	tRAS	16	3 * tREFI1 (Normal), 5 * tREFI2 (FGR)	nS	1
Row Precharge	tRP	36	-	nS	2
ACT to ACT / REF	tRC	52	-	nS	
Write Recovery	tWR	10	-	nS	3
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA	CWL+WBL/ 2+Max(16nCK,10ns)	-	nCK,ns	4
NOTE 1 tRASmax is based on the maximum allowance for postponed REF commands NOTE 2 Clock-based nRP timings are defined in the Speed Bin tables. NOTE 3 Clock-based nRTP and nWR timings are defined in MR6. NOTE 4 Notes from Section 13 Timing Parameters still apply					

Examples of the timings affected by the updating of the activation counter bits are shown in Figure 260 through Figure 262. The “i” references DRAM internal commands, not external commands issued by the Host.

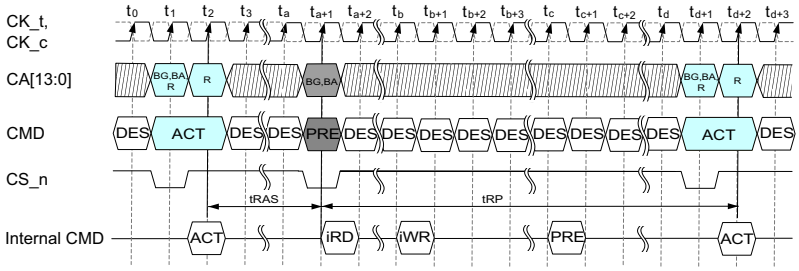


Figure 260 — Example ACT-PRE with ACU

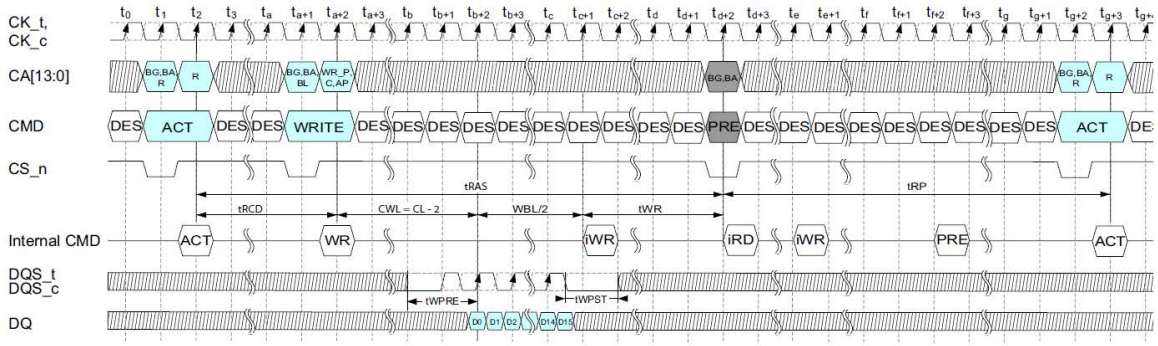


Figure 261 — Example ACT-WR-PRE with ACU

16.3 Per Row Activation Counting Core Timing Parameters (cont'd)

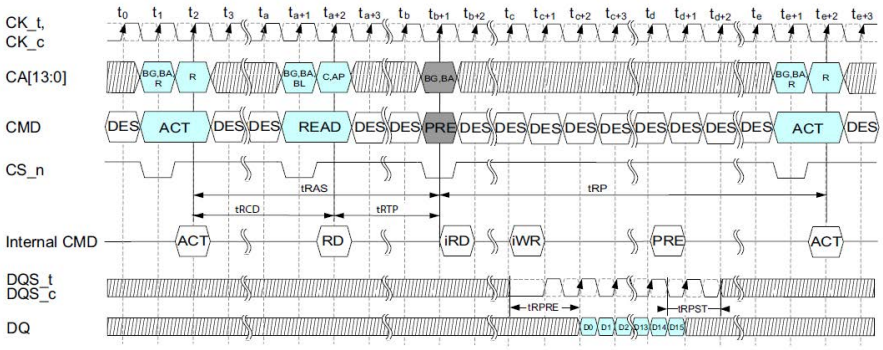


Figure 262 — Example ACT-RD-PRE with ACU

16.3.1 Refresh Operation Scheduling Flexibility

Refresh Operation Scheduling Flexibility is reduced when PRAC is enabled to allow targeted refreshes to occur at an improved rate.

In Normal Refresh mode, a maximum of 2 REFab command can be postponed. In the case that 2 REFab command is postponed, the resulting maximum interval between the surrounding REFab commands is limited to 3 × tREFI1. At any given time, a maximum of 3REFab commands can be issued within 1 x tREFI1 window.

In FGR Mode, the maximum REFab commands that may be postponed is 4, with the resulting maximum interval between the surrounding REFab commands limited to 5 x tREFI2. At any given time, a maximum of 5 REFab commands can be issued within 1 x tREFI2 window.

16.3.2 Precharge Timing

Unlike the traditional Precharge (PRE) command, the PRAC PRE initiates an internal read followed by an internal write to increment the Activation Counting bits for all open rows affected by the PRE command. To allow for adequate power distribution network (PDN) recovery, the Row Precharge time, tRP, shall be scaled by the number of rows being closed.

Table 351 — Per Row Activation Counting (PRAC) Precharge Timing

Parameter	Number of Rows	tRP Required	Notes
Per Bank Precharge (PREpb)	1	tRP,min	
Same Bank Precharge (PREsb)	1 - 8	tRP,min	
All Bank Precharge (PREab)	1 - 8 9 - 32	tRP,min tRP,min + 4 ns	

16.4 Per Row Activation Counting Response

Since the DRAM is counting ACT commands on a per row basis, action may be required upon one or more rows reaching a counter threshold level or levels, or when a queue holding row addresses for targeted refreshing reaches or passes a critical level. This action is a request by the DRAM for the host to pause normal activity for a recovery period where refresh management (RFM commands) or other functions may be performed. This action is a “back-off”. The back-off protocol is described in the next section.

The counter and/or queue threshold level(s) may be changed (reduced) by setting the Adaptive Per Row Activation Counting level in MR71:OP[3:2] to something other than the default MR71:OP[3:2]=00_B. These alternate levels are based on the default starting value. The threshold level(s) reductions are approximately Level A = default - 10%, Level B = default - 20%, and Level C = default - 30%. Changing levels requires an ACI or full array refresh to set/reset all counters to a known state below critical threshold levels and to empty the queue.

In addition to the back-off which is required to keep activation counts from exceeding the threshold level, the DRAM can proactively perform targeted refreshes during Refresh (REF) and/or Refresh Management (RFM) commands to reduce and/or prevent the occurrence of the Alert Back-Off being triggered.

16.4.1 Targeted Refresh

For targeted refreshing during Refresh commands, the DRAM will adjust the normal refreshes accordingly to allow time for the additional row refreshing to occur. The back-off protocol will exist for cases where the DRAM cannot keep up during normal Refresh commands. There is no change to tRFC when PRAC is enabled.

16.4.2 Targeted RFM

DDR5 does not require issuing RFM commands as proactive mitigation when PRAC is enabled.

However, as a guideline for a host that chooses to have the DRAM proactively perform targeted refreshing during Refresh Management commands, the host may track the level of activity that occurs on a per-bank or sub-bank basis. When the Bank Activation Threshold (BAT) is reached (example BAT shown in Table 352), the RFMsb or RFMab command is issued. The duration of the RFM command (tRFM) is sufficient for the Row Refresh Span of +/-1 and +/-2 physically adjacent rows and the target row to be refreshed. This tRFM duration is directly related to the time required to refresh the rows. Due to a single row being refreshed on multiple banks corresponding to the RFMab or RFMsb command being issued, the per row refresh duration is tRRF.

Table 352 — Example Bank Activation Threshold (BAT)

Parameters	Symbol	Value	Units	Notes
Bank Activation Threshold	BAT	75	Activations	1
NOTE 1 The example BAT is derived from tREFI1=3.9 µs / tRC,min=52 ns.				

Table 353 — Per Row Refresh Timing

Parameters	Symbol	Duration	Units	Notes
All bank per row refresh	tRRFab(min)	70	ns	
Same bank per row refresh	tRRFsb(min)	60	ns	

Table 354 — Refresh Management Command Timing

Parameters	Symbol	Duration	Units	Notes
RFM All Bank (RFMab)	tRFMab	(4+1) * tRRFab	ns	
RFM Same Bank (RFMsb)	tRFMsb	(4+1) * tRRFsb	ns	

16.4.2 Targeted RFM (cont'd)

Table 355 — 3DS and DDP Refresh Management Command Timing

Parameters	Symbol	Duration	Units	Notes
RFM All Bank (RFMab) with 3DS same logical rank	tRFMab_slr	tRFMab	ns	1
RFM Same Bank (RFMsb) with 3DS same logical rank	tRFMsb_slr	tRFMsb	ns	1
RFM All Bank (RFMab) with 3DS different logical rank	tRFMab_dlr	tRFMab/3	ns	3,4
RFM Same Bank (RFMsb) with 3DS different logical rank	tRFMsb_dlr	tRFMsb/3	ns	3,5
RFM All Bank (RFMab) with 3DS or DDP different physical rank	tRFMab_dpr	tRFMab/3	ns	2,3,4
RFM Same Bank (RFMsb) with 3DS or DDP different physical rank	tRFMsb_dpr	tRFMsb/3	ns	2,3,5

NOTE 1 All 3D Stacked (3DS) devices follow the same requirements as the monolith die for same logical ranks

NOTE 2 Parameter applies to all DDP, or dual-physical-rank (36 and 40 placement) 3DS-based DIMMs built with JESD301-1 "PMIC 50x0 Specification", but may not apply to DIMMs built with higher current capacity PMICs.

NOTE 3 3DS and DDP tRFM parameters are to be rounded up to the nearest 1 ns after the tRFM/3 calculation

NOTE 4 Parameter applies from RFMab to RFMab or RFMsb

NOTE 5 Parameter applies from RFMsb to RFMsb or RFMab

16.5 Back-off Protocol

DDR5 DRAM devices may support the optional Per Row Activation Counting (PRAC) for monitoring per row activity to ensure all rows are refreshed as needed to maintain data integrity. To facilitate the refresh activity, the DRAM may request the host pause normal activity for a maintenance period where refresh management (RFM commands) or other functions may be performed. This is called a "back-off".

16.5.1 Alert Back-Off Protocol

The DDR5 back-off protocol uses the ALERT_n signal and mode register settings to provide a handshake between the DRAM and the host. This is the Alert Back-Off (ABO).

16.5.1.1 PRAC Triggered Alert Back-off

The Alert Back-off (ABO) protocol is enabled when PRAC is enabled by setting MR70:OP[1]=1_B. Upon reaching critical threshold levels by one or more rows, or when a queue holding addresses for targeted refreshing reaches or passes a critical level, the DRAM asserts ALERT_n and sets the ABO Flag at MR70:OP[5]=1_B, indicating that ALERT_n was asserted due to additional refresh management (RFM) being required. All commands received by the DRAM are executed while ALERT_n is asserted to maintain synchronization between DRAMs in the same rank on a DIMM.

Commands that may trigger the ABO include PREab/PREsb/PREpb, WRPA, WRA, RDA, REFab/REFsb and RFMab/RFMab and the MPC function Manual ECS. ALERT_n will be asserted within tABO_Assert, which occurs between issuing the trigger command and before the max(5ns,10nCK) following the completion of the respective command duration shown in Table 356.

Table 356 — Duration to ALERT_n Assertion / Deassertion

Symbol	Description	Command	Mono Device Max	3DS Device Max
tABO_Assert	Duration to ALERT_n assertion	PREab/PREsb/PREpb	tRP+max(5ns, 10nCK)	tRP+max(7.5ns,15nCK)
		WRPA/WRA	CWL+WBL/ 2+tWR+tRP+max(5ns,10nCK)	CWL+WBL/2 +tWR+tRP+max(7.5ns,15nCK)
		RDA	tRTP+tRP+max(5ns,10nCK)	tRTP+tRP+max(7.5ns,15nCK)
		REFab (Normal)	tRFC1+max(5ns,10nCK)	tRFC1+max(7.5ns,15nCK)
		REFab (FGR)	tRFC2+max(5ns,10nCK)	tRFC2+max(7.5ns,15nCK)
		REFsb	tRFCsb+max(5ns,10nCK)	tRFCsb+max(7.5ns,15nCK)
		RFMab	tRFMab+max(5ns,10nCK)	tRFMab+max(7.5ns,15nCK)
		RFMsb	tRFMsb+max(5ns,10nCK)	tRFMsb+max(7.5ns,15nCK)
		MPC function Manual ECS	tECSc+max(5ns,10nCK)	tECSc+max(7.5ns,15nCK)
	Duration to ALERT_n deassertion	SRX	tXS+max(5ns,10nCK)	tXS+max(7.5ns,15nCK)
		SRE	tCKLCS+max(5ns,10nCK)	tCKLCS+max(7.5ns,15nCK)

16.5.1.1 PRAC Triggered Alert Back-off (cont'd)

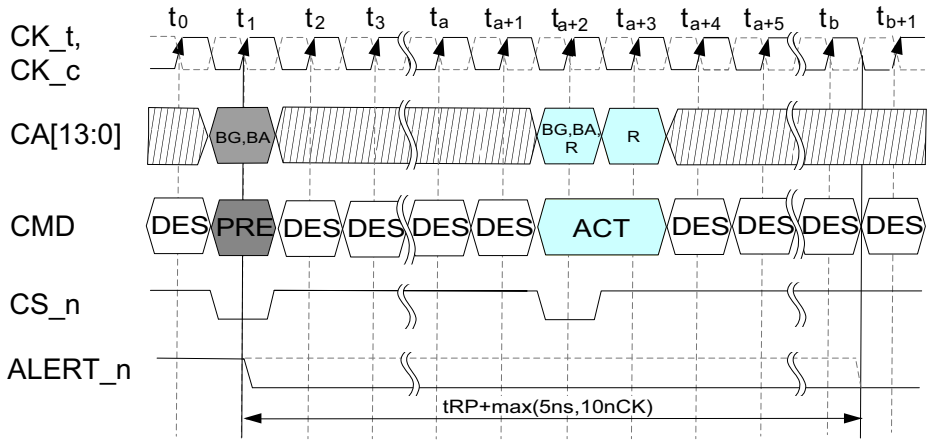


Figure 263 — Example Duration to ALERT_n Assertion for PRE Command

Since the PREpb required during hPPR/sPPR and the PREab during mPPR have different functions than closing a row, no counter bits will be incremented associated with the repaired row, therefore no ABO will be triggered in this instance.

16.5.1.2 Alert Back-off

To instantiate the ABO, ALERT_n is asserted by the DRAM with a fixed duration of clock cycles as defined by tABO_PW.

Table 357 — Alert Back-off Timing Parameters

Symbol	Description	Min	Typ	Max	Unit	Note
tABO_PW	Alert Back-Off pulse width	-	640	-	nCK	
tABO_ACT	Normal traffic to the DRAM allowed	-	-	180	ns	

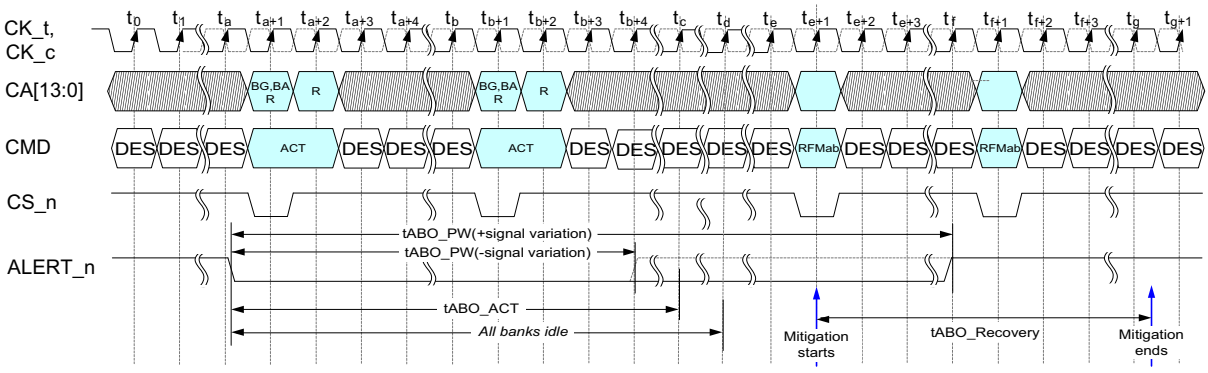


Figure 264 — Alert Back-Off Timing Diagram

After the ALERT_n is asserted, a bounded number of Activate (ACT) commands are permitted before the host starts the RFM-based recovery period. Issuing ACT commands along with normal traffic is allowed within the tABO_ACT window,however no additional ACT commands are allowed at the end of the tABO_ACT window until tABO_Recovery is complete. The host shall complete idling all banks within tREFI/2 after the ALERT_n is asserted, which is followed by the recovery period (tABO_Recovery).

16.5.1.2 Alert Back-off (cont'd)

The recovery period begins when host issues the first RFMab command in response to ALERT_n. The DRAM self-clears the ABO flag by setting MR70:OP[5]=0_B by the end of the tABO_Recovery period, tABO_Recovery ends tRFMab after the last RFMab commandor after tABO_PW, whichever takes longer.

The only RFM commands allowed during the tABO_Recovery period are RFMab. The duration of the RFMab command is described in the previous section (Per Row Activation Counting Response). The number of RFMab commands required to be issued per ABO maintenance period are defined by mode register ABO_RFM bits, MR71:OP[1:0]. Systems that have stricter requirements for isochronous bandwidth may limit the number of RFMab commands by setting MR71:OP[1:0] to a lower value.

If additional RFM commands are needed, the Alert Back-Off protocol is restarted following the Alert Back-Off delay, as described below.

During the ABO_Recovery period, a host may issue only RFMab, REFab/REFsb, PDE, PDX, SRE, PREab/PREsb/PREpb, NOP, MRW (PRAC-related MR changes not allowed during ABO_Recovery) and MRR commands. Refresh commands issued are to ensure that DRAM refresh requirements are not violated. The Refresh commands do not perform any of the refresh management required.

If Power Down is entered after ABO has been asserted but before the ALERT_n pulse has completed, the DRAM continues to assert ALERT_n for the expected tABO_PW duration, however the Host only resumes issuing RFM commands after exiting Power Down.

If Power Down is entered after ABO has been asserted and the tABO_PW duration has completed, the Host is responsible for issuing all of the expected RFM commands as of combination of commands before entering and after exiting Power Down.

Table 358 — PRAC Power Down Timing Parameters

Parameter	Symbol	Min	Max	Unit	Note
Write command to Power-Down Entry command	tWRPDEN	CWL+WBL/ 2+WRLegacy+1	-	nCK	1,3,4
Write w/Auto Precharge command to Power-Down Entry command	tWRAPDEN	CWL+WBL/ 2+WRLegacy+1	-	nCK	1,2,3,4

NOTE 1 Write Recovery (WRLegacy) is calculated from non-PRAC tWR by using the Rounding Algorithm. Refer to the Rounding Definitions and Algorithm section for more information.

NOTE 2 Write Recovery (WRLegacy) in clock cycles as programmed in MR6.

NOTE 3 Write can refer to both Target command and Non-Target command when CA11=H during PDE command.

NOTE 4 WBL: Write burst length associated with Write command.

a) WBL = 32 (36 with WCRC on) for fixed BL32 and BL32 in BL32 OTF mode

b) WBL = 16 (18 with WCRC on) for fixed BL16 and BL16 in BL32 OTF mode

c) WBL = 16 (18 with WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

In Self Refresh, the DRAM de-asserts ALERT_n. Upon exiting Self Refresh, the DRAM will reevaluate and issue a new ALERT_n if ABO is still needed.

16.5.1.3 Alert Back-Off Delays

ABO_Delay defines an interval in which DRAM shall service a minimum number of Activate commands before it can reassert ALERT_n for another Alert Back-Off. ALERT_n asserted for other operation such as Write DQ CRC errors is allowed with no timing restrictions.

ABO_Delay is specified by the number of Activate commands in MR71:OP[1:0].Commands that activate one or more rows in a DRAM include ACT, REFab/REFsb and RFMab/RFMsb and the MPC function Manual ECS, and any that occur are included in the total ABO_Delay Activate count allowed .

Following ABO_Delay, any of the commands included in clause clause 16.5.1.1 may trigger the ABO, as well as an ACT command.

16.5.1.3 Alert Back-Off Delays (cont'd)

Table 359 — Alert Back-Off Delay Parameter

Symbol	Description	Value	Unit	Note
ABO_Delay	Minimum number of Activate commands allowed	MR71:OP[1:0]	Activates	

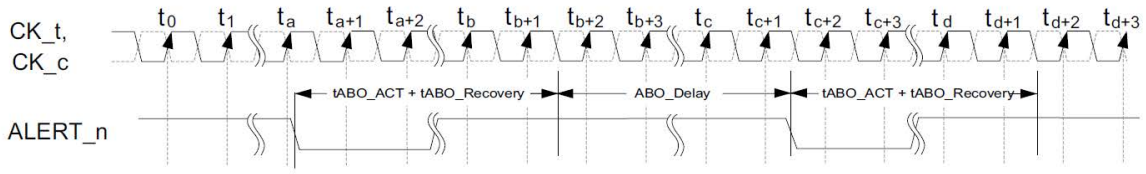


Figure 265 — Back to Back Alert Back-Off Delay

16.6 ALERT_n Priorities

At times, both Write CRC and Alert Back-Off may occur simultaneously resulting in an overlap of ALERT_n assertions, or the occurrence of the two events back-to-back (non-overlapped) may result in a short "glitch" on ALERT_n. For all events, the DRAM shall treat the ALERT_n as a "NOR" function where ALERT_n is issued whenever an event occurs, and the DRAM sets the corresponding Write CRC (MR50:OP[3]) or Alert Back-Off (MR70:OP[5] flag indicating which type of event, or possibly both, occurred.

16.7 Activation Counter Errors

The DRAM has the capability to detect errors that occur within the counter bits, and the following protocol defines how the DRAM will report the associated failing row address to the host.

If a counter bit error is detected, the DRAM sets the Counter Error Flag, MR72:OP[0]=1_B.

While the Counter Error Flag is set, the counter function for the specific row with the error is disabled. The DRAM will not assert the Alert Back-Off to request RFM commands for errors associated with that row. All other rows without counter errors continue to count activity and assert ALERT_n, if necessary.

During ECS (Manual or Auto mode), if the Counter Error Flag is set and the DRAM logs a failing row address, the DRAM will update MR73-MR75 with the failing row address and set the Counter Address Report Flag, MR72:OP[1]=1_B, when the ECS reaches the failing row. Only the first failing row will be reported. Additional rows will be reported in a subsequent scrub if they continue to fail after the Counter Address Report Flag is cleared by the host.

A counter RAS error that occurs during the ECS may still trigger the Counter Error Flag, but may not set the Counter Address Report Flag nor report the failing row address.

With the failing row address information, the host can repair the bad row with hPPR/sPPR or off-line that row.

The host clears the Counter Error Flag and Counter Address Report Flag, once the necessary information about the failing row has been collected and mitigative actions taken.

16.8 Per Row Activation Counting Testing

An optional test mode for PRAC may be included to check the ability of the DRAM to reach a threshold per row or fill the row address queue and issue the ABO. Test mode support is indicated by MR71:OP[4]=1_B.

PRAC Testing is enabled by setting MR71:OP[5]=1_B. Once enabled, the counter for target row to be tested is initialized by the host setting MR71:OP[6]=1_B, followed by an ACT/PRE to the target row. The host then sets MR71:OP[6]=0_B and issues 32 ACT/PRE or fewer to the target row or rows to trigger the ABO (multiple increments to the counter bits may occur depending on tRAS duration, mimicking normal operation). ABO is required as describe previously before testing subsequent rows.

Depending on counter bit starting values, all DRAMs on a DIMM may not trigger the Alert Back-Off at the same time (detected by MR70:OP[5]), however all DRAMs will trigger within 32 Activations.

After PRAC Testing has been complete, the test mode is cleared by setting MR71:OP[5]=0_B. Since the counter cells will be in an unknown state following testing, a full Activation Counter Initialization (ACI) is required before resuming normal operations.

Refresh commands are not allowed while PRAC Testing is enabled. Data in normal cells is not maintained during in PRAC Testing.

16.9 ALERT_n Verification

Support for an optional mode to verify ALERT_n is indicated by MR70:OP[6]=1_B.

ALERT_n Verification is triggered by setting MR70:OP[7]=1_B. The DRAM asserts ALERT_n and sets the ABO Flag at MR70:OP[5]=1_B within tMRD after the MRW and will keep ALERT_n asserted for tABO_PW. The host shall follow all normal ABO procedures for clearing the ALERT_n. MR70:OP[7] and MR70:OP[5] will be self-cleared by the DRAM prior to the end of the tABO_Recovery period.

For 3DS devices, only the base die triggers the ALERT_n and sets the ABO flag at MR70:OP[5]=1B in response to MR70:OP[7]=1B.

tABO_Recovery plus tABO_Delay shall be completed prior to triggering a subsequent ALERT_n Verification by setting MR70:OP[7]=1_B.

Data in normal cells is maintained during ALERT_n Verification, as long as refresh is maintained. No per row counter values nor thresholds are altered during this mode.

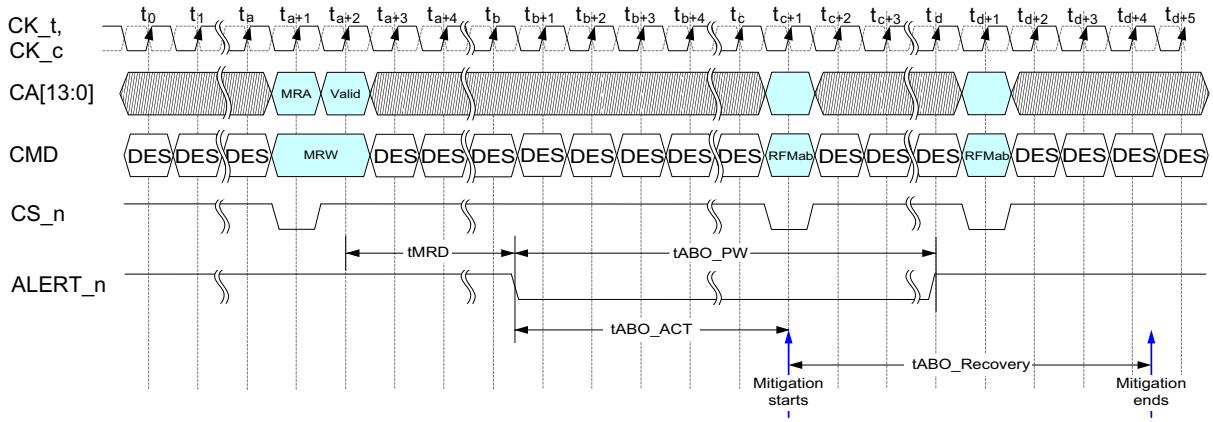


Figure 266 — Alert Verification Mode

16.10 PRAC and ABO Mode Register Definition

Table 360 — MR6 Register Information

Function	Register Type	Operand	Description	Notes
Write Recovery Time Legacy / PRAC	R/W	OP[3:0]	0000_B: 48nCK (Legacy) / 16nCK (PRAC) 0001_B: 54nCK (Legacy) / 18nCK (PRAC) 0010_B: 60nCK (Legacy) / 20nCK (PRAC) 0011_B: 66nCK (Legacy) / 22nCK (PRAC) 0100_B: 72nCK (Legacy) / 24nCK (PRAC) 0101_B: 78nCK (Legacy) / 26nCK (PRAC) 0110_B: 84nCK (Legacy) / 28nCK (PRAC) 0111_B: 90nCK (Legacy) / 30nCK (PRAC) 1000_B: 96nCK (Legacy) / 32nCK (PRAC) 1001_B: 102nCK (Legacy) / 34nCK (PRAC) 1010_B: 108nCK (Legacy) / 36nCK (PRAC) 1011_B: 114nCK (Legacy) / 38nCK (PRAC) 1110_B: 120nCK (Legacy) / 40nCK (PRAC) 1101_B: 126nCK (Legacy) / 42nCK (PRAC) 1110_B: 132nCK (Legacy) / 44nCK (PRAC) 1111_B: 138nCK (Legacy) / 46nCK (PRAC)	1
tRTP Legacy / PRAC	R/W	OP[7:4]	0000_B: 12nCK 0001_B: 14nCK 0010_B: 15nCK 0011_B: 17nCK 0100_B: 18nCK 0101_B: 20nCK 0110_B: 21nCK 0111_B: 23nCK 1000_B: 24nCK 1001_B: 26nCK 1010_B: 27nCK 1011_B: 29nCK 1110_B: 30nCK 1101_B: 32nCK 1110_B: 33nCK 1111_B: 35nCK	2

NOTE 1 tWR,min is defined in the “Timing Parameters” tables. Host must operate with MR settings resulting in tCK * MR6:OP[3:0] >= tWR,min.
NOTE 2 tRTP, min is defined in the “Timing Parameters” tables. Host must operate with MR settings resulting in tCK * MR6:OP[7:4]>= tRTP,min.
NOTE 3 All nCK conversions require rounding algorithm consideration.

16.10 PRAC and ABO Mode Register Definition (cont'd)

Table 361 — MR70 Register Information

Function	Register Type	Operand	Description	Notes
Per Row Activation Counting and Alert Back-Off Support (Optional)	R	OP[0]	0_B: PRAC and ABO not supported 1_B: PRAC and ABO supported	
Per Row Activation Counting and Alert Back-Off Enable/Disable	R/W	OP[1]	0_B: Disable PRAC and ABO (Default) 1_B: Enable PRAC and ABO	2,3
Activation Counter Initialization	R/W	OP[2]	0_B: Normal operating mode (Default) 1_B: Initialization mode	2
Activation Counter Initialization Complete	R	OP[3]	0_B: Initialization not completed 1_B: Initialization completed	1,2
RFU	RFU	OP[4]	RFU	
Alert Back-Off Flag	R	OP[5]	0_B: Clear 1_B: Source of ALERT_n	1
ALERT_n Verification Support (Optional)	R	OP[6]	0_B: ALERT_n Verification not supported 1_B: ALERT_n Verification supported	
ALERT_n Verification	R/W	OP[7]	0_B: ALERT_n Verification Disabled (Default) 1_B: ALERT_n Verification Trigger	

NOTE 1 MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced

NOTE 2 When PRAC is disabled, MR70:OP[1]=0_B, both MR70:OP[2] and MR70:OP[3] are reset to the default 0_B by the DRAM. Likewise when ACI is enabled, MR70:OP[2]=1_B, MR70:OP[3] is reset to 0_B by the DRAM.

NOTE 3 This bit can only be set by the host (MR70:OP[1]=1_B). An MRW with MR70:OP[1]=0_B will not disable PRAC. A Reset is required to disable PRAC once enabled. MRR to MR70:OP[1] will read aligned to PRAC enabled/disabled status.

Table 362 — MR71 Register Information

Functions	Type	Operand	Description	Notes
Min RFMab Commands during Recovery Period (ABO_RFM) and min ACT commands during Alert Back-Off Delay (ABO_ Delay)	R/W	OP[1:0]	00_B: 4 (Default) 01_B: 2 10_B: 1 11_B: RFU	
Adaptive Per Row Activation Counting	R/W	OP[3:2]	00_B: Default Mitigation Threshold (Default) 01_B: Mitigation Threshold Level A 10_B: Mitigation Threshold Level B 11_B: Mitigation Threshold Level C	
PRAC Testing Support (Optional)	R	OP[4]	0_B: PRAC Testing not supported 1_B: PRAC Testing supported	
PRAC Testing Enable/Disable	R/W	OP[5]	0_B: Disable PRAC Testing (Default) 1_B: Enable PRAC Testing	
PRAC Testing Initialization	R/W	OP[6]	0_B: Disable PRAC Testing Initialization (Default) 1_B: Enable PRAC Testing Initialization	
RFU	RFU	OP[7]	RFU	

16.10 PRAC and ABO Mode Register Definition (cont'd)

Table 363 — MR72 Register Information

Function	Register Type	Operand	Data	Notes
Counter Error Flag	R/W	OP[0]	0_B: Clear 1_B: Counter error detected	1,2
Counter Address Report Flag	R/W	OP[1]	0_B: Clear 1_B: Failing row address available in MR73-MR75	1,2
RFU	RFU	OP[7:2]	RFU	

NOTE 1 MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced.
NOTE 2 These flags can only be set by the DRAM. MRW of MR72:OP[0]=0_B or MR72:OP[1]=0_B will clear the flag. MRW of MR72:OP[0]=1_B or MR72:OP[1]=1_B by the host will read unchanged from what was previously in the MR (1 if set by the DRAM, otherwise 0).

Table 364 — MR73 Register Information

Function	Register Type	Operand	Data	Notes
8 bits of the row address	R	OP[7:0]	Activation Counter Error Row Address R[7:0]	1

NOTE 1 MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR73 through MR75 Activation Counter Error address data

Table 365 — MR74 Register Information

Function	Register Type	Operand	Data	Notes
8 bits of the row address	R	OP[7:0]	Activation Counter Error Row Address R[15:8]	1

NOTE 1 MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR73 through MR75 Activation Counter Error address data

Table 366 — MR75 Register Information

Function	Register Type	Operand	Data	Notes
2 bits of the row address	R	OP[1:0]	Activation Counter Error Row Address R[17:16]	1
2 bits of the bank address	R	OP[3:2]	Activation Counter Error Row Bank Address BA[1:0]	1
3 bits of the bank group	R	OP[6:4]	Activation Counter Error Row Bank Group BG[2:0]	1
RFU	RFU	OP[7]	RFU	

NOTE 1 MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR73 through MR75 Activation Counter Error address data

ANNEX A - (Informative) Differences between JESD79-5A and JESD79-5

This annex briefly describes most of the changes made to this standard, JESD79-5A, compared to its predecessor, JESD79-5 (July 2020). Some editorial changes are not included.

Changes Made in JESD79-5A

Section	Description of Change
2.2	Updated Section
2.6	Updated Table 3
2.7	Updated Table 6
3.1	Updated Section
3.3	Updated Table 9
3.3.1	Updated Section
3.4.1	Updated Section
3.5	Updated Section
3.5.1	Updated Table 24
3.5.6	Updated Section
3.5.8	Updated Section
3.5.9	Updated Section
3.5.11	Updated Section
3.5.14	Updated Section
3.5.15	Updated Section Updated Table 28
3.5.16	Updated Section
3.5.17	Updated Section
3.5.21	Updated Section
3.5.23	Updated Section
3.5.24	Updated Section
3.5.25	Updated Section
3.5.44	Updated Section
3.5.51	Updated Section
3.5.59	Updated Section
3.5.60	Updated Section
3.5.61	Updated Section
3.5.65	Added Section
3.5.66	Added Section
3.5.67	Added Section
3.5.68	Added Section
3.5.69	Added Section
3.5.70	Added Section
3.5.80	Updated Section

Changes Made in JESD79-5A (cont'd)

3.5.81	Updated Section
3.5.82	Updated Section
3.5.83	Updated Section
3.5.84	Updated Section
3.5.85	Updated Section
4.1	Updated Table 30
4.1.1	Added Section
4.4.3	Updated Section Updated Figure 15 Updated Table 38
4.6.1	Added Section
4.7.2.1	Updated Table 40 Updated Table 41
4.7.3	Updated Figure 34 Updated Figure 38
4.8.4	Updated Figure 47 Updated Figure 51
4.8.8.1	Updated Section Updated Table 56
4.9	Updated Section Updated Table 58
4.9.2	Added Section
4.10.1	Updated Table 62
4.13.5	Updated Table 72 Updated Table 73 Updated Table 74 Updated Table 75
4.13.6	Updated Figure 68
4.17.1	Updated Section
4.17.3	Updated Table 96
4.19.1	Updated Section
4.20.3	Updated Figure 85
4.21.1	Updated Section
4.21.2	Updated Section
4.21.3	Updated Section
4.21.4	Updated Section
4.21.5	Updated Section
4.23.2	Updated Section
4.24.1	Updated Table 120
4.24.2	Updated Table 121
4.25.1	Updated Table 122
4.25.2	Updated Table 123
4.26	Updated Table 125
4.29	Updated Section Updated Figure 123 Added Table 131

Changes Made in JESD79-5A (cont'd)

4.29.1.1	Updated Section Updated Figure 124
4.29.2	Updated Section
4.29.2.1	Updated Section Updated Figure 125
4.29.2.2	Added Section
4.29.2.3	Added Section
4.3	Added Section
4.31.1	Updated Section
4.31.3	Updated Table 137 Updated Figure 133
4.32	Updated Section Updated Table 139 Added Figure 137 Added Figure 138
4.33	Updated Figure 140 Updated Figure 141
4.34.1	Updated Figure 144
4.37.1	Updated Section
4.37.2	Updated Section
4.37.3	Updated Section
4.39.1	Updated Section
4.39.3.3	Added Section
4.39.3.4	Updated Section Updated Table 159
4.39.3.6	Added Section
4.39.3.6	Added Section
4.39.4	Updated Section
4.4	Updated Section
4.40.1	Updated Section
4.41.1	Updated Figure 165
4.42	Updated Section
4.42.1	Added Section
4.43	Updated Section
5.4.1	Updated Table 173
6.3	Updated Table 177
8.2	Updated Table 189
8.3.2	Updated Section
8.4	Updated Figure 203 Updated Table 193
8.5.1	Updated Table 191
8.6.1	Updated Section Updated Table 204
8.7.2	Updated Table 209 Updated Table 210
8.8	Updated Figure 210 Updated Table 212

Changes Made in JESD79-5A (cont'd)

8.8.1	Section removed
8.8.2	Section removed
8.9.1	Updated Figure 211
8.9.2	Updated Table 213 Updated Table 214 Updated Figure 212
8.9.3	Added Section
8.9.4	Added Section
8.10.1	Updated Table 222 Updated Table 223 Updated Table 224
9.6	Updated Table 240 Updated Table 241
9.8	Updated Table 246 Updated Table 247
9.10.2	Updated Table 253
9.11.1	Updated Table 255
10.1	Updated Table 258
10.2	Updated Table 259
10.3	Updated Table 260
10.4	Updated Table 261
10.5	Updated Table 262
10.6	Updated Table 263
10.7	Updated Table 264
10.8	Updated Table 265
10.9	Updated Table 266
10.1	Updated Section
10.11	Updated Table 267
10.12	Updated Table 268
10.13	Updated Table 269
10.14	Updated Table 270
10.15	Updated Table 271
10.16	Updated Table 272
10.17	Updated Table 273
10.18	Updated Table 274
10.19	Updated Table 275
10.2	Updated Table 276
10.21	Updated Table 277
10.22	Updated Table 278
10.23	Updated Table 279
10.24	Updated Table 280
10.25	Updated Section
10.26	Updated Table 281
10.27	Updated Table 282

Changes Made in JESD79-5A (cont'd)

10.28	Updated Table 283
10.29	Updated Table 284
10.3	Updated Table 285
11.1	Updated Section Updated Table 286
11.2	Updated Table 287
11.3	Updated Table 288
11.4	Updated Section Updated Table 289
11.5	Updated Section
	Updated Table 290
11.6	Updated Table 291
11.7	Updated Table 292
11.8	Section removed; following sections renumbered
11.8	Updated Section Updated Table 293
11.9	Updated Section Updated Table 294
11.1	Updated Section Updated Table 295
11.11	Updated Section Updated Table 296
12	Updated Table 297 Updated Table 298 Updated Table 299 Updated Table 300
13.2	Updated Section
13.2.1	Updated Table 302
13.2.2	Updated Table 303
13.3	Updated Section
13.3.1	Updated Table 304
13.3.2	Updated Table 305
13.3.3	Updated Table 306
13.3.6	Updated Table 309
13.3.7	Updated Table 310
13.3.8	Updated Table 311
15	Added Chapter

ANNEX B - (Informative) Differences between JESD79-5B and JESD79-5A

This annex briefly describes most of the changes made to this standard, JESD79-5B, compared to its predecessor, JESD79-5A (October 2021). Some editorial changes are not included.

B.1 General Editorial Changes

- Corrected typographical errors
- Added space between number and unit of measure
- Figure titles at bottom of figure
- NOTES placed inside tables
- Replaced instances of specification with standard
- Replaced ampersand (&) with "and" except inside tables
- Oxford comma
- Change "must" to "shall"
- Updated cross references for tables and figures
- Added missing figure and table titles for consistency with JESD79-5A (Table title numbers 1, 2, 3, 25, 58, 114, 115, 116, 117, 118, 167, 168, 169, 170, 248, 249, 326, and 327

B.2 Changes from JC-42.3 Meetings

- DDR5_Package_Electrical_Spec_Values_5200_5600
- DDR5_ZQ_Calibration_Commands_Ballot” with grayed notes added below the calculation examples
- Added DDR5 Power Up Sequence Clarification
- DDR5 DFE Figure Clarification Ballot
- DDR5 PPR Address note for 24Gb
- DDR5 Sref Operation tREFI Postpone
- DDR5 Sref tREFI Postpone
- DDR5 Self Refresh Frequency Change
- DDR5 CA NOP State during CSTM
- DDR5 IDD2 Clarification
- DDR5 WB suppression Clarification
- DDR5 Power Down Timing Note Update
- DDR5 CT Mode Timing Alignment
- DDR5_Mono_AC_Timing_Parameters_6800-7600
- DDR5 VrefCA CS DQ min Correction
- DDR5 tRx_DQS2DQ Clarification
- DDR5 6400 Speed Bin Table Correction
- DDR5 DCA Training Assist Mode 2 Clarification
- DDR5 DQS Slew Rate 3200 6400
- RB22-050_DDR5 tADC 6800-7600
- DDR5 RFM Enhancements
- DDR5 tWPST 3200-6400
- DDR5 Input Clock Slew Rate 5200 6400
- DDR5 AC DC Output Levels SESR DIFSR 6000 6400
- DDR5 Rx Stressed Eye Tests 6000 6400
- Rx Clock_Voltage_Sensitivity_6000_6400
- Rx_DQS_Voltage_Sensitivity_6000_6400
- Rx_DQ_Voltage_Sensitivity_6000_6400
- DDR5 Silicon Pad IO Capacitance 6000 6400

ANNEX B - (Informative) Differences between JESD79-5B and JESD79-5A (cont'd)

- DDR5 PDA Diagrams
- DDR5 MRR MRW MPC timing
- Loopback Output Timing Parameters
- DDR5 Rx DQS Jitter Sensitivity 6000 6400
- DDR5 RFM Enhancements Ballot DRFM
- DDR5 MRR MRW MPC timing R1", where 3DS MRR to be confined to all banks idle state
- DDR5 JEDEC Draft Spec Rev1.81 Voting Comments
- DDR5 Draft 181 feedback

B.3 Changes from Task Group Meetings

- DDR5 PDX during tRFC
- DDR5 DataRate Clarifications
- Typo correction in DDR5-3DS-3200AN's tRC
- DDR5 CA CS Rx Mask Clarification
- DDR5 Rounding Algorithm for Max Parameters
- DDR5 tWR Rounding Algo Propagation
- MR4 Editorial Update for Wide Temperature Changes
- DDR5 tPGM Clarification
- DDR5 IDD Editorials
- Intel_Clock_Jitter.pdf
- DDR5 Rounding Algorithm for Negative Values
- DDR5 DQS2DQ Volt 5200-6400
- DDR5 tWPST 3200-6400
- DDR5 Read Preamble Training Clarification
- DDR5 DCA Training Assist Mode 2 Clarification
- DDR5 ODT Timing Cleanup
- DDR5 Package Output Driver Test Mode Clarification
- DDR5 Write CRC Auto Disable Clarification
- DDR5 Package Electrical Spec Values 5200 6400
- DDR5 Mono Speed Bin Tables 6800-7200
- Typographical errors corrected
  - page 213, "Determin" to "Determine", "ragne" to "range", MR4:OP5[]=1" to MR4:OP[5]=1",
  - page 364, in Figure 192's timing indicator tf+5 to tf+5", Figure 193, add "RTT_PARK" in yellow RTT area
  - page 365, in Figure 194, add "RTT_PARK" in yellow RTT area
  - page 367, in Figure 198, add "DQS_RTT_PARK" for R0 DQS RTT
  - page 367, in Figure 199, add "DQS_RTT_PARK" for R0 DQS RTT
  - page 44, section 3.4.1, "MRR NT ODT MRRMRR" to "MRR NT ODT"
  - page 49, in Figure 9, add "DQS_RTT_PARK" for R0 DQS RTT"
  - page 344, Section 4.42 title, remove "a" in front of "Refresh"
  - page 404, in Figure 225, change line color from red to black
  - page 425, in Figure 243, updating RB22054 for SRQdiff for 6000 and 6400
  - page 225, in Figure 76, remove term "spacing" for note 1
  - page 226, in Figure 78, remove term "spacing" for note 1
  - page 418, modified context for tLBQ_Set, tLBQ_Hld definition to properly describe behavior by removing "t", i.e. "tLBDQS / tLBDQ" to "LBDQS / LBDQ", "tBDQS / tLBDQ" to "LBDQS / LBDQ", respectively
  - page 398, in Table 193, reflectin approved ballot RB22056, adding (*120) for 6000 and 6400
  - page 97/98, fixing typo for "issuing any MRR" to "Issuing any MRR", and MRW to MR42:OP[7 0 to MRW to MR42: OP[7]=0"
  - page 40, changing ALERT_N to ALERT_n

ANNEX B - (Informative) Differences between JESD79-5B and JESD79-5A (cont'd)

- page 298, in Figure 138, changing ALERT_N to ALERT_n
- page 328, in Figure 159, changing Alert_n to ALERT_n
- page 170, 1st sentence to reflect behavior correctly, "The following read timing diagrams cover write timings for fixed BL32" to "The following read timing diagrams cover read timings for fixed BL32"
- page 172, in Figure 42, subsequent READ operation's DQ burst to be shifted right 0.5UI for edge-aligned behavior
- page 173, in Figure 43, subsequent READ operation's DQ burst to be shifted right 0.5UI for edge-aligned behavior

• Typographical and formatting errors corrected

- page 116, removed MR61 with note pointing nowhere
- page 355, Section 5.1 title modified to add "DQS, DM, and TDQS"
- page 498, Table 294 updated in accordance to numbering
- page 39, section 3.3.1's sequence 1 should point to Table 7, where it was used to be Table 2
- page 40, Figure 3's note 3 of (Tz) to be changed to (Tk)
- page 447, removed Speed Bin for 6400 duplicated Supported CL rows
- page 492, Table 295, removed unnecessary 6000/6400 columns
- page 39, note 3 in figure 3, "no execute" not "execute"
- page 179, "WR_partial" to "WR_Partial (WR_P)" in section 4.8.1
- page 492, table's label from "DDR5-5200/6400 to DDR5-5200 to DDR5-6400"
- WR_Partial has numerous combinations of Upper/Lowercases

• page 456, DDR5-8400 speed bin was not properly updated, so reflected based on "DDR5 Mono Speed Bin Tables 6800-7200

• Feedback on DDR5 Rx Eye Mask and CA Td and Cck Ci

• CSGeardown_rev06_Opt2.pdf

• DDR5 Draft 183 feedback

• DDR5 MR59 Editorial Update

ANNEX C - (Informative) Differences between JESD79-5C and JESD79-5B

This annex briefly describes most of the changes made to this standard, JESD79-5C, compared to its predecessor, JESD79-5B (September 2022). Some editorial changes are not included.

C.1 Editorial Changes

- 7200 Tx Rx Specs
- Added missing MR42 DCA TAM1's footnote reference from RB21-223 "DDR5 DCA Training Assist Mode II for DCA Training based on 4-phase Clocks R2"
- ARFM Clarification
- BL32 Clarification
- Changed all the red texts into black, changed red texts in the figures, and highlight changes made into black, in particular for section 4.16.1, Figure 76 through Figure 89, and section 5.3.2, Figure 186 through Figure 199
- Cio min timing
- Continuous Burst Mode Timing Clarification
- CS geardown DRAM internal clock clarification
- CS_Geardown_Clarification for option B only
- DDR5 8400-8800 tCCD M tRRD L
- DDR5 Data Output Disable
- DDR5 DDP CA ODT
- DDR5 Rounding Algo CWL Clarification
- DDR5 Same BG CRC Timing Adder incorporated with "WR to WR timings
- Timing Diagram Figure Correction
- DQ Requirement WPRE Interamble
- DQ Requirement Write Preamble Interamble
- DRFM_Clarification
- Editorial update of the Copyright and Notice pages
- Figure 3 RESET initial vertical location
- Fixed notes numbering order, used to be started from 14th, changed those to be started from 1st, in Section 10.30
- IDD6 ODT Editorial update
- IO Capacitance Editorial Update
- Loopback Output Timing
- Loopback Write Burst Output Mode Clarification
- MBIST mPPR Feedback
- MPC Bank State Editorial
- MPC Editorial update
- MPSM Idle MRW Command
- MR18 MR54-57 update
- MR42 Note11
- MR43-44 Typo Correction
- MR53 Editorial Update
- MRR to MRW Timing Constraint
- p299, mPPR Timings table numbering
- p315, table numbering is missing, and corrected to table 142,
- p350, referencing table 2 to be fixed to section MR 3.5.15,
- p361 through p366, figure 186 through figure 199, containing red texts in the diagram turned into black texts
- p391, table 199 title has upper bounded by 6800, but fixed to 8800,
- p397, section 8.6.2 had wrong referencing, table 2, which was fixed to table 207,
- p435, Tx Stressed Eye's table 254 modified to reflect "DDR5 Tx DQ Stressed Eye Spec Clarification for the DDR5-3200 through DDR5-4800 to remove EH/EW for 4UI and 5UI cases

ANNEX C - (Informative) Differences between JESD79-5C and JESD79-5B (cont'd)

- PKG Capacitance 6800-7200
- Power Up Init Reset
- PowerDown_description to remove "while the target SDRAM remains"
- Power-up initialization RTT clarification
- Pre Pst Timing Parameters
- Preamble and Postamble for lower data rate
- Read Training Pattern
- Refresh Description Words
- RFMsb Clarification
- Rx CA CS Voltage and Timing 6800-7200
- Rx Stressed Eye Tests 7600-8000
- sPPR Undo Lock Clarification
- SRX CLK Sync
- tRRD Clarification "w/o REFab"
- tSYNC GEAR/tCND GEAR Timing
- Tx DQ Stressed Eye Spec Clarification
- TX Stress Eye Clarification
- Typo correction made in Section 10.30, note 12 in page 498 to reflect Write CRC contemplation properly
- Write Leveling Editorial
- Write_to_Write_Timing_Clarification
- x4_RMW_ECS_Writeback_Clarification
- ZQCAL Timing

C.2 Modifications

- 2-cycle command cancel clarification
- 3DS AC Timing Parameters
- 3DS Speed Bin Tables 7600-8800
- AC DC Output Levels SESR_DIFSR 8400 to 8800
- AC DC Output Measurement Levels VOL VOH SESR & DIFSR 7600-8000
- CK VIX 6800-7200
- CK VIX 7600-8000
- CK VIX 8400 to 8800
- Clock Slew Rate 6800-7200
- Clock Slew Rate 7600-8000
- Clock Slew Rate 8400 to 8800
- CSGeardown
- DDP AC DC Output Levels SESR_DIFSR 3200 to 6400
- DDP Package, Pinout Description and Addressing
- DDP Pinout
- DDP PKG Capacitance 3200 to 6400
- DDP Timings
- DDR5 Per Row Activation
- Deleted Chapter 17
- DQS Slew Rate 6800-7200
- DQS Slew Rate 7600-8000
- DQS Slew Rate 8400 to 8800
- DQS VIX 6800-7200
- DQS VIX 7600-8000

ANNEX C - (Informative) Differences between JESD79-5C and JESD79-5B (cont'd)

- DQS VIX 8400 to 8800
- ECS MR Selections
- EOL Array Timings
- Input Clock Jitter 6000-6400
- Input Clock Jitter 6800-7200
- Input Clock Jitter 7600 to 8800
- IO Timing Parameters Clarification
- JESD79-5_IDD_IPP_tables
- Loopback output timing parameter
- Modified section 3.5, MR overview from MR70 thru MR75 to allow for PRAC addition
- Mono AC Timing Parameters 7600-8800 with Edit update for tCCD_M and tRRD_L to 17nCK for 8400 and 8800
- Mono Speed Bin Tables 7600-8800
- MPC DLL RESET Clarification
- PASR Defeature
- PDE/PDX NT Commands
- Per Row Activation
- PKG Capacitance 6800-7200
- PKG Capacitance 7600 to 8800
- PMIC Reference update
- Power Ramp Down Time Clarification
- Power-up initialization
- Preamble/Postamble Measurement Method
- READ Preamble/Postamble Timing Parameters
- Rearranged WRP into tXS_DLL
- Refresh Description Clarification
- Rx CA CS Voltage and Timing 6800-7200
- Rx CA CS Voltage and Timing 7600 to 8800
- Rx CA CS Voltage and Timings new format
- Rx Clock Voltage Sensitivity 6800 7200
- Rx Clock Voltage Sensitivity 7600-8000
- Rx Clock Voltage Sensitivity 8400-8800
- Rx DQ Voltage Sensitivity 6800-7200
- Rx DQ Voltage Sensitivity 7600-8000
- Rx DQ Voltage Sensitivity 8400 to 8800
- Rx DQS Jitter Sensitivity 6800 7200
- Rx DQS Jitter Sensitivity 7600-8000
- Rx DQS Jitter Sensitivity 8400 to 8800
- Rx DQS Voltage Sensitivity 6800 - 7200
- Rx DQS Voltage Sensitivity 7600-8000
- Rx DQS Voltage Sensitivity 8400 to 8800
- Rx Stressed Eye 6800 7200
- Rx Stressed Eye Tests 8400 to 8800
- Silicon Pad IO Capacitance 6800-7200
- Silicon Pad IO Capacitance 7600-8000
- Silicon Pad IO Capacitance 8400 to 8800
- Silicon Pad IO Capacitance DDP 3200 to 6400
- SRX Clock-Sync
- State diagram for MPC functions requiring all banks idle
- tADC Measurement Method
- tFAW_dlr REFab Clarification

ANNEX C - (Informative) Differences between JESD79-5C and JESD79-5B (cont'd)

- tREFABRD_dlr
- tRRD_dlr Clarification
- Tx DQ Jitter 6000-6400
- Tx DQ Jitter 6800 7200
- Tx DQ Jitter 6800-8000
- Tx DQ Jitter 8400 to 8800
- Tx DQ Stressed Eye 6800 7200
- Tx DQ Stressed Eye 7600-8000
- Tx DQ Stressed Eye 8400 to 8800
- Tx DQS Jitter 6000-6400
- Tx DQS Jitter 6800 7200
- Tx DQS Jitter 6800-8000
- Tx DQS Jitter 8400 to 8800
- Tx_DQ_Stressed_Eye_6000_6400
- VOL VOH SESR & DIFSR 6800-7200
- Write Leveling Clarification
- Write Preamble Update
- Write to Write Timing Feedback

ANNEX D - (Informative) Differences between JESD79-5C.01 and JESD79-5C

This annex briefly describes most of the changes made to this standard, JESD79-5C.01, compared to its predecessor, JESD79-5C (April 2024). Some editorial changes are not included.

Correction of typographical errors that were not screened out during the voting process but were subsequently approved by the JC-42.3 Task Group TG423B5.

- Table 223: Change table title from “...to 8400” to “...to 8800”
- Table 232: Change header title (1st row) from “DDR5 6800-8400” to DDR5 6800-8800”
- Table 252: Change header title (1st row) from “DDR5 6800-8400” to DDR5 6800-8800”
- Table 255: Change header title (1st row) from “DDR5 3200-6400” to DDR5 6800-8800”
- Clause 10.15 on pages 407-408, footnote 12: Change 8000 to 8400 and 8400 to 8800 (similar to clause 10.30 footnote 12)
- Table 327: Change header title (1st row) from “... to DDR5-4800” to “... to DDR5-6400”

Editorial reformatting of the Table of Contents to add the document title “DDR5 SDRAM” at the top of each page per the newly revised JEDEC Manual JM7A “Style Manual for Standards and Other Publications of JEDEC”.

ANNEX E - (Informative) Differences between JESD79-5D and JESD79-5C.01

This annex briefly describes most of the changes made to this standard, JESD79-5D, compared to its predecessor, JESD79-5C.01 (July 2024). Some editorial changes are not included.

Major functional changes and correction of typographical errors that were not screened out during the voting process but were subsequently approved by the JC-42.3 Task Group TG423B5.

- Mono AC Timing Parameters 9200
- 3DS AC Timing Parameters 9200
- CK VIX 9200
- DQS VIX 9200
- AC DC Output Levels VOL VOH SESR DIFSR 9200
- Rx Clock Voltage Sensitivity 9200
- PKG Capacitance 9200
- Rx DQS Jitter Sensitivity 9200
- Tx DQ Stressed Eye 9200
- Tx DQ Jitter 9200
- Tx DQS Jitter 9200
- Silicon Pad IO Capacitance 9200
- Rx CA CS Voltage and Timing 9200
- DQS Slew Rate 9200
- Clock Slew Rate 9200
- Mono Speed Bin Tables 9200
- 3DS Speed Bin Tables 9200
- Rx DQS Voltage Sensitivity 9200
- Rx DQ Voltage Sensitivity 9200
- Rx stressed eye tests 9200
- 9200 General Spec Updates
- Input Clock Jitter 9200
- Z(f) removal (modified Table 196 - DC Operating Conditions, deleted old Figures 212 and 213)
- Edits on typo for table 223 title from “... to 8400” to “...to 8800”
- Edits on typo of 8400 to 8800 in table 232’s 1st row
- Edits on typo of 8400 to 8800 in table 252’s 1st row
- Edits on typo of “3200 to 6400” to “6800 to 8800” in table 255’s 1st row
- Edits on typo 8000, 8400s to 8400, 8800s
- Edits on typo from 4800 to 6400, 8000, 8400s to 8400, 8800s
- Edits on typo in tPDA_DQS_DELAY at 3600, 4400 in table 89, 90
- Edits on typo of command described in MPSM Deep Power Down State [4.12.3] section
- Update table 37 notes to match table 38 notes
- Edits on typo by exchanging column of BA0 and BA1 in table 64
- Edits on verbiage described in DRFM [4.42.2] section
- Edits on editorial items described in DDR5 Per Row Activation Counting_R8
- tCCD_WR_dpr Parameter Removal in table 339, 340, 341, 342, 343, 344, 345
- Update for Per Row Activation Counting solution, based on DDR5 Per Row Activation Counting_R9 ballot
- DDR5_PRAC_PPR_Clarification_R3
- DDR5_PRAC_tRTP_Timing_Extension_fast_track_ballot_proposal_r2
- DDR5_Per_Row_Activation_Counting_Ballot_R10a
- Edits on “DDR5_PRAC_R10_Presentation_Updated”
- Edits on “DDR5 IO Capacitance_Editorial”
- Edits on “DDR5 JESD79-5C.01 v1.31 PDA clarification R2”
- Edits on “DDR5 tCCD clarification”

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Standard Improvement Form **JEDEC Standard JESD79-5D**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

3. Other suggestions for document improvement:

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Company: _____ E-mail: _____
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